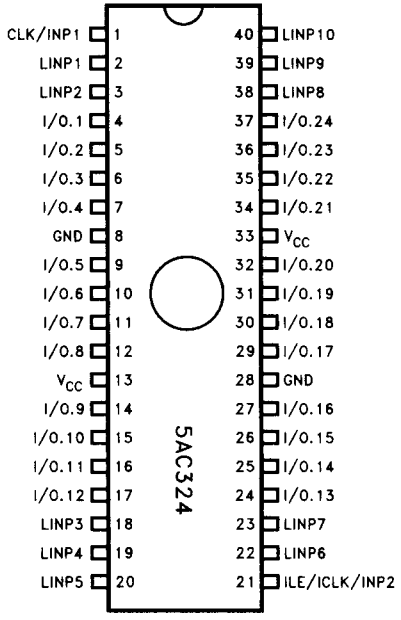
5AC324
1-MICRON CMOS 24-MACROCELL PLD

- **High-Performance LSI Semi-Custom Logic Alternative to Low-end Gate Arrays, TTL, 74HC SSI and MSI Logic, and PLDs**
- **High Speed t_{PD} 25 ns, 66 MHz Performance Pipelined, 33.3 MHz w/ Feedback**
- **24 Macrocells with Programmable I/O Architecture; Up to 36 Inputs (12 Dedicated, 24 I/O)**
- **10 Programmable Inputs Configurable as Latches, Registers, or Flow-Through**
- **1 Flow-Through Input or Global CLK Pin; 1 Flow-Through Input or Global ILE/ICLK Pin**
- **Programmable AND, Allocatable OR Design Allows up to 16 P-Terms per Macrocell**
- **Software-Supported P-Term Allocation Between Adjacent Macrocells**
- **Programmable Output Registers Configurable as D, T, JK, or SR Types**
- **Dual Feedback on All Macrocells for Implementing Buried Registers with Bidirectional I/O**
- **2 P-Terms on All Macrocell Control Signals**
- **Programmable Low-Power Option for "Stand-by" Operation; 150 μA Typical Standby Current**
- **UV Erasable (CerDIP) EPROM Technology or OTP**
- **100% Generically Tested EPROM Logic Control Array**
- **JEDEC Pinout**
- **Available in 40-pin CerDIP/PDIP and 44-Pin PLCC Packages**

(See Packaging Spec., Order Number 240800, Package Type D, P, and N)



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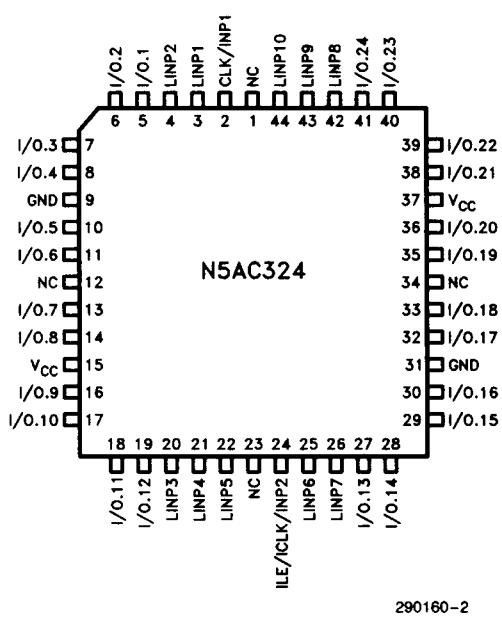

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Figure 1. 5AC324 Pinout Diagrams

INTRODUCTION

The Intel 5AC324 CMOS PLD (Programmable Logic Device) is a high integration device that overcomes the primary limitations of standard PLDs. Due to a proprietary I/O architecture and macrocell structure, the 5AC324 is capable of implementing high performance logic functions more effectively than previously possible. The 5AC324 can be used as an alternative to low-end gate arrays, multiple programmable logic devices, or LS-, HC-, or HCT SSI and MSI logic devices. Input and macrocell features for the 5AC324 are a superset of features offered on other PLD-type products.

The 5AC324 uses advanced CMOS EPROM cells as logic control elements instead of poly-silicon fuses. This technology allows the device to operate at levels necessary in high performance systems while significantly reducing power consumption. Its programmable standby mode reduces power to near zero in applications where a slight speed loss is traded for power savings.

ARCHITECTURE DESCRIPTION

The architecture of the 5AC324 is based on the familiar "Sum-Of-Products" programmable AND, fixed OR structure. This structure is then surrounded by powerful, programmable macrocells and inputs. The 5AC324 can implement both combinatorial and sequential logic functions through a highly flexible macrocell and I/O structure. The architecture of the device supports both combinatorial-register and register-combinatorial-register forms of logic to easily accomodate state machine designs.

Figure 2 shows a global view of the 5AC324 architecture. The 5AC324 contains a total of 24 I/O programmable macrocells, 10 programmable input structures, and two clock inputs that can be programmed to function either as combinatorial inputs or clock inputs for the input structures and macrocells.

Each of the ten programmable inputs can be individually configured as a latch, register or flow-through

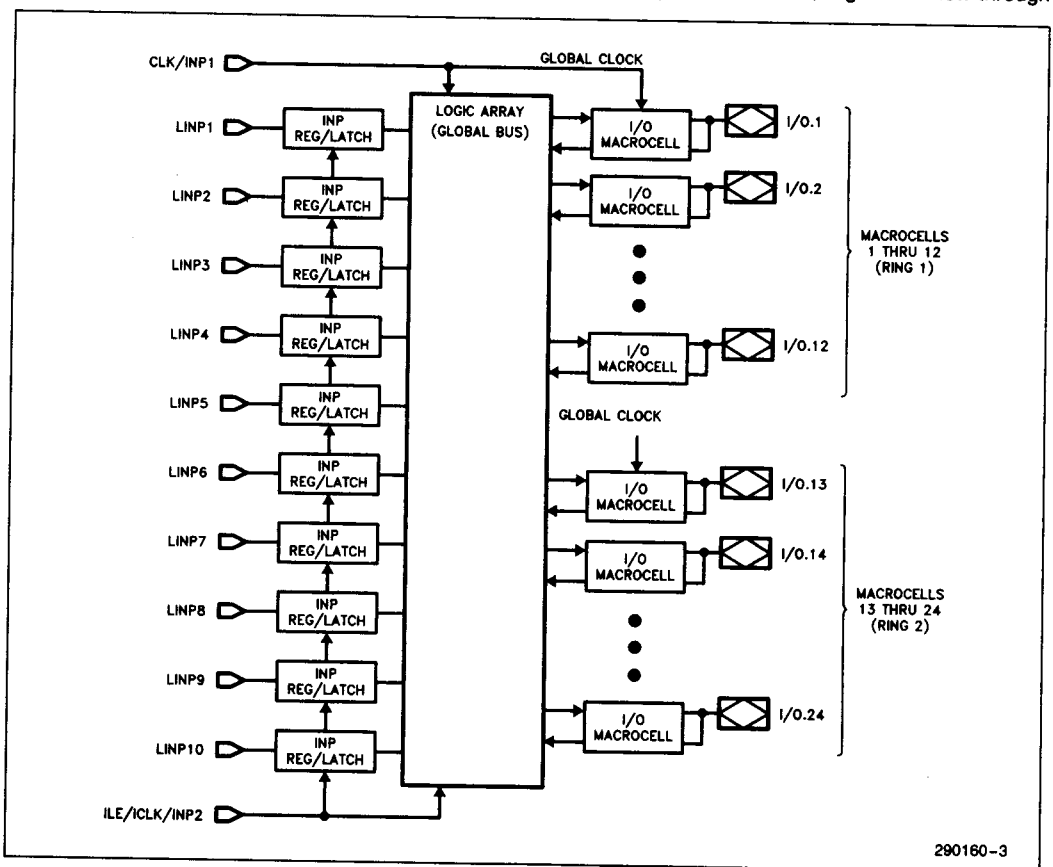


Figure 2. 5AC324 Global Architecture

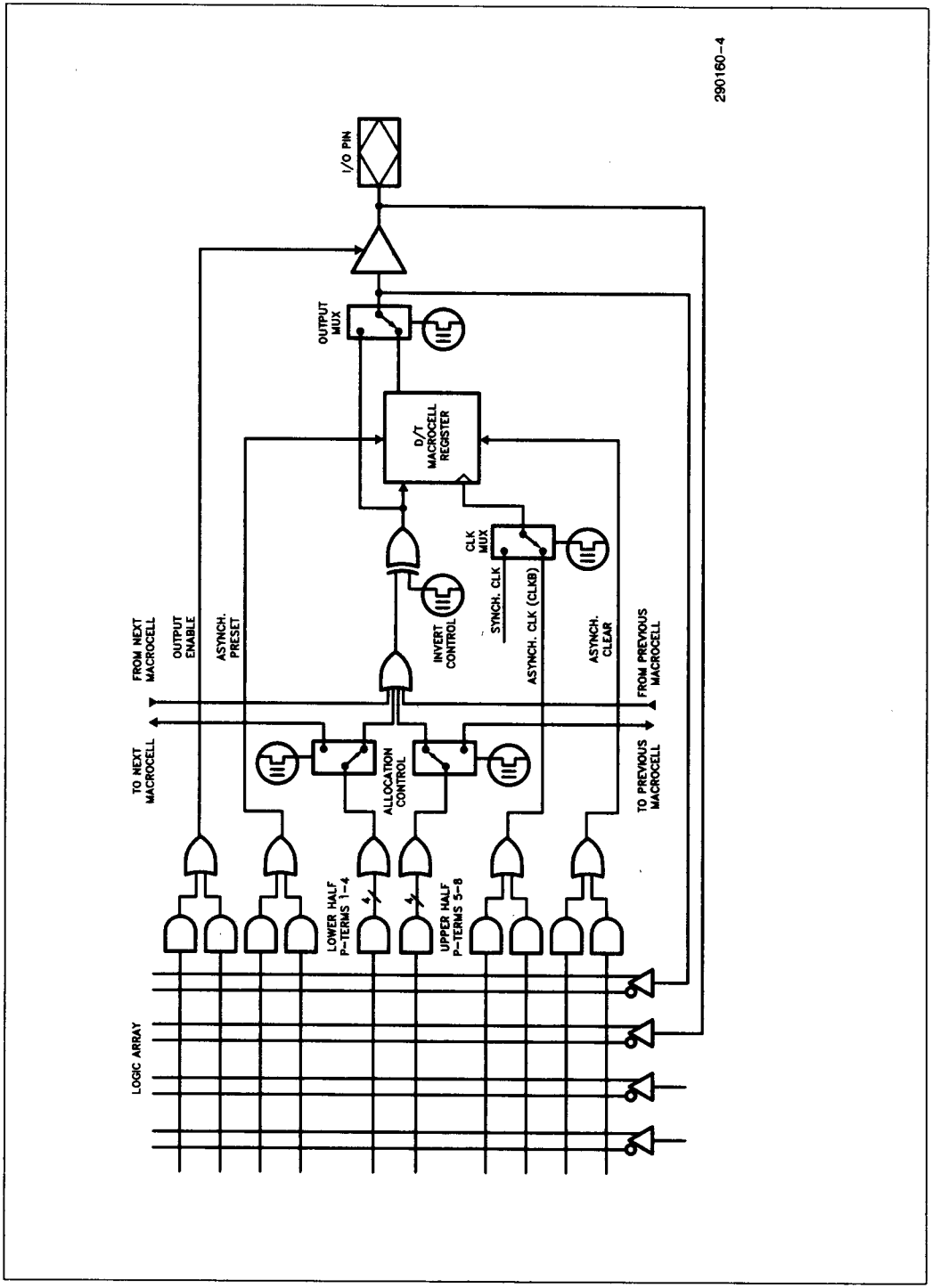


Figure 3. 5AC324 Macrocell Architecture

input. Input latches/registers can be synchronously or asynchronously clocked.

Figure 3 shows the basic architecture of each of the 24 macrocells in the 5AC324. Each macrocell contains 16 p-terms (product terms), with 8 p-terms available for the global array and 8 p-terms dedicated to the four control signals: OE, PRESET, CLEAR, and ASYNCH. CLK. The 8 p-terms from the logic array are organized as a user-programmable AND array and a user-configurable OR array. The inputs to the AND array originate from the true and complement signals from the programmable input structure, the dedicated inputs, and the 48 feedback paths from the 24 I/O macrocells to the global bus. This global bus simplifies designing with the device by eliminating the need to partition a circuit to fit into a local/global internal bus structure.

PROGRAMMABLE INPUTS

Figure 4 shows a block diagram of the 5AC324 input structure. The device contains 10 user-programmable inputs that can be individually configured to operate in one of five modes:

- input register (D-register), synchronously clocked
- input register (D-register), asynchronously clocked
- input latch, (D-latch), synchronously clocked
- input latch, (D-latch), asynchronously clocked
- Flow-through input

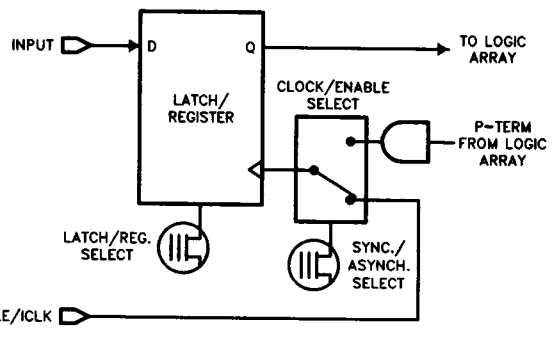
Configuration is accomplished through the programming of EPROM architecture control bits via the logic compiler and programmer software. If synchronous operation is selected, the ILE/ICLK pin is used as a global latch/clock to all input latch/register structures. For asynchronous operation, a separate product term in the array is used to derive the ILE/ICLK signal for each input structure. Because the clock signal for each programmable input can be individually selected, a mix between synchronously and asynchronously clocked inputs is possible. Software can configure each input structure as a flow-through input by selecting a latch and tying the ILE p-term to VCC. Data is latched/clocked on the falling edge of ILE/ICLK (synchronous mode). ILE/ICLK can function as an input to the logic array at the same time as it is used to synchronously clock the input registers.

MACROCELLS

Each of the 24 macrocells in the device contains 8 p-terms to support logic functions and 8 p-terms for control signals. The 8 p-terms for logic functions are subdivided into 2 groups, each with 4 p-terms. This grouping of p-terms supports the proprietary p-term allocation scheme in the 5AC324. Each macrocell also provides dual feedbacks to the logic array, which results in more efficient macrocell/pin usage than possible with single feedbacks.

Register Configuration

Each macrocell can be configured as a D, T, RS, or JK register. The 8 p-terms for control functions are organized so that 2 p-terms support each of the 4 control signals: Output Enable (OE), asynchronous I/O preset (PRESET), asynchronous I/O reset (CLEAR), and asynchronous I/O register clock (ASYNCH. CLK). Availability of 2 p-terms per control signal is another feature that increases the efficiency of the device by reducing the need to use intermediate macrocells sometimes needed to implement control functions.



NOTE:
Software implements a direct (flow-through) input by selecting an asynchronous latch and tying its control P-term to V_{CC}.

Figure 4. 5AC324 Programmable Input Structure

CLK is a global clock signal that can be used to synchronously clock any or all macrocell registers. When CLK is not used as a synchronous clock, it functions only as a dedicated input to the logic array. CLK can be used as an input to the logic array at the same time as it is used as a macrocell clock.

Combinatorial Configuration

The macrocell register can be bypassed to implement combinatorial logic functions. When configured to provide combinatorial logic, only the OE control signal is used.

Invert Select Bit

An invert select EPROM bit is used to invert the product term input into each macrocell register, including double inputs on JK and SR registers. This invert option allows the highest possible logic utilization by use of DeMorgan's logic inversion.

LOGIC ARRAY

Each intersecting point in the logic array contains a programmable EPROM connection. Initially (erased state), all connections are complete, i.e., both true and complement states of all signals are connected to each p-term.

Connections are opened during programming. When both the true and complement connections exist, a logical false results on the output of the AND gate. If both the true and complement connections of a signal are programmed "open", then a logic "don't care" results for that signal. If all connections for a p-term are programmed open, then a logical true results on the output of the AND gate.

PRODUCT TERM ALLOCATION

Product Term (p-term) allocation is defined as taking logic resources (p-terms) from macrocells where they are not used to support demand for additional p-terms in other macrocells. In the 5AC324, p-term allocation can occur in increments of 4 p-terms between adjacent macrocells. The 5AC324 includes 2 rings of 12 macrocells each. P-term groups from one macrocell can be allocated to the adjacent macrocell in the ring. P-term allocation between the two rings is not supported.

EXAMPLE:

Figure 5 shows a p-term allocation example. In this example, the logic function in macrocell 4 requires 16 p-terms. In this case, software allocates 4 p-terms from the previous macrocell in Ring 1 (macrocell 5) and 4 p-terms from the next macrocell (macrocell 3) to accumulate a total of 16 p-terms (8 + 4 + 4). This implementation leaves macrocells 3 and 5 with a remainder of 4 p-terms. These remaining p-terms can also be allocated away to, or supplemented with p-terms from, their adjacent macrocells in Ring 1 (macrocells 2 and 6).

With this scheme, any macrocell inside the device can support logic functions requiring between 0 and 16 p-terms. P-terms allocated away do not affect that macrocell's output structure. The input to the macrocell can be tied to VCC or GND, even when all p-terms have been allocated away. Thus the register and all control signals are still available for use if needed.

Figure 6 shows adjacent macrocells in the 5AC324. Table 1 shows the previous and next macrocells for each macrocell in the device, along with the corresponding allocation ring. P-term allocation is implemented automatically in the development software and is transparent to the user. Users can still use explicit pin assignment, but should assign pins in a way that does not conflict with p-term allocation.

Software support allows the control signals on macrocells to be used to implement simple logic functions even when all the input p-terms have been allocated to adjacent macrocells.

DUAL-FEEDBACK/BURIED LOGIC

Macrocell output can be fed back to the logic array on either one of the two feedback paths. If the pin feedback is used (connected after the output buffer), bidirectional I/O can be implemented. If the internal feedback path is used to implement a buried register or buried logic function, the pin feedback is still available for use as an input. The availability of dual feedbacks on the 5AC324 enhances resource efficiency over single feedback devices.

AUTOMATIC STAND-BY MODE

The 5AC324 contains a programmable bit, the Turbo Bit, that optimizes operation for speed or for power savings. When the Turbo Bit is programmed (TURBO = ON), the device is optimized for maximum

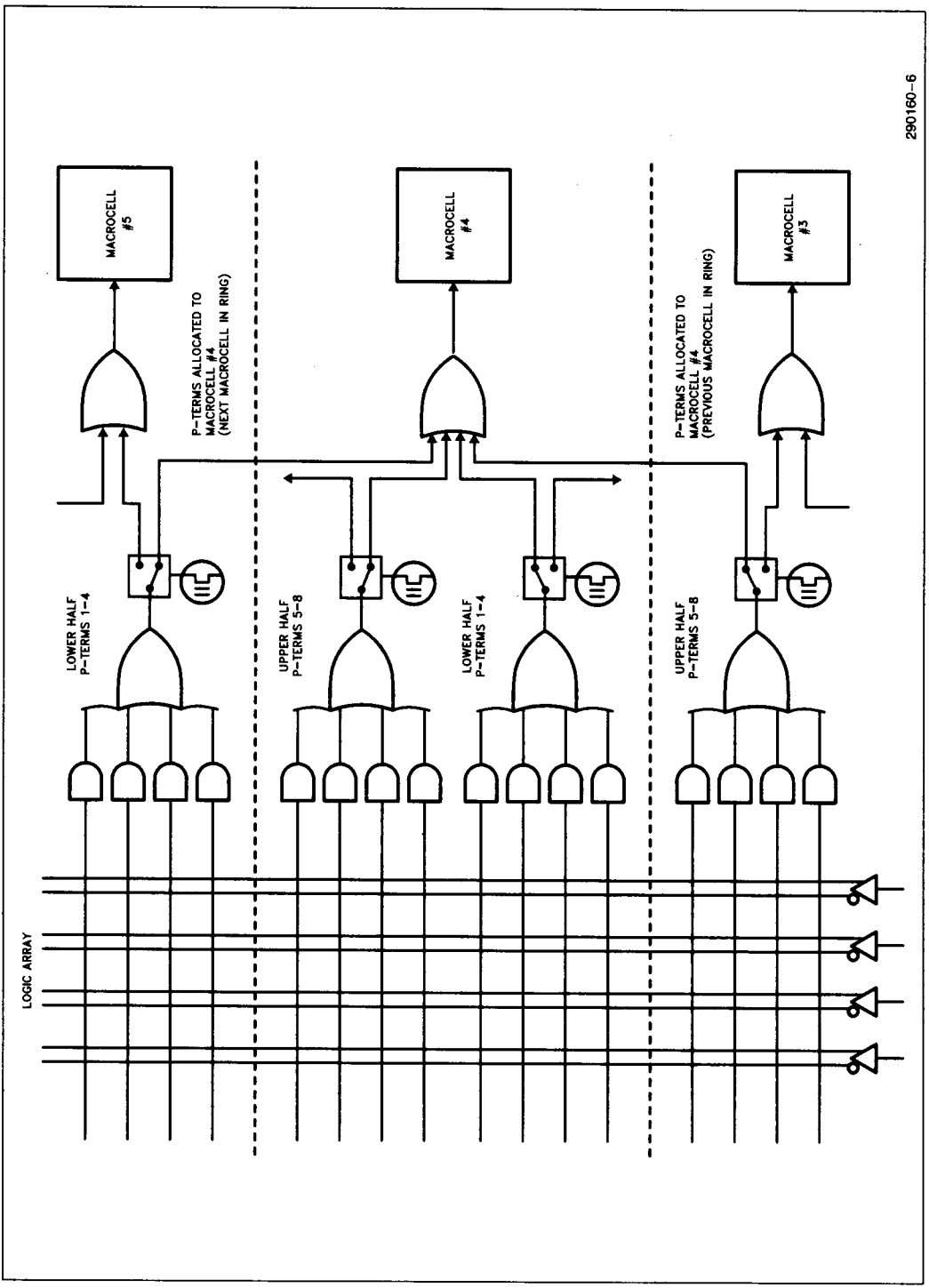


Figure 5. P-Term Allocation Example (8 + 4 + 4)

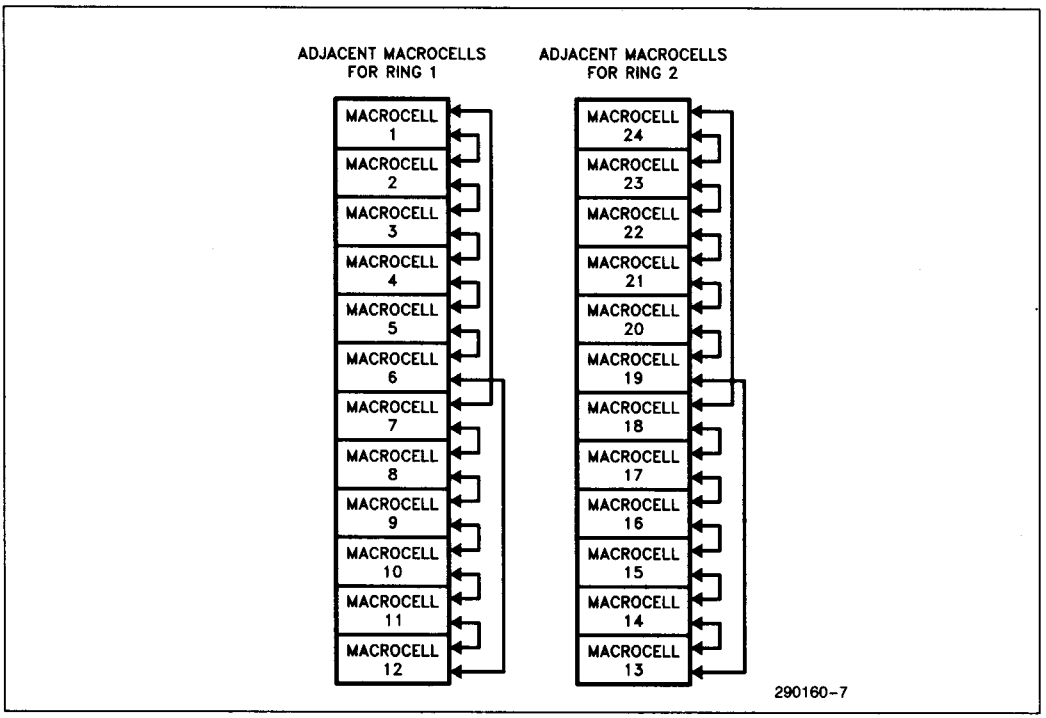


Figure 6. 5AC324 Adjacent Macrocell

Table 1. Product Term Allocation Rings

RING 1			RING 2		
Current Macrocell	**Next Macrocell**	**Previous Macrocell**	**Current Macrocell**	**Next Macrocell**	**Previous Macrocell**
1	7	2	13	19	14
2	1	3	14	13	15
3	2	4	15	14	16
4	3	5	16	15	17
5	4	6	17	16	18
6	5	12	18	17	24
7	8	1	19	20	13
8	9	7	20	21	19
9	10	8	21	22	20
10	11	9	22	23	21
11	12	10	23	24	22
12	6	11	24	18	23

speed. When the Turbo Bit is not programmed (TURBO = OFF), the device is optimized for power savings by entering standby mode during periods of inactivity.

Figure 7 shows the device entering standby mode approximately 100 ns after the last input or I/O transition. When the next input or I/O transition is detected, the device returns to active mode. Wakeup time adds an additional 20 ns to the propagation delay through the device as measured from the first transition. No delay will occur if an output is dependent on more than one input and the last of the inputs changes after the device has returned to active mode.

After erasure, the Turbo Bit is unprogrammed (OFF); automatic standby mode is enabled. When the Turbo Bit is programmed (ON), the device never enters standby mode.

POWER-ON CHARACTERISTICS

On V_{CC} power-up, the 5AC324 registers are reset to a logic low. Input latch/register output (to the logic array) are also set to a logic low. 5AC324 inputs and outputs begin responding approximately 20 μS after V_{CC} power-up or after a power-loss/power-up sequence. After power-up, macrocells can be preset to a logic high via the PRESET control signal for each macrocell.

ERASED STATE CONFIGURATION

After erasure and prior to programming, all macrocells are configured as combinatorial outputs with output buffers three-stated. Inputs are configured as synchronous registers.

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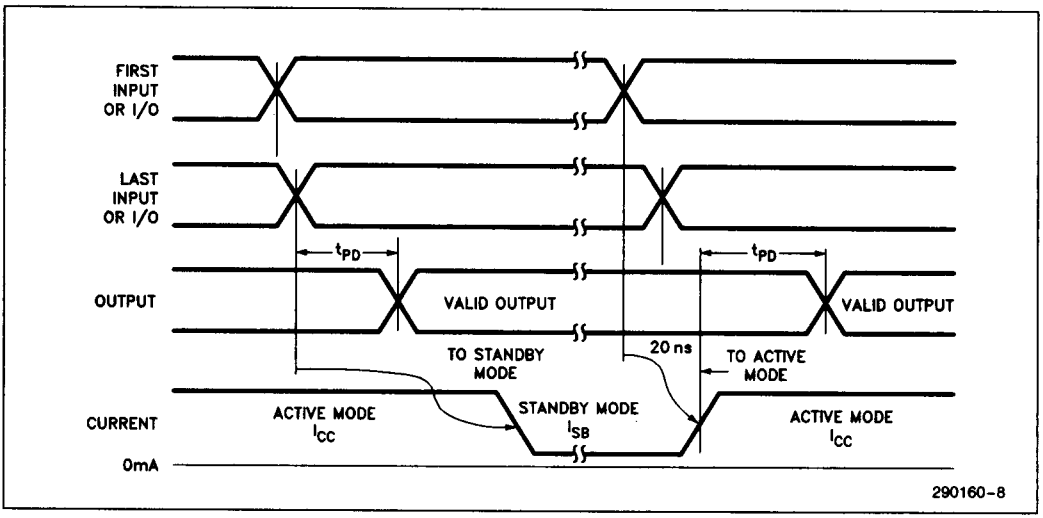


Figure 7. 5AC324 Standby and Active Mode Transitions

ERASURE CHARACTERISTICS

Erasure time for the 5AC324 is 1 hour at 12,000 $\mu W/cm^2$ with a 2537Å UV lamp.

Erasure characteristics of the device are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000Å. It should be noted that sunlight and certain types of flourescent lamps have wavelengths in the 3000Å-4000Å range. Data shows that constant exposure to room level flourescent lighting could erase the typical 5AC324 in approximately six years, while it would take approximately two weeks to erase the device when exposed to direct sunlight. If the device is to be exposed to these lighting conditions for extended periods of time, conductive opaque labels should be placed over the device window to prevent unintentional erasure.

The recommended erasure procedure for the 5AC324 is exposure to shortwave ultraviolet light with a wavelength of 2537Å. The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of forty (40) $Wsec/cm^2$. The erasure time with this dosage is approximately 1 hour using an ultraviolet lamp with a 12,000 $\mu W/cm^2$ power rating. The device should be placed within 1 inch of the lamp tubes during exposure. The maximum integrated dose the 5AC324 can be exposed to without damage is 7258 $Wsec/cm^2$ (1 week at 12,000 $\mu W/cm^2$). Exposure to high intensity UV light for longer periods may cause permanent damage to the device.

Intelligent Programming Algorithm

The 5AC324 supports the Intelligent Programming Algorithm, which rapidly programs Intel PLDs, while maintaining a high degree of reliability. It is particularly suited for production programming environments. This method ensures reliability as the incremental programming margin of each bit has been verified during programming. Programming voltage and waveform specifications are available by request from Intel to support programming the device.

LATCH-UP IMMUNITY

All of the input, I/O, and clock pins of the device have been designed to resist latch-up which is inherent in inferior CMOS structures. The 5AC324 is designed with Intel's proprietary 1-micron CMOS EPROM process. Thus, each of the pins will not experience latch-up with currents up to ± 100 mA and voltages ranging from $-0.5V$ to $(V_{CC} + 0.5V)$. The programming pin is designed to resist latch-up to the 13.5V maximum device limit.

DESIGN RECOMMENDATIONS

For proper operation, it is recommended that all input and output pins be constrained to the voltage range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$. All unused inputs and I/Os should be tied high or low to minimize power consumption (do not leave them floating). A power supply decoupling capacitor of at least $0.2\mu F$ must be connected directly between each V_{CC} and GND pin.

As with all CMOS devices, ESD handling procedures should be used with the 5AC324 to prevent damage to the device during programming, assembly, and test.

FUNCTIONAL TESTING

Since the logical operation of the 5AC324 is controlled by EPROM elements, the device is completely testable during the manufacturing process. Each programmable EPROM bit controlling the internal logic is tested using application independent test patterns. EPROM cells in the device are 100% tested for programming and erasure. After testing, the devices are erased before shipments to the customers. No post-programming tests of the EPROM array are required.

The testability and reliability of EPROM-based programmable logic devices is an important feature over similar devices based on fuse technology. Fuse-based programmable logic devices require a user to perform post-programming tests to insure device functionality. During the manufacturing process, tests on fuse-based parts can only be performed in very restricted ways in order to avoid preprogramming the array.

ADF PRIMITIVES SUPPORTED

The following ADF primitives are supported by this device:

INP	NOTF
LINP	JOJF
RINP	JONF
CONF	SONF
COCF	SOSF
COIF	TOIF
RONF	TONF
ROIF	TOTF
RORF	CLKB
NOCF	LINB
NORF	
NOJF	
NOSF	

SOFTWARE SUPPORT

Full logic compilation and functional simulation for the 5AC324 is supported by PLDshell Plus software. The GUPI 40D44J provides programming support on Intel programmers.

PLDshell Plus design software is Intel's user-friendly design tool for μPLD design. PLDshell Plus allows users to incorporate their preferred text editor, programming software, and additional design tools into an easy-to-use, menued design environment that includes Intel's PLDasm logic compiler and simulation software along with disassembly, conversion, and translation utilities. The PLDasm compiler and simulator software accepts industry-standard PDS source files that express designs as Boolean equations, truth tables, or state machines. On-line help, datasheet briefs, technical notes, and error message information, along with waveform viewing/printing capability make the design task as easy as possible. PLDshell Plus software is available from Intel Literature channels or from your local Intel sales representative.

Tools that support schematic capture and timing simulation for the 5AC324 are available. Please refer to the "Development Tools" section of the Programmable Logic handbook.

The 5AC324 is also supported by third-party logic compilers such as ABEL†, CUPL†, PLDesigner†, Log/IC, etc. Programming support is provided by third-party programmer companies such as Data I/O, Logical Devices, STAG, etc. Please refer to the "Third-Party Support" lists in the *Programmable Logic* handbook for complete information and vendor contacts.

ORDERING INFORMATION

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Order Code	Package	Operating Range
25	17.8	66	N5AC324-25	PLCC	Commercial
			P5AC324-25	PDIP	
			D5AC324-25	*CERDIP	
30	20	50	N5AC324-30	PLCC	Commercial
			P5AC324-30	PDIP	
			D5AC324-30	*CERDIP	
30	20	50	TN5AC324-30	PLCC	Industrial

*Windowed package allows UV erase.

†ABEL is a trademark of Data I/O Corporation. CUPL is a trademark of Logical Devices, Inc. PLDesigner is a trademark of MINC, Inc. Log/IC is a trademark of ISDATA, Inc.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{CC})[1] ..... −2.0V to +7.0V

Programming Supply Voltage (V_{PP})[1] ..... −2.0V to +13.5V

D.C. Input Voltage (V_I)[1,2] .... −0.5V to V_{CC} +0.5V

Storage Temperature (T_{stg}) ..... −65°C to +150°C

Ambient Temperature (T_{amb})[3] ... −10°C to +85°C

NOTES:
1. Voltage with respect to GND.
2. Minimum D.C. input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7.0V less than 20 ns under no load conditions.
3. Under bias. Extended Temperature versions are also available.

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	+70	°C
t_R	Input Rise Time		500	ns
t_F	Input Fall Time		500	ns

D.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

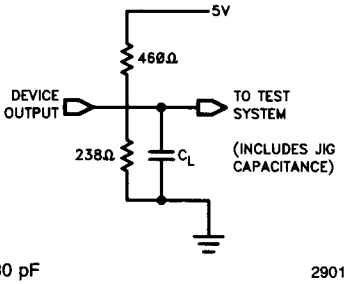
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}[4]	High Level Input Voltage	2.0		V_{CC} +0.3	V	
V_{IL}[4]	Low Level Input Voltage	−0.3		0.8		
V_{OH}[5]	High Level Output Voltage	2.4			V	I_O = −4.0 mA D.C., V_{CC} = min.
V_{OL}	Low Level Output Voltage			0.45	V	I_O = 8.0 mA D.C., V_{CC} = min.
I_I	Input Leakage Current			±10	μA	V_{CC} = max., GND < V_{IN} < V_{CC}
I_{OZ}	Output Leakage Current			±10	μA	V_{CC} = max., GND < V_{OUT} < V_{CC}
I_{SC}[6]	Output Short Circuit Current	−30		−90	mA	V_{CC} = max., V_{OUT} = 0.5V

D.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%) (Continued)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SB}[7]	Standby Current		150	500	μA	V_{CC} = max., V_{IN} = V_{CC} or GND, Standby Mode
I_{CC}	Power Supply Current (See I_{CC} vs Freq. Graph)		20		mA	V_{CC} = max., V_{IN} = V_{CC} or GND, No Load, f_{IN} = 1 MHz, Active Mode (Turbo = Off), Device Prog. as Two 12-Bit Counters

NOTES:
4. Absolute values with respect to device GND; all over and undershoots due to system or tester noise are included.
5. I_O at CMOS levels (3.84V) = −2 mA.
6. Not more than 1 output should be tested at a time. Duration of that test should not exceed 1 second.
7. With Turbo Bit Off, device automatically enters standby mode approximately 100 ns after last input transition.

A.C. TESTING LOAD CIRCUIT



C_L = 30 pF

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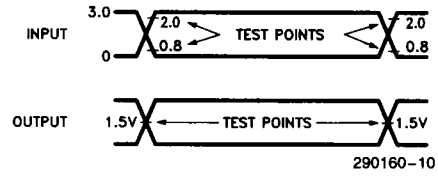
A.C. TESTING INPUT, OUTPUT WAVEFORM



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A.C. Testing: Inputs are driven at 3.0V for a Logic "1" and 0V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0" on inputs. Outputs are measured at a 1.5V point. Device input rise and fall times < 6 ns.

CAPACITANCE

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
C_{IN}	Input Capacitance			8	pF	V_{IN} = 0V, f = 1.0 MHz
C_{OUT}	I/O Capacitance			15	pF	V_{OUT} = 0V, f = 1.0 MHz
C_{CLK}	Clock Pin Capacitance			15	pF	V_{IN} = 0V, f = 1.0 MHz
C_{VPP}	V_{PP} Pin (LIN3)			25	pF	V_{IN} = 0V, f = 1.0 MHz

COMBINATORIAL MODE A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%, Turbo Bit On)[8]

Symbol	Parameter	5AC324-25			5AC324-30			5AC324-35			Non-Turbo[9] Mode	Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PD}	Input or I/O to Output Valid		20	25		25	30		30	35	+20	ns
t_{PZX}[10]	Input or I/O to Output Enable		20	25		25	30		30	35	+20	ns
t_{PXZ}[10]	Input or I/O to Output Disable		20	25		25	30		30	35	+20	ns
t_{CLR}	Asynch. Reset to Q Reset		20	25		25	30		30	35	+20	ns
t_{SET}	Asynch. Set to Q Set		20	25		25	30		30	35	+20	ns

NOTES:
8. Typical values are at T_A = +25°C, V_{CC} = 5V, Active Mode.
9. If device is operated with Turbo bit Off (Non-Turbo Mode) and the device is inactive for approx. 100 ns, increase time by amount shown.
10. t_{PZX} and t_{PXZ} measured at ±0.5V from steady-state voltage as driven by spec. output load. t_{PXZ} measured with C_L = 5 pF.

SYNCHRONOUS CLOCK MODE (MACROCELLS) A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%, Turbo Bit On)[8]

Symbol	Parameter	5AC324-25			5AC324-30			5AC324-35			Non-Turbo[9] Mode	Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Maximum Frequency (Pipelined) ($1/t_{CW}$)—No Feedback		80	66		66	50		50	40		MHz
f_{CNT1}	Maximum Frequency ($1/t_{SU} + t_{CO}$) —External Feedback		40	33		33.3	25		27	21.2		MHz
f_{CNT2}	Maximum Frequency ($1/t_{CNT}$) —Internal Feedback		40	33.3		33.3	28.5		28.5	25		MHz
t_{SU1}	Input Setup Time to CLK ↑	12.5	10		20	15		25	20		+20	ns
t_{SU2}	I/O Setup Time to CLK ↑	12	10		20	15		25	20		+20	ns
t_H	Input or I/O Hold Time from CLK ↑	0			0			0				ns
t_{CO}	CLK ↑ to Output Valid		15	17.8		15	20		17	22		ns
t_{CNT}	Register Output Feedback to Register Input— Internal Path		25	30		30	35		35	40	+20	ns
t_{CH}	Clock High Time	7			9			11				ns
t_{CL}	Clock Low Time	7			9			11				ns
t_{CW}	Minimum Clock Period	15			20			25				ns

SYNCHRONOUS CLOCK MODE (INPUT STRUCTURE) A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%, Turbo Bit On)[8]

Symbol	Parameter	5AC324-25			5AC324-30			5AC324-35			Non-Turbo[9] Mode	Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{MAXI}	Maximum Frequency ($1/t_{CWI}$)		80	66		60	50		50	40		MHz
t_{SUIR}	Input Register Setup Time Before ILE/ICLK ↓	1			2.5			5				ns
t_{ESUI}[11]	Input Latch Setup Time Before ILE ↑	1			2.5			5				ns
t_{COI}	ICLK ↓ to Comb. Output		25	30		30	35		35	40	+20	ns
t_{EOI}	ILE ↑ to Comb. Output		25	30		30	35		35	40	+20	ns
t_{HI}	Input Hold after ICLK ↓	8			9			10				ns
t_{EHI}	Input Hold after ILE ↓	7			8			9				ns
t_{CHI}	ILE/ICLK High Time	7			9			11				ns
t_{CLI}	ILE/ICLK Low Time	7			9			11				ns
t_{CWI}	Minimum Input Clock Period	15			20			25				ns

ASYNCHRONOUS CLOCK MODE (MACROCELLS) A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%, Turbo Bit On)[8]

Symbol	Parameter	5AC324-25			5AC324-30			5AC324-35			Non-Turbo[9] Mode	Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{AMAX}	Max. Frequency (Pipelined) ($1/t_{ACW}$)—No Feedback		80	66		60	50		50	40		MHz
f_{ACNT_1}	Max. Frequency ($1/t_{ASU} + t_{ACO}$) External Feedback		32.2	27.7		27	23.8		22.2	20		MHz
f_{ACNT_2}	Max. Frequency ($1/t_{ACNT}$) Internal Feedback		40	33.3		33.3	28.5		28.5	25		MHz
t_{ASU1}	Input Setup Time to Asynch. CLK	11			12			15			+20	ns
t_{ASU2}	I/O Setup Time to Asynch. CLK	11			12			15			+20	ns
t_{AH}	Input or I/O Hold Time from Asynch. CLK	3	0		4	0		5	0			ns
t_{ACO}	Asynch. CLK to Output Valid		20	25		25	30		30	35	+20	ns
t_{ACNT}	Asynch. Output Feedback to Register Input - Internal Path		25	30		30	35		35	40	+20	ns
t_{ACH}	Asynch. CLK High Time	7			9			11			+20	ns
t_{ACL}	Asynch. CLK Low Time	7			9			11			+20	ns
t_{ACW}	Asynch. CLK Period	15			20			25			+20	ns

ASYNCHRONOUS CLOCK MODE (INPUT STRUCTURE) A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%, Turbo Bit On)[8]

Symbol	Parameter	5AC324-25			5AC324-30			5AC324-35			Non-Turbo[9] Mode	Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{AMAXI}	Maximum Frequency Input Register ($1/t_{ACWI}$)		80	66		60	50		50	40		MHz
t_{ASUIR}	Input Register Setup Time Before Asynch. ICLK	−5			−5			−5				ns
t_{AESUI}[11]	Input Latch Setup Time Before Asynch. ILE	−5			−5			−5				ns
t_{ACOI}	Asynch. ICLK to Comb. Output		25	30		30	35		45	50	+20	ns
t_{AEOI}	Asynch. ILE to Comb. Output		25	30		30	45		45	50	+20	ns
t_{AHI}	Input Hold after Asynch. ICLK	15			18			20				ns
t_{AEHI}	Input Hold after Asynch. ILE	14			17			19				ns
t_{ACHI}	Asynch. ILE/ICLK High Time	7			9			11			+20	ns
t_{ACLI}	Asynch. ILE/ICLK Low Time	7			9			11			+20	ns
t_{ACWI}	Minimum Input Clock Period	15			20			25			+20	ns

NOTE:
11. This specification must be met to guarantee t_{EOI}. When ILE goes high before data is valid, use t_{PD} instead of t_{EOI}.

INPUT-CLOCK-TO-MACROCELL-CLOCK A.C. CHARACTERISTICS

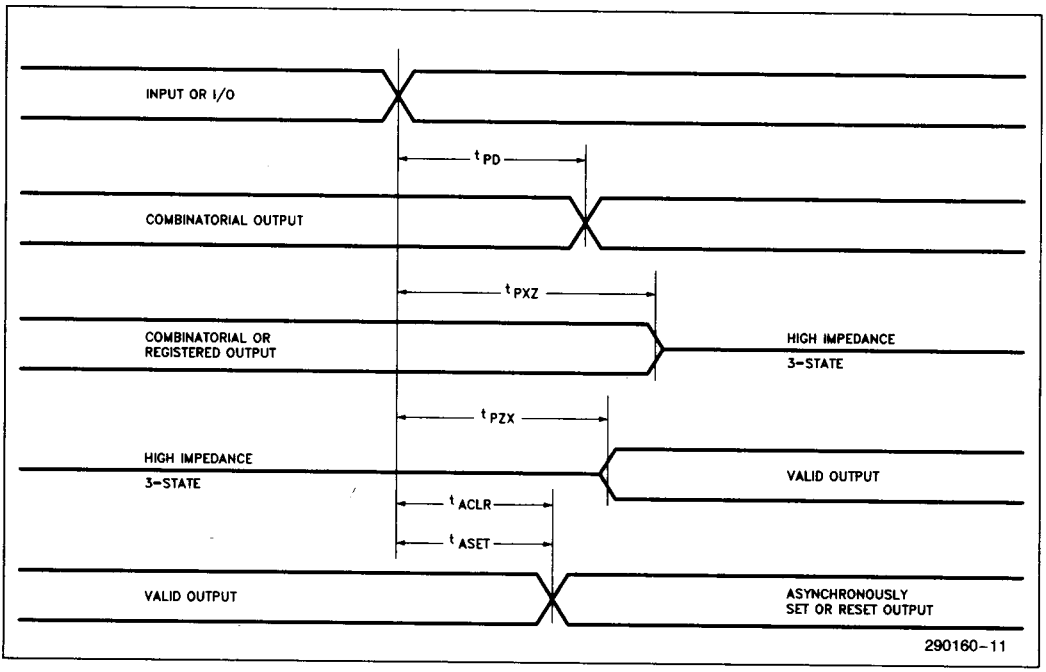
(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%, Turbo Bit On)[8]

Symbol	Parameter	5AC324-25			5AC324-30			5AC324-35			Non-Turbo[9] Mode	Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{C1C2}[12]	Synchronous ILE/ICLK to Synchronous Macrocell CLK	20			25			30			+20	ns
	Synchronous ILE/ICLK to Asynchronous Macrocell CLK	12.5			15			18			+20	ns
	Asynchronous ILE/ICLK to Synchronous Macrocell CLK	40			45			50			+20	ns
	Asynchronous ILE/CLK to Asynchronous Macrocell CLK	20			25			30			+20	ns

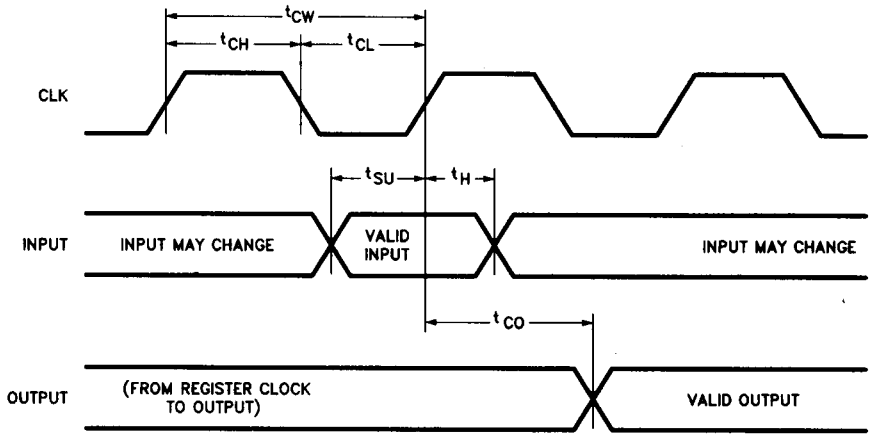
NOTE:
12. Times for SETUP, HOLD, and OUTPUT VALID are shown in previous tables.

SWITCHING WAVEFORMS

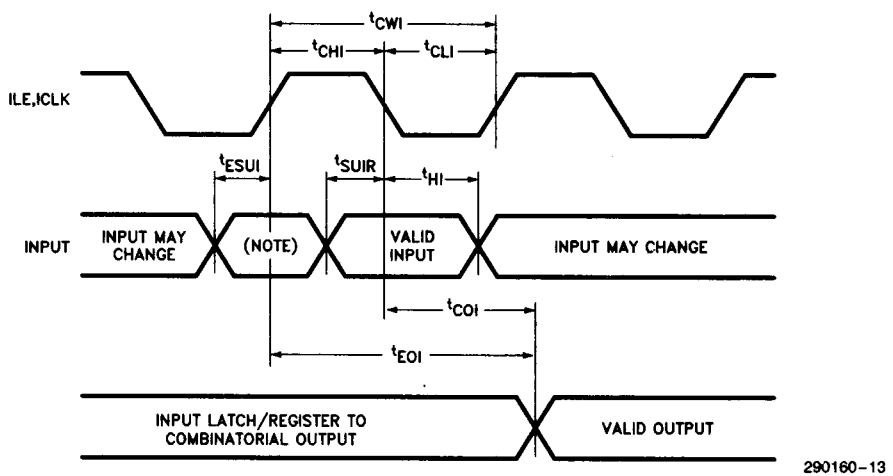
COMBINATORIAL MODE



SYNCHRONOUS CLOCK MODE (MACROCELLS)

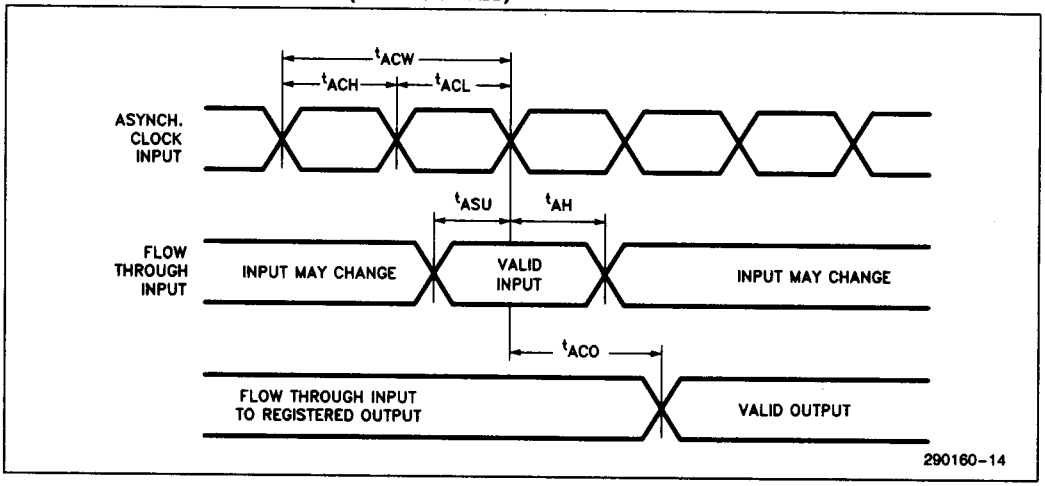


SYNCHRONOUS CLOCK MODE (INPUT STRUCTURE)

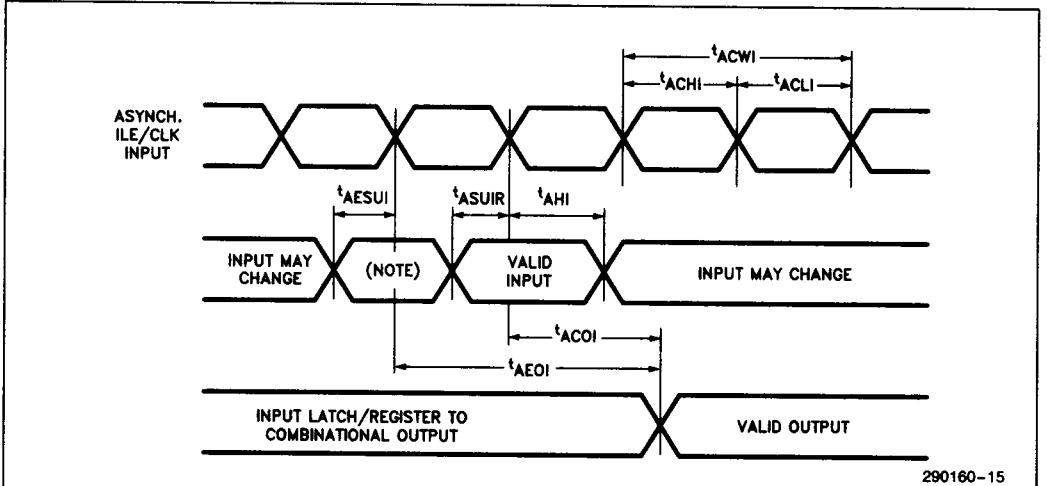


NOTE:
When ILE goes high before data is valid, use t_{PD} instead of t_{EOI}.

ASYNCHRONOUS CLOCK MODE (MACROCELLS)

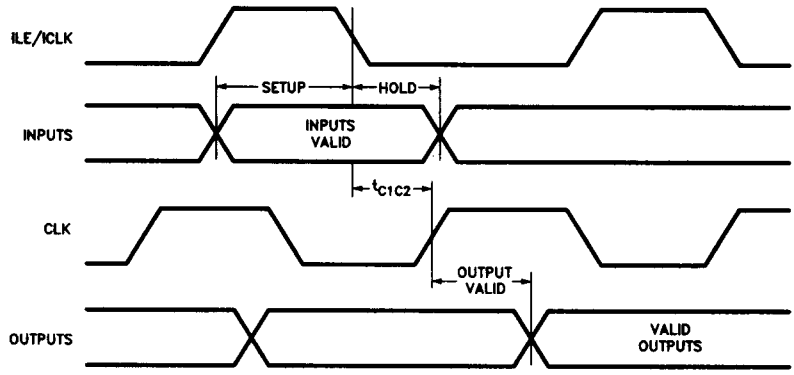


ASYNCHRONOUS CLOCK MODE (INPUT STRUCTURE)



NOTE:
When ILE goes high before data is valid, use t_{PD} instead of t_{AEOI}.

INPUT-CLOCK-TO-MACROCELL CLOCK TIMING (CLOCKED PIPELINED DATA)

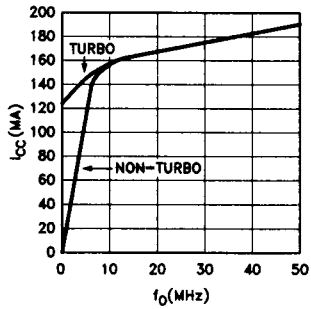


290160-16

CLOCK, SETUP, HOLD, and OUTPUT VALID times are dependent on synchronous/asynchronous clocking and are listed in the specification tables.

2

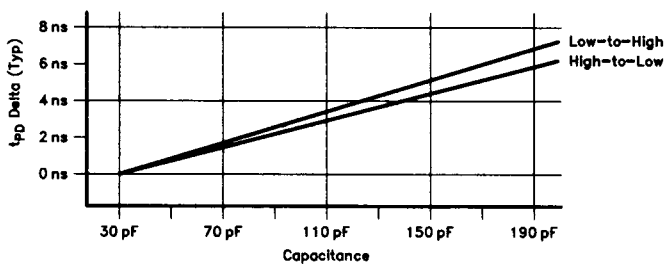
5AC324 I_{CC} vs. Frequency



290160-17

Conditions: T_A = 25°C
V_{CC} = 5.0V

5AC324 t_{PD} Derating vs. Capacitive Loading



290160-18

Conditions: T_A = 25°C
V_{CC} = 5.0V