LXT9785/LXT9785E

Advanced 10/100 8-Port Transceivers

Datasheet

The LXT9785 and LXT9785E are 8-port Fast Ethernet PHY Transceivers that support IEEE 802.3 physical layer applications at 10 Mbps and 100 Mbps. These devices provide both Serial/ Source Synchronous Serial Media Independent Interfaces (SMII/SS-SMII) and Reduced Media Independent Interface (RMII) for switching and other independent port applications. The LXT9785 and LXT9785E are identical except for the IP telephony features included in the LXT9785E transceiver. The LXT9785E is an enhanced version of the LXT9785 that detects Data Terminal Equipment (DTE) capable of being powered remotely from the switch over a Category 5 cable. The system can use the information collected by the LXT97985E to apply power if the DTE at the far end requires power over the cable, such as an IP telephone.

All network ports provide a combination twisted-pair (TP) or pseudo-ECL (PECL) interface for both 10 Mbps or 100 Mbps (10BASE-T and 100BASE-TX) Ethernet over twisted-pair, or 100 Mbps (100BASE-FX) Ethernet over fiber-optic media.

The LXT9785/9785E provides three discrete LED driver outputs for each port. The devices support both half-duplex and full-duplex operation at 10 Mbps and 100 Mbps and require only a single 2.5V power supply.

Applications

- Enterprise switches
- IP telephony switches
- Storage Area Networks
- Multi-port Network Interface Cards (NICs)

Product Features

- Eight IEEE 802.3-compliant 10BASE-T or 100BASE-TX ports with integrated filters.
- 100BASE-FX fiber-optic capability on all ports.
- 2.5V operation.
- Low power consumption; 250 mW per port typical.
- Multiple RMII or SMII/SS-SMII ports for independent PHY port operation.
- Auto MDIX crossover capabilities.
- Proprietary Optimal Signal Processing™ architecture improves SNR by 3 dB over ideal analog filters.
- Optimized for dual-high stacked RJ-45 applications.
- MDIO sectionalization into 2x4 or 1x8 configurations.
- Supports both auto-negotiation systems and legacy systems without auto-negotiation capability.
- Robust baseline wander correction.
- Configurable via MDIO port or external control pins.
- JTAG boundary scan.
- 208-pin PQFP: LXT9785HC, LXT9785EHC
- 241-ball BGA: LXT9785BC, LXT9785EBC
- DTE detection for remote powering applications (LXT9785E only).

As of January 15, 2001, this document replaces the Level One document known as *LXT9785/9785E Advanced 10/100 8-Port PHY Datasheet*.

Order Number: 249241-003
April 2001

Contents

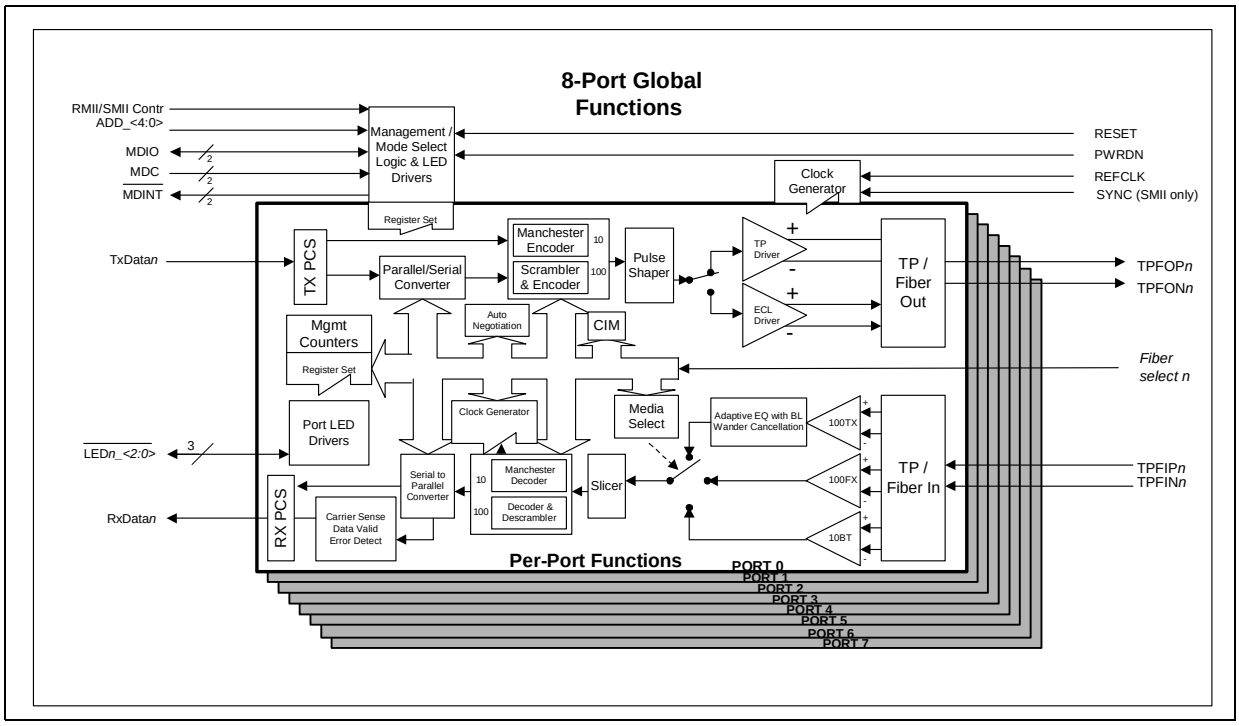
Figures

Tables

Revision History

Date	Revision	Page	Description
April 2001	003	1	Modified and added new language to front page.
		61	Reset: Modified language in first paragraph.
		85	Added new section on DTE discovery.
		93	Supported JTAG Instructions table: replaced long hit streams with hex.
		97	LED Circuit: Modified paragraph language.
		97	LED Circuit diagram: Modified diagram.
		99	Replaced Typical Fiber Interface diagram.
		102	Required Clock Characteristics table: Replaced SMII Input frequency and RMII Input frequency symbol with “f”.
		122	Auto-Negotiation and Fast Link Pulse Timing Parameters: FLP burst width under Typ = 2.
		126	Control Register table: Modified table and table notes.
		128	PHY Identification Register 2 (Address 3): Modified table.
		128	PHY Identifier Bit Mapping: Modified diagram.
		131	Auto-Negotiation Expansion: Modified table and table notes.
		133	Port Configuration Register table: Modified table and table notes.
		140	Trim Enable Register: Modified table (DTE Discovery).
		141	Modified Register Bit Map table.

Figure 1. LXT9785/9785E Block Diagram



1.0 Pin Assignments and Signal Descriptions

Figure 2. LXT9785/9785E RMII 208-Pin PQFP Assignments

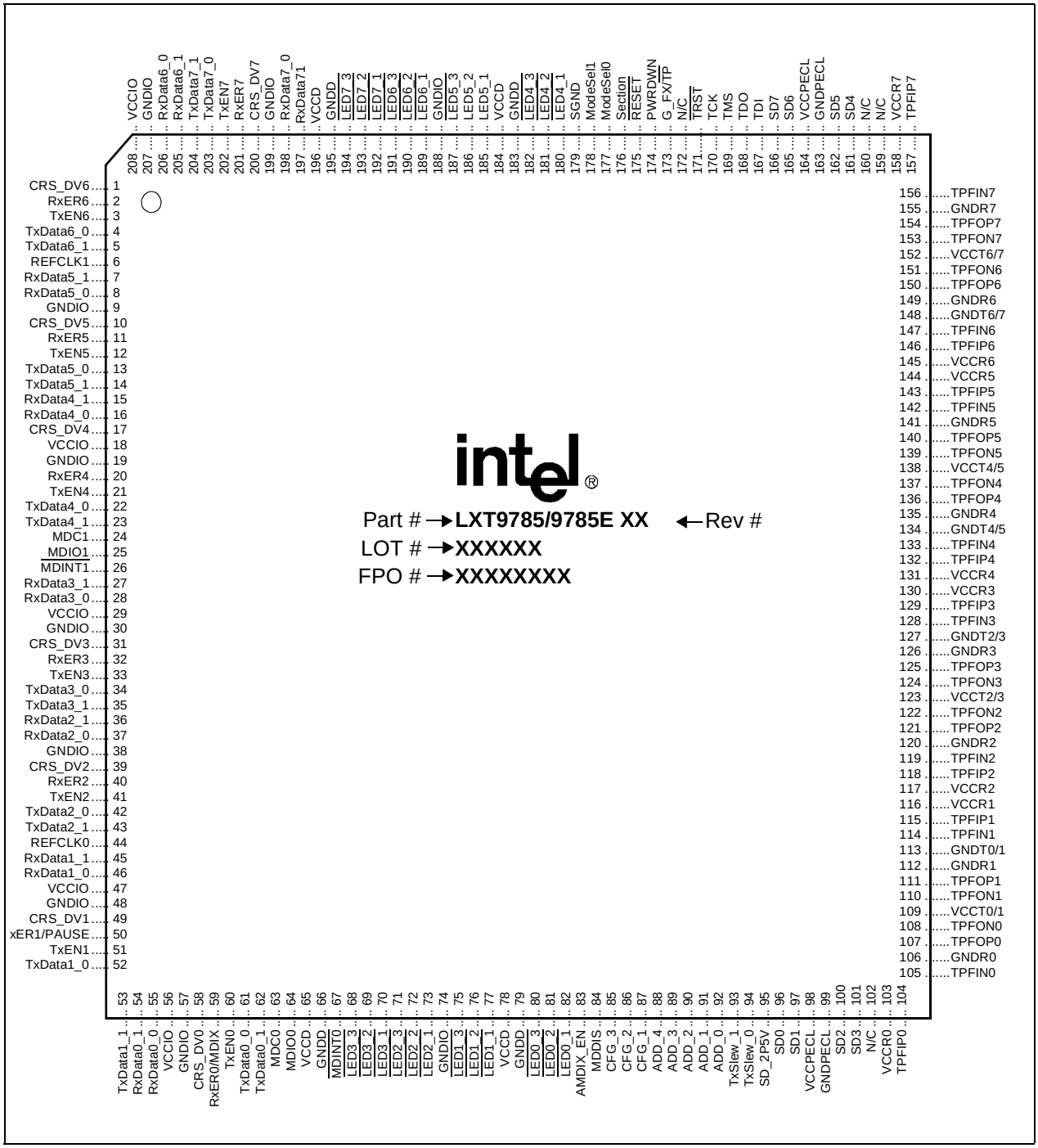


Figure 3. LXT9785/9785E SMII 208-Pin PQFP Assignments

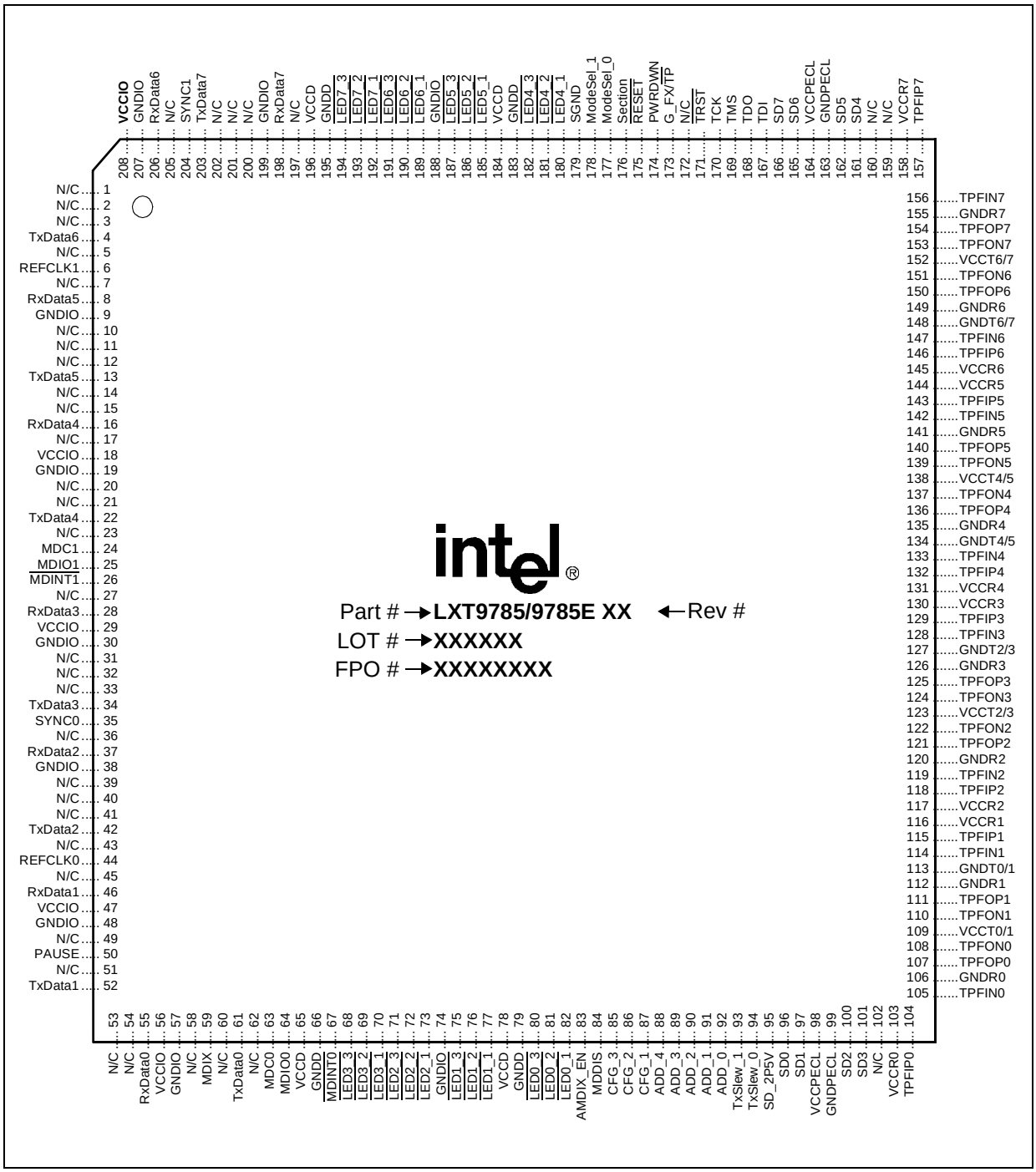


Figure 4. LXT9785/9785E SS-SMII 208-Pin PQFP Assignments

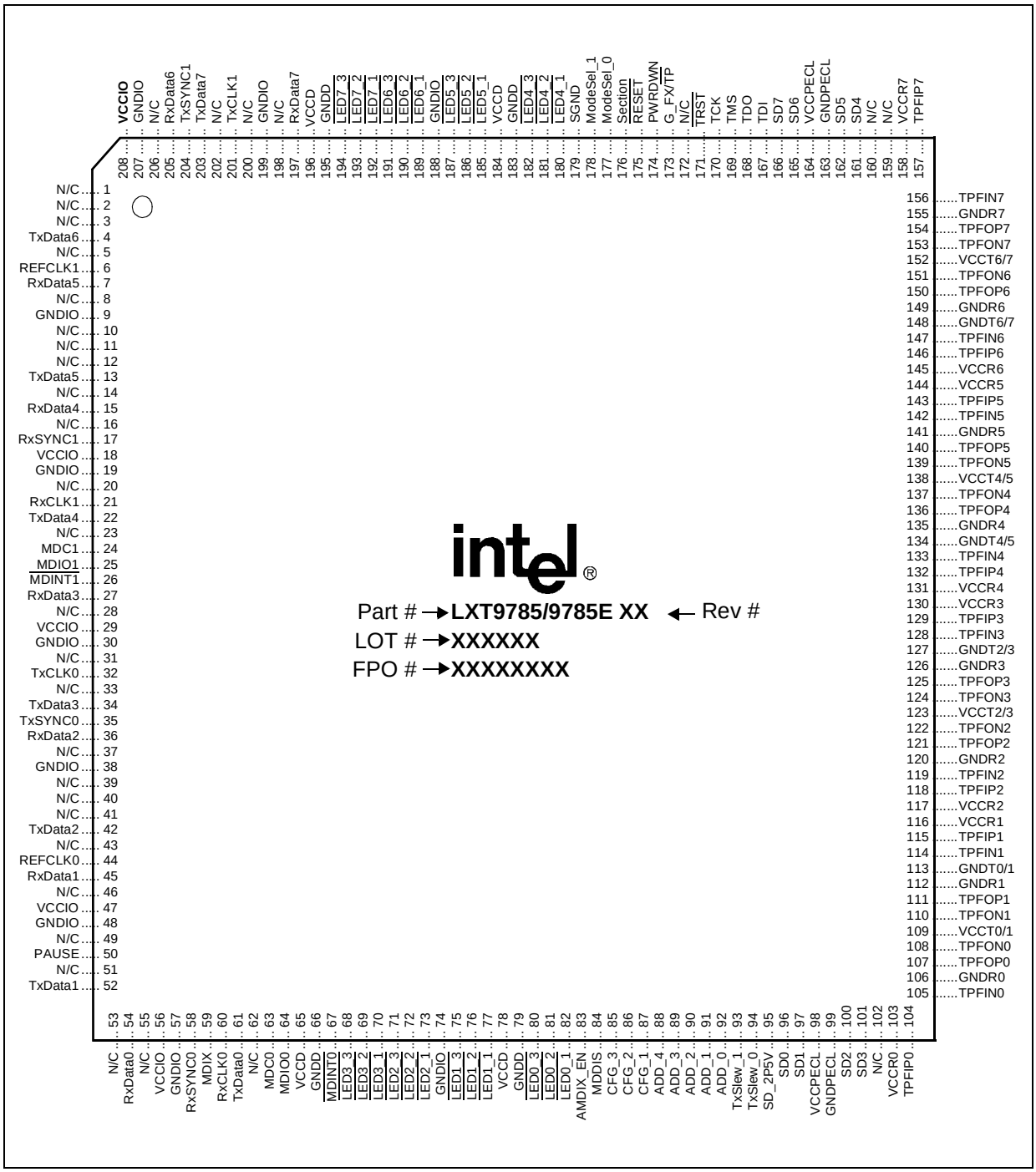


Figure 5. LXT9785/9785E RMII 241-Ball PBGA Assignments

RMII	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	GNDD	VCCIO	RxData1_0	TxData2_1	CRS_DV2	TxData3_1	TxEN3	VCCIO	GNDD	MDIO1	TxData4_0	RxER4	RxData4_0	TxEN5	RxER5	TxData6_1	RxER6	A
B	RxData0_1	TxEN1	GNDD	RxData1_1	TxData2_0	RxData2_0	GNDD	CRS_DV3	RxData3_1	MDC1	TxEN4	CRS_DV4	TxData5_0	RxData5_0	RxData5_1	CRS_DV6	RXD6_1	B
C	VCCIO	RXD0_0	TXD1_0	CRS_DV1	GNDD	TxEN2	RxData2_1	RxER3	$\overline{\text{MDINT1}}$	TxData4_1	VCCIO	RxData4_1	GNDD	TxEN6	RxData6_0	TxData7_1	GNDD	C
D	GNDD	RxER0/MDIX	GNDD	TxData1_1	RxER1/PAUSE	GNDD	RxER2	TxData3_0	RxData3_0	GNDD	TxData5_1	CRS_DV5	TxData6_0	VCCIO	GNDD	TxEN7	RxER7	D
E	MDC0	TxData0_0	TxEN0	CRS_DV0	GNDD	REFCLK0	GNDD		GNDD		GNDD	REFCLK1	GNDD	TXD7_0	CRS_DV7	RxData7_0	GNDD	E
F	$\overline{\text{MDINT0}}$	$\overline{\text{LED3_1}}$	MDIO0	TxData0_1	VCCD								GNDD	RXD7_1	N/C	$\overline{\text{LED7_3}}$	$\overline{\text{LED7_2}}$	F
G	$\overline{\text{LED2_3}}$	N/C	$\overline{\text{LED3_2}}$	$\overline{\text{LED3_3}}$	N/C								VCCD	N/C	$\overline{\text{LED7_1}}$	N/C	$\overline{\text{LED6_3}}$	G
H	$\overline{\text{LED1_3}}$	$\overline{\text{LED2_1}}$	$\overline{\text{LED2_2}}$	N/C				GNDD	GNDD	GNDD				N/C	$\overline{\text{LED6_1}}$	$\overline{\text{LED6_2}}$	$\overline{\text{LED5_3}}$	H
J	$\overline{\text{LED0_3}}$	N/C	$\overline{\text{LED1_2}}$	$\overline{\text{LED1_1}}$	VCCD			GNDD	GNDD	GNDD			N/C	VCCD	$\overline{\text{LED5_1}}$	$\overline{\text{LED5_2}}$	$\overline{\text{LED4_3}}$	J
K	AMDIX_EN	$\overline{\text{LED0_2}}$	$\overline{\text{LED0_1}}$	N/C				GNDD	GNDD	GNDD				SGND	N/C	$\overline{\text{LED4_1}}$	$\overline{\text{LED4_2}}$	K
L	MDDIS	CFG_3	CFG_2	ADD_4	VCC PECL								VCC PECL	PWR DWN	SEC TION	MODE SEL_0	MODE SEL_1	L
M	CFG_1	ADD_3	ADD_2	TxSLEW_1	GND PECL								GND PECL	G_FX/$\overline{\text{TP}}$	$\overline{\text{RESET}}$	TCK	$\overline{\text{TRST}}$	M
N	ADD_1	ADD_0	TxSLEW_0	SD1	SD3	VCCT	VCCT		VCCT		VCCT	VCCT	VCCR	TDI	TDO	TMS	SD7	N
P	SD_2P5V	SD0	SD2	VCCR	GNDR	GNDR	VCCR	VCCR	VCCR	VCCR	VCCR	VCCR	GNDR	GNDT	SD4	SD5	SD6	P
R	GNDT	TPFIP(0)	GNDT	TPFON(1)	GNDT	TPFIP(2)	GNDR	TPFIN(3)	GNDR	TPFON(4)	GNDR	TPFIP(6)	GNDR	TPFOP(7)	GNDT	TPFIP(7)	GNDT	R
T	TPFIN(0)	TPFOP(0)	TPFOP(1)	TPFIN(1)	TPFIN(2)	TPFOP(2)	TPFON(3)	TPFIP(3)	TPFIP(4)	TPFOP(4)	TPFOP(5)	TPFIN(5)	TPFIN(6)	TPFOP(6)	TPFON(7)	TPFIN(7)	GNDT	T
U	TPFON(0)	GNDT	TPFIP(1)	GNDT	TPFON(2)	GNDT	TPFOP(3)	GNDR	TPFIN(4)	GNDT	TPFON(5)	GNDT	TPFIP(5)	GNDT	TPFON(6)	GNDT	GNDT	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Figure 6. LXT9785/9785E SMII 241-Ball PBGA Assignments

SMII	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	GNDD	VCCIO	RxData 1	N/C	N/C	SYNC0	N/C	VCCIO	GNDD	MDIO1	TxData 4	N/C	RxData 4	N/C	N/C	N/C	N/C	A
B	N/C	N/C	GNDD	N/C	TxData 2	RxData 2	GNDD	N/C	N/C	MDC1	N/C	N/C	TxData 5	RxData 5	N/C	N/C	N/C	B
C	VCCIO	RxData 0	TxData 1	N/C	GNDD	N/C	N/C	N/C	MDINT1	N/C	VCCIO	N/C	GNDD	N/C	RxData 6	SYNC1	GNDD	C
D	GNDD	MDIX	GNDD	N/C	PAUSE	GNDD	N/C	TxData 3	RxData 3	GNDD	N/C	N/C	TxData 6	VCCIO	GNDD	N/C	N/C	D
E	MDC0	TxData 0	N/C	N/C	GNDD	REF CLK0	GNDD		GNDD		GNDD	REF CLK1	GNDD	TxData 7	N/C	RxData 7	GNDD	E
F	$\overline{\text{MDINT0}}$	$\overline{\text{LED3\_1}}$	MDIO0	N/C	VCCD								GNDD	N/C	N/C	$\overline{\text{LED7\_3}}$	$\overline{\text{LED7\_2}}$	F
G	$\overline{\text{LED2\_3}}$	N/C	$\overline{\text{LED3\_2}}$	$\overline{\text{LED3\_3}}$	N/C								VCCD	N/C	$\overline{\text{LED7\_1}}$	N/C	$\overline{\text{LED6\_3}}$	G
H	$\overline{\text{LED1\_3}}$	$\overline{\text{LED2\_1}}$	$\overline{\text{LED2\_2}}$	N/C				GNDD	GNDD	GNDD				N/C	$\overline{\text{LED6\_1}}$	$\overline{\text{LED6\_2}}$	$\overline{\text{LED5\_3}}$	H
J	$\overline{\text{LED0\_3}}$	N/C	$\overline{\text{LED1\_2}}$	$\overline{\text{LED1\_1}}$	VCCD			GNDD	GNDD	GNDD			N/C	VCCD	$\overline{\text{LED5\_1}}$	$\overline{\text{LED5\_2}}$	$\overline{\text{LED4\_3}}$	J
K	AMDIX_EN	$\overline{\text{LED0\_2}}$	$\overline{\text{LED0\_1}}$	N/C				GNDD	GNDD	GNDD				SGND	N/C	$\overline{\text{LED4\_1}}$	$\overline{\text{LED4\_2}}$	K
L	MDDIS	CFG_3	CFG_2	ADD_4	VCC PECL								VCC PECL	PWR DWN	SECTION	MODE SEL_0	MODE SEL_1	L
M	CFG_1	ADD_3	ADD_2	TxSLEW_1	GND PECL								GND PECL	G_FX/$\overline{\text{TP}}$	$\overline{\text{RESET}}$	TCK	$\overline{\text{TRST}}$	M
N	ADD_1	ADD_0	TxSLEW_0	SD1	SD3	VCCT	VCCT		VCCT		VCCT	VCCT	VCCR	TDI	TDO	TMS	SD7	N
P	SD_2P5V	SD0	SD2	VCCR	GNDR	GNDR	VCCR	VCCR	VCCR	VCCR	VCCR	VCCR	GNDR	GNDT	SD4	SD5	SD6	P
R	GNDT	TPFIP (0)	GNDT	TPFON(1)	GNDT	TPFIP (2)	GNDR	TPFIN (3)	GNDR	TPFON(4)	GNDR	TPFIP (6)	GNDR	TPFOP(7)	GNDT	TPFIP (7)	GNDT	R
T	TPFIN(0)	TPFOP(0)	TPFOP(1)	TPFIN(1)	TPFIN(2)	TPFOP(2)	TPFON(3)	TPFIP (3)	TPFIP (4)	TPFOP(4)	TPFOP(5)	TPFIN (5)	TPFIN (6)	TPFOP(6)	TPFON(7)	TPFIN(7)	GNDT	T
U	TPFON(0)	GNDT	TPFIP (1)	GNDT	TPFON(2)	GNDT	TPFOP(3)	GNDR	TPFIN (4)	GNDT	TPFON(5)	GNDT	TPFIP (5)	GNDT	TPFON(6)	GNDT	GNDT	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Figure 7. LXT9785/9785E SS-SMII 241-Ball PBGA Assignments

SS-SMII	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	GNDD	VCCIO	N/C	N/C	N/C	TxSYNC0	N/C	VCCIO	GNDD	MDIO1	TxData4	N/C	N/C	N/C	N/C	N/C	N/C	A
B	RxData0	N/C	GNDD	RxData1	TxData2	N/C	GNDD	N/C	RxData3	MDC1	RxCLK1	RxSYNC1	TxData5	N/C	RxData5	N/C	RxData6	B
C	VCCIO	RxData0	TxData1	N/C	GNDD	N/C	RxData2	TxCLK0	MDINT1	N/C	VCCIO	RxData4	GNDD	N/C	N/C	TxSYNC1	GNDD	C
D	GNDD	MDIX	GNDD	N/C	PAUSE	GNDD	N/C	TxData3	N/C	GNDD	N/C	N/C	TxData6	VCCIO	GNDD	N/C	TxCLK1	D
E	MDC0	TXD0	RxCLK0	RxSYNC0	GNDD	REFCLK0	GNDD		GNDD		GNDD	REFCLK1	GNDD	TxData7	N/C	N/C	GNDD	E
F	$\overline{\text{MDINT0}}$	$\overline{\text{LED3\_1}}$	MDIO0	N/C	VCCD								GNDD	RxData7	N/C	$\overline{\text{LED7\_3}}$	$\overline{\text{LED7\_2}}$	F
G	$\overline{\text{LED2\_3}}$	N/C	$\overline{\text{LED3\_2}}$	$\overline{\text{LED3\_3}}$	N/C								VCCD	N/C	$\overline{\text{LED7\_1}}$	N/C	$\overline{\text{LED6\_3}}$	G
H	$\overline{\text{LED1\_3}}$	$\overline{\text{LED2\_1}}$	$\overline{\text{LED2\_2}}$	N/C				GNDD	GNDD	GNDD				N/C	$\overline{\text{LED6\_1}}$	$\overline{\text{LED6\_2}}$	$\overline{\text{LED5\_3}}$	H
J	$\overline{\text{LED0\_3}}$	N/C	$\overline{\text{LED1\_2}}$	$\overline{\text{LED1\_1}}$	VCCD			GNDD	GNDD	GNDD			N/C	VCCD	$\overline{\text{LED5\_1}}$	$\overline{\text{LED5\_2}}$	$\overline{\text{LED4\_3}}$	J
K	AMDIX_EN	$\overline{\text{LED0\_2}}$	$\overline{\text{LED0\_1}}$	N/C				GNDD	GNDD	GNDD				SGND	N/C	$\overline{\text{LED4\_1}}$	$\overline{\text{LED4\_2}}$	K
L	MDDIS	CFG_3	CFG_2	ADD_4	VCC PECL								VCC PECL	PWR DWN	SECTION	MODESEL_0	MODESEL_1	L
M	CFG_1	ADD_3	ADD_2	TxSLEW_1	GND PECL								GND PECL	G_FX/$\overline{\text{TP}}$	$\overline{\text{RESET}}$	TCK	$\overline{\text{TRST}}$	M
N	ADD_1	ADD_0	TxSLEW_0	SD1	SD3	VCCT	VCCT		VCCT		VCCT	VCCT	VCCR	TDI	TDO	TMS	SD7	N
P	SD_2P5V	SD0	SD2	VCCR	GNDR	GNDR	VCCR	VCCR	VCCR	VCCR	VCCR	VCCR	GNDR	GNDT	SD4	SD5	SD6	P
R	GNDT	TPFIP(0)	GNDT	TPFON(1)	GNDT	TPFIP(2)	GNDR	TPFIN(3)	GNDR	TPFON(4)	GNDR	TPFIP(6)	GNDR	TPFOP(7)	GNDT	TPFIP(7)	GNDT	R
T	TPFIN(0)	TPFOP(0)	TPFOP(1)	TPFIN(1)	TPFIN(2)	TPFOP(2)	TPFON(3)	TPFIP(3)	TPFIP(4)	TPFOP(4)	TPFOP(5)	TPFIN(5)	TPFIN(6)	TPFOP(6)	TPFON(7)	TPFIN(7)	GNDT	T
U	TPFON(0)	GNDT	TPFIP(1)	GNDT	TPFON(2)	GNDT	TPFOP(3)	GNDR	TPFIN(4)	GNDT	TPFON(5)	GNDT	TPFIP(5)	GNDT	TPFON(6)	GNDT	GNDT	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Table 1. RMII PQFP Pin List

Pin	Symbol	Type[1]	Reference for Full Description
1	CRS_DV6	O, TS, SL	Table 4 on page 39
2	RxER6	O, TS, SL, ID	Table 4 on page 39
3	TxEN6	I, ID	Table 4 on page 39
4	TxData6_0	I, ID	Table 4 on page 39
5	TxData6_1	I, ID	Table 4 on page 39
6	REFCLK1	I	Table 4 on page 39
7	RxData5_1	O, TS, ID	Table 4 on page 39
8	RxData5_0	O, TS	Table 4 on page 39
9	GNDIO	–	Table 14 on page 49
10	CRS_DV5	O, TS, SL	Table 4 on page 39
11	RxER5	O, TS, SL, ID	Table 4 on page 39
12	TxEN5	I, ID	Table 4 on page 39
13	TxData5_0	I, ID	Table 4 on page 39
14	TxData5_1	I, ID	Table 4 on page 39
15	RxData4_1	O, TS,ID	Table 4 on page 39
16	RxData4_0	O, TS	Table 4 on page 39
17	CRS_DV4	O, TS, SL	Table 4 on page 39
18	VCCIO	–	Table 14 on page 49
19	GNDIO	–	Table 14 on page 49
20	RxER4	O, TS, SL, ID	Table 4 on page 39
21	TxEN4	I, ID	Table 4 on page 39
22	TxData4_0	I, ID	Table 4 on page 39
23	TxData4_1	I, ID	Table 4 on page 39
24	MDC1	I, ST, ID	Table 8 on page 43
25	MDIO1	I/O, TS, SL, IP	Table 8 on page 43
26	$\overline{\text{MDINT1}}$	OD, TS, SL, IP	Table 8 on page 43
27	RxData3_1	O, TS, ID	Table 4 on page 39
28	RxData3_0	O, TS	Table 4 on page 39
29	VCCIO	–	Table 14 on page 49
30	GNDIO	–	Table 14 on page 49
31	CRS_DV3	O, TS, SL	Table 4 on page 39
32	RxER3	O, TS, SL, ID	Table 4 on page 39
33	TxEN3	I, ID	Table 4 on page 39

1. AI=Analog Input, AO=Analog Output, I=Input, O=Output, OD=Open Drain output, ST=Schmitt Triggered input, TS=Tri-State-able output, SL=Slew-rate Limited output, IP=Weak Internal Pull-up, ID=Weak Internal Pull-down

Table 1. RMII PQFP Pin List (Continued)

Pin	Symbol	Type[1]	Reference for Full Description
34	TxData3_0	I, ID	Table 4 on page 39
35	TxData3_1	I, ID	Table 4 on page 39
36	RxData2_1	O, TS, ID	Table 4 on page 39
37	RxData2_0	O, TS	Table 4 on page 39
38	GNDIO	–	Table 14 on page 49
39	CRS_DV2	O, TS, SL	Table 4 on page 39
40	RxER2	O, TS, SL, ID	Table 4 on page 39
41	TxEN2	I, ID	Table 4 on page 39
42	TxData2_0	I, ID	Table 4 on page 39
43	TxData2_1	I, ID	Table 4 on page 39
44	REFCLK0	I	Table 4 on page 39
45	RxData1_1	O, TS, ID	Table 4 on page 39
46	RxData1_0	O, TS	Table 4 on page 39
47	VCCIO	–	Table 14 on page 49
48	GNDIO	–	Table 14 on page 49
49	CRS_DV1	O, TS, SL	Table 4 on page 39
50	RxER1/PAUSE	O, TS, SL, ID	Table 12 on page 46
51	TxEN1	I, ID	Table 4 on page 39
52	TxData1_0	I, ID	Table 4 on page 39
53	TxData1_1	I, ID	Table 4 on page 39
54	RxData0_1	O, TS, ID	Table 4 on page 39
55	RxData0_0	O, TS	Table 4 on page 39
56	VCCIO	–	Table 14 on page 49
57	GNDIO	–	Table 14 on page 49
58	CRS_DV0	O, TS, SL	Table 4 on page 39
59	RxER0/MDIX	O, TS, SL, ID	Table 12 on page 46
60	TxEN0	I, ID	Table 4 on page 39
61	TxData0_0	I, ID	Table 4 on page 39
62	TxData0_1	I, ID	Table 4 on page 39
63	MDC0	I, ST, ID	Table 8 on page 43
64	MDIO0	I/O, TS, SL, IP	Table 8 on page 43
65	VCCD	–	Table 14 on page 49
66	GNDD	–	Table 14 on page 49
67	$\overline{\text{MDINT0}}$	OD, TS, SL, IP	Table 8 on page 43

1. AI=Analog Input, AO=Analog Output, I=Input, O=Output, OD=Open Drain output, ST=Schmitt Triggered input, TS=Tri-State-able output, SL=Slew-rate Limited output, IP=Weak Internal Pull-up, ID=Weak Internal Pull-down

Table 1. RMII PQFP Pin List (Continued)

Pin	Symbol	Type[1]	Reference for Full Description
68	LED3_3	OD, TS, SO, IP	Table 13 on page 48
69	LED3_2	OD, TS, SL, IP	Table 13 on page 48
70	LED3_1	OD, TS, SL, IP	Table 13 on page 48
71	LED2_3	OD, TS, SL, IP	Table 13 on page 48
72	LED2_2	OD, TS, SL, IP	Table 13 on page 48
73	LED2_1	OD, TS, SL, IP	Table 13 on page 48
74	GNDIO	–	Table 14 on page 49
75	LED1_3	OD, TS, SL, IP	Table 13 on page 48
76	LED1_2	OD, TS, SL, IP	Table 13 on page 48
77	LED1_1	OD, TS, SL, IP	Table 13 on page 48
78	VCCD	–	Table 14 on page 49
79	GNDD	–	Table 14 on page 49
80	LED0_3	OD, TS, SL, IP	Table 13 on page 48
81	LED0_2	OD, TS, SL, IP	Table 13 on page 48
82	LED0_1	OD, TS, SL, IP	Table 13 on page 48
83	AMDIX_EN	I, ST, IP	Table 12 on page 46
84	MDDIS	I, ST, ID	Table 8 on page 43
85	CFG_3	I, ST, ID	Table 12 on page 46
86	CFG_2	I, ST, ID	Table 12 on page 46
87	CFG_1	I, ST, ID	Table 12 on page 46
88	ADD_4	I, ST, ID	Table 12 on page 46
89	ADD_3	I, ST, ID	Table 12 on page 46
90	ADD_2	I, ST, ID	Table 12 on page 46
91	ADD_1	I, ST, ID	Table 12 on page 46
92	ADD_0	I, ST, ID	Table 12 on page 46
93	TxSLEW_1	I, ST, ID	Table 12 on page 46
94	TxSLEW_0	I, ST, ID	Table 12 on page 46
95	SD_2P5V	I, ST, ID	Table 9 on page 44
96	SD0	I	Table 9 on page 44
97	SD1	I	Table 9 on page 44
98	VCCPECL	–	Table 14 on page 49
99	GNDPECL	–	Table 14 on page 49
100	SD2	I	Table 9 on page 44
101	SD3	I	Table 9 on page 44

1. AI=Analog Input, AO=Analog Output, I=Input, O=Output, OD=Open Drain output, ST=Schmitt Triggered input, TS=Tri-State-able output, SL=Slew-rate Limited output, IP=Weak Internal Pull-up, ID=Weak Internal Pull-down

Table 1. RMII PQFP Pin List (Continued)

Pin	Symbol	Type[1]	Reference for Full Description
102	N/C	–	Table 15 on page 50
103	VCCR0	–	Table 14 on page 49
104	TPFIP0	AO/AI	Table 10 on page 44
105	TPFIN0	AO/AI	Table 10 on page 44
106	GNDR0	–	Table 14 on page 49
107	TPFOP0	AO/AI	Table 10 on page 44
108	TPFON0	AO/AI	Table 10 on page 44
109	VCCT0/1	–	Table 14 on page 49
110	TPFON1	AO/AI	Table 10 on page 44
111	TPFOP1	AO/AI	Table 10 on page 44
112	GNDR1	–	Table 14 on page 49
113	GNDT0/1	–	Table 14 on page 49
114	TPFIN1	AO/AI	Table 10 on page 44
115	TPFIP1	AO/AI	Table 10 on page 44
116	VCCR1	–	Table 14 on page 49
117	VCCR2	–	Table 14 on page 49
118	TPFIP2	AO/AI	Table 10 on page 44
119	TPFIN2	AO/AI	Table 10 on page 44
120	GNDR2	–	Table 14 on page 49
121	TPFOP2	AO/AI	Table 10 on page 44
122	TPFON2	AO/AI	Table 10 on page 44
123	VCCT2/3	–	Table 14 on page 49
124	TPFON3	AO/AI	Table 10 on page 44
125	TPFOP3	AO/AI	Table 10 on page 44
126	GNDR3	–	Table 14 on page 49
127	GNDT2/3	–	Table 14 on page 49
128	TPFIN3	AO/AI	Table 10 on page 44
129	TPFIP3	AO/AI	Table 10 on page 44
130	VCCR3	–	Table 14 on page 49
131	VCCR4	–	Table 14 on page 49
132	TPFIP4	AO/AI	Table 10 on page 44
133	TPFIN4	AO/AI	Table 10 on page 44
134	GNDT4/5	–	Table 14 on page 49
135	GNDR4	–	Table 14 on page 49

1. AI=Analog Input, AO=Analog Output, I=Input, O=Output, OD=Open Drain output, ST=Schmitt Triggered input, TS=Tri-State-able output, SL=Slew-rate Limited output, IP=Weak Internal Pull-up, ID=Weak Internal Pull-down

Table 1. RMII PQFP Pin List (Continued)

Pin	Symbol	Type[1]	Reference for Full Description
136	TPFOP4	AO/AI	Table 10 on page 44
137	TPFON4	AO/AI	Table 10 on page 44
138	VCCT4/5	–	Table 14 on page 49
139	TPFON5	AO/AI	Table 10 on page 44
140	TPFOP5	AO/AI	Table 10 on page 44
141	GNDR5	–	Table 14 on page 49
142	TPFIN5	AO/AI	Table 10 on page 44
143	TPFIP5	AO/AI	Table 10 on page 44
144	VCCR5	–	Table 14 on page 49
145	VCCR6	–	Table 14 on page 49
146	TPFIP6	AO/AI	Table 10 on page 44
147	TPFIN6	AO/AI	Table 10 on page 44
148	GNDT6/7	–	Table 14 on page 49
149	GNDR6	–	Table 14 on page 49
150	TPFOP6	AO/AI	Table 10 on page 44
151	TPFON6	AO/AI	Table 10 on page 44
152	VCCT6/7	–	Table 14 on page 49
153	TPFON7	AO/AI	Table 10 on page 44
154	TPFOP7	AO/AI	Table 10 on page 44
155	GNDR7	–	Table 14 on page 49
156	TPFIN7	AO/AI	Table 10 on page 44
157	TPFIP7	AO/AI	Table 10 on page 44
158	VCCR7	–	Table 14 on page 49
159	N/C	–	Table 15 on page 50
160	N/C	–	Table 15 on page 50
161	SD4	I	Table 9 on page 44
162	SD5	I	Table 9 on page 44
163	GNDPECL	–	Table 14 on page 49
164	VCCPECL	–	Table 14 on page 49
165	SD6	I	Table 9 on page 44
166	SD7	I	Table 9 on page 44
167	TDI	I, ST, IP	Table 11 on page 45
168	TDO	O, TS	Table 11 on page 45
169	TMS	I, ST, IP	Table 11 on page 45

1. AI=Analog Input, AO=Analog Output, I=Input, O=Output, OD=Open Drain output, ST=Schmitt Triggered input, TS=Tri-State-able output, SL=Slew-rate Limited output, IP=Weak Internal Pull-up, ID=Weak Internal Pull-down

Table 1. RMII PQFP Pin List (Continued)

Pin	Symbol	Type[1]	Reference for Full Description
170	TCK	I, ST, ID	Table 11 on page 45
171	TRST	I, ST, IP	Table 11 on page 45
172	N/C	–	Table 15 on page 50
173	G_FX/$\overline{TP}$	I, ST, ID	Table 12 on page 46
174	PWRDWN	I, ST, ID	Table 12 on page 46
175	RESET	I, ST, IP	Table 12 on page 46
176	Section	I, ST, ID	Table 12 on page 46
177	ModeSel0	I, ST, ID	Table 12 on page 46
178	ModeSel1	I, ST, ID	Table 12 on page 46
179	SGND	–	Table 14 on page 49
180	LED4_1	OD, TS, SL, IP	Table 13 on page 48
181	LED4_2	OD, TS, SL, IP	Table 13 on page 48
182	LED4_3	OD, TS, SL, IP	Table 13 on page 48
183	GNDD	–	Table 14 on page 49
184	VCCD	–	Table 14 on page 49
185	LED5_1	OD, TS, SL, IP	Table 13 on page 48
186	LED5_2	OD, TS, SL, IP	Table 13 on page 48
187	LED5_3	OD, TS, SL, IP	Table 13 on page 48
188	GNDIO	–	Table 14 on page 49
189	LED6_1	OD, TS, SL, IP	Table 13 on page 48
190	LED6_2	OD, TS, SL, IP	Table 13 on page 48
191	LED6_3	OD, TS, SL, IP	Table 13 on page 48
192	LED7_1	OD, TS, SL, IP	Table 13 on page 48
193	LED7_2	OD, TS, SL, IP	Table 13 on page 48
194	LED7_3	OD, TS, SL, IP	Table 13 on page 48
195	GNDD	–	Table 14 on page 49
196	VCCD	–	Table 14 on page 49
197	RxData7_1	O, TS, ID	Table 4 on page 39
198	RxData7_0	O, TS	Table 4 on page 39
199	GNDIO	–	Table 14 on page 49
200	CRS_DV7	O, TS, SL	Table 4 on page 39
201	RxER7	O, TS, SL, ID	Table 4 on page 39
202	TxEN7	I, ID	Table 4 on page 39
203	TxData7_0	I, ID	Table 4 on page 39

1. AI=Analog Input, AO=Analog Output, I=Input, O=Output, OD=Open Drain output, ST=Schmitt Triggered input, TS=Tri-State-able output, SL=Slew-rate Limited output, IP=Weak Internal Pull-up, ID=Weak Internal Pull-down

Table 1. RMII PQFP Pin List (Continued)

Pin	Symbol	Type[1]	Reference for Full Description
204	TxData7_1	I, ID	Table 4 on page 39
205	RxData6_1	O, TS, ID	Table 4 on page 39
206	RxData6_0	O, TS	Table 4 on page 39
207	GNDIO	–	Table 14 on page 49
208	VCCIO	–	Table 14 on page 49

1. AI=Analog Input, AO=Analog Output, I=Input, O=Output, OD=Open Drain output, ST=Schmitt Triggered input, TS=Tri-State-able output, SL=Slew-rate Limited output, IP=Weak Internal Pull-up, ID=Weak Internal Pull-down

Table 2. SMII PQFP Pin List

Pin	Symbol	Type[1]	Reference for Full Description
1	N/C	–	Table 15 on page 50
2	N/C	–	Table 15 on page 50
3	N/C	–	Table 15 on page 50
4	TxData6	I, ID	Table 15 on page 50
5	N/C	I, ID	Table 15 on page 50
6	REFCLK1	I	Table 5 on page 41
7	N/C	–	Table 15 on page 50
8	RxData5	O, TS	Table 6 on page 41
9	GNDIO	–	Table 14 on page 49
10	N/C	–	Table 15 on page 50
11	N/C	–	Table 15 on page 50
12	N/C	–	Table 15 on page 50
13	TxData5	I, ID	Table 5 on page 41
14	N/C	–	Table 15 on page 50
15	N/C	O, TS,ID	Table 15 on page 50
16	RxData4	O, TS	Table 6 on page 41
17	N/C	–	Table 15 on page 50
18	VCCIO	–	Table 14 on page 49
19	GNDIO	–	Table 14 on page 49
20	N/C	O, TS, SL, ID	Table 15 on page 50
21	N/C	I, ID	Table 15 on page 50
22	TxData4	I, ID	Table 5 on page 41
23	N/C	–	Table 15 on page 50
24	MDC1	I, ST, ID	Table 8 on page 43
25	MDIO1	I/O, TS, SL, IP	Table 8 on page 43
26	$\overline{\text{MDINT1}}$	OD, TS, SL, IP	Table 8 on page 43
27	N/C	–	Table 15 on page 50
28	RxData3	O, TS	Table 6 on page 41
29	VCCIO	–	Table 14 on page 49
30	GNDIO	–	Table 14 on page 49
31	N/C	–	Table 15 on page 50
32	N/C	–	Table 15 on page 50
33	N/C	–	Table 15 on page 50

1. AI=Analog Input, AO=Analog Output, I=Input, O=Output, OD=Open Drain output, ST=Schmitt Triggered input, TS=Tri-State-able output, SL=Slew-rate Limited output, IP=Weak Internal Pull-up, ID=Weak Internal Pull-down

Table 2. SMII PQFP Pin List (Continued)

Pin	Symbol	Type[1]	Reference for Full Description
34	TxData3	I, ID	Table 5 on page 41
35	SYNC0	I, ID	Table 6 on page 41
36	N/C	–	Table 15 on page 50
37	RxData2	O, TS	Table 6 on page 41
38	GNDIO	–	Table 14 on page 49
39	N/C	–	Table 15 on page 50
40	N/C	–	Table 15 on page 50
41	N/C	–	Table 15 on page 50
42	TxData2	I, ID	Table 5 on page 41
43	N/C	–	Table 15 on page 50
44	REFCLK0	I	Table 5 on page 41
45	N/C	–	Table 15 on page 50
46	RxData1	O, TS	Table 6 on page 41
47	VCCIO	–	Table 14 on page 49
48	GNDIO	–	Table 14 on page 49
49	N/C	–	Table 15 on page 50
50	PAUSE	I, ID	Table 12 on page 46
51	N/C	–	Table 15 on page 50
52	TxData1	I, ID	Table 5 on page 41
53	N/C	–	Table 15 on page 50
54	N/C	–	Table 15 on page 50
55	RxData0	O, TS	Table 6 on page 41
56	VCCIO	–	Table 14 on page 49
57	GNDIO	–	Table 14 on page 49
58	N/C	–	Table 15 on page 50
59	MDIX	I, ID	Table 12 on page 46
60	N/C	–	Table 15 on page 50
61	TxData0	I, ID	Table 5 on page 41
62	N/C	–	Table 15 on page 50
63	MDC0	I, ST, ID	Table 8 on page 43
64	MDIO0	I/O, TS, SL, IP	Table 8 on page 43
65	VCCD	–	Table 14 on page 49
66	GNDD	–	Table 14 on page 49
67	$\overline{\text{MDINT0}}$	OD, TS, SL, IP	Table 8 on page 43

1. AI=Analog Input, AO=Analog Output, I=Input, O=Output, OD=Open Drain output, ST=Schmitt Triggered input, TS=Tri-State-able output, SL=Slew-rate Limited output, IP=Weak Internal Pull-up, ID=Weak Internal Pull-down

Table 2. SMII PQFP Pin List (Continued)

Pin	Symbol	Type[1]	Reference for Full Description
68	LED3_3	OD, TS, SO, IP	Table 13 on page 48
69	LED3_2	OD, TS, SL, IP	Table 13 on page 48
70	LED3_1	OD, TS, SL, IP	Table 13 on page 48
71	LED2_3	OD, TS, SL, IP	Table 13 on page 48
72	LED2_2	OD, TS, SL, IP	Table 13 on page 48
73	LED2_1	OD, TS, SL, IP	Table 13 on page 48
74	GNDIO	–	Table 14 on page 49
75	LED1_3	OD, TS, SL, IP	Table 13 on page 48
76	LED1_2	OD, TS, SL, IP	Table 13 on page 48
77	LED1_1	OD, TS, SL, IP	Table 13 on page 48
78	VCCD	–	Table 14 on page 49
79	GNDD	–	Table 14 on page 49
80	LED0_3	OD, TS, SL, IP	Table 13 on page 48
81	LED0_2	OD, TS, SL, IP	Table 13 on page 48
82	LED0_1	OD, TS, SL, IP	Table 13 on page 48
83	AMDIX_EN	I, ST, IP	Table 12 on page 46
84	MDDIS	I, ST, ID	Table 8 on page 43
85	CFG_3	I, ST, ID	Table 12 on page 46
86	CFG_2	I, ST, ID	Table 12 on page 46
87	CFG_1	I, ST, ID	Table 12 on page 46
88	ADD_4	I, ST, ID	Table 12 on page 46
89	ADD_3	I, ST, ID	Table 12 on page 46
90	ADD_2	I, ST, ID	Table 12 on page 46
91	ADD_1	I, ST, ID	Table 12 on page 46
92	ADD_0	I, ST, ID	Table 12 on page 46
93	TxSLEW_1	I, ST, ID	Table 12 on page 46
94	TxSLEW_0	I, ST, ID	Table 12 on page 46
95	SD_2P5V	I, ST, ID	Table 9 on page 44
96	SD0	I	Table 9 on page 44
97	SD1	I	Table 9 on page 44
98	VCCPECL	–	Table 14 on page 49
99	GNDPECL	–	Table 14 on page 49
100	SD2	I	Table 9 on page 44
101	SD3	I	Table 9 on page 44

1. AI=Analog Input, AO=Analog Output, I=Input, O=Output, OD=Open Drain output, ST=Schmitt Triggered input, TS=Tri-State-able output, SL=Slew-rate Limited output, IP=Weak Internal Pull-up, ID=Weak Internal Pull-down

Table 2. SMII PQFP Pin List (Continued)

Pin	Symbol	Type[1]	Reference for Full Description
102	N/C	–	Table 15 on page 50
103	VCCR0	–	Table 14 on page 49
104	TPFIP0	AI/AO	Table 10 on page 44
105	TPFIN0	AI/AO	Table 10 on page 44
106	GNDR0	–	Table 14 on page 49
107	TPFOP0	AO/AI	Table 10 on page 44
108	TPFON0	AO/AI	Table 10 on page 44
109	VCCT0/1	–	Table 14 on page 49
110	TPFON1	AO/AI	Table 10 on page 44
111	TPFOP1	AO/AI	Table 10 on page 44
112	GNDR1	–	Table 14 on page 49
113	GNDT0/1	–	Table 14 on page 49
114	TPFIN1	AI/AO	Table 10 on page 44
115	TPFIP1	AI/AO	Table 10 on page 44
116	VCCR1	–	Table 14 on page 49
117	VCCR2	–	Table 14 on page 49
118	TPFIP2	AI/AO	Table 10 on page 44
119	TPFIN2	AI/AO	Table 10 on page 44
120	GNDR2	–	Table 14 on page 49
121	TPFOP2	AO/AI	Table 10 on page 44
122	TPFON2	AO/AI	Table 10 on page 44
123	VCCT2/3	–	Table 14 on page 49
124	TPFON3	AO/AI	Table 10 on page 44
125	TPFOP3	AO/AI	Table 10 on page 44
126	GNDR3	–	Table 14 on page 49
127	GNDT2/3	–	Table 14 on page 49
128	TPFIN3	AI/AO	Table 10 on page 44
129	TPFIP3	AI/AO	Table 10 on page 44
130	VCCR3	–	Table 14 on page 49
131	VCCR4	–	Table 14 on page 49
132	TPFIP4	AI/AO	Table 10 on page 44
133	TPFIN4	AI/AO	Table 10 on page 44
134	GNDT4/5	–	Table 14 on page 49
135	GNDR4	–	Table 14 on page 49

1. AI=Analog Input, AO=Analog Output, I=Input, O=Output, OD=Open Drain output, ST=Schmitt Triggered input, TS=Tri-State-able output, SL=Slew-rate Limited output, IP=Weak Internal Pull-up, ID=Weak Internal Pull-down

Table 2. SMII PQFP Pin List (Continued)

Pin	Symbol	Type[1]	Reference for Full Description
136	TPFOP4	AO/AI	Table 10 on page 44
137	TPFON4	AO/AI	Table 10 on page 44
138	VCCT4/5	–	Table 14 on page 49
139	TPFON5	AO/AI	Table 10 on page 44
140	TPFOP5	AO/AI	Table 10 on page 44
141	GNDR5	–	Table 14 on page 49
142	TPFIN5	AI/AO	Table 10 on page 44
143	TPFIP5	AI/AO	Table 10 on page 44
144	VCCR5	–	Table 14 on page 49
145	VCCR6	–	Table 14 on page 49
146	TPFIP6	AI/AO	Table 10 on page 44
147	TPFIN6	AI/AO	Table 10 on page 44
148	GNDT6/7	–	Table 14 on page 49
149	GNDR6	–	Table 14 on page 49
150	TPFOP6	AO/AI	Table 10 on page 44
151	TPFON6	AO/AI	Table 10 on page 44
152	VCCT6/7	–	Table 14 on page 49
153	TPFON7	AO/AI	Table 10 on page 44
154	TPFOP7	AO/AI	Table 10 on page 44
155	GNDR7	–	Table 14 on page 49
156	TPFIN7	AI/AO	Table 10 on page 44
157	TPFIP7	AI/AO	Table 10 on page 44
158	VCCR7	–	Table 14 on page 49
159	N/C	–	Table 15 on page 50
160	N/C	–	Table 15 on page 50
161	SD4	I	Table 9 on page 44
162	SD5	I	Table 9 on page 44
163	GNDPECL	–	Table 14 on page 49
164	VCCPECL	–	Table 14 on page 49
165	SD6	I	Table 9 on page 44
166	SD7	I	Table 9 on page 44
167	TDI	I, ST, IP	Table 11 on page 45
168	TDO	O, TS	Table 11 on page 45
169	TMS	I, ST, IP	Table 11 on page 45

1. AI=Analog Input, AO=Analog Output, I=Input, O=Output, OD=Open Drain output, ST=Schmitt Triggered input, TS=Tri-State-able output, SL=Slew-rate Limited output, IP=Weak Internal Pull-up, ID=Weak Internal Pull-down

Table 2. SMII PQFP Pin List (Continued)

Pin	Symbol	Type[1]	Reference for Full Description
170	TCK	I, ST, ID	Table 11 on page 45
171	TRST	I, ST, IP	Table 11 on page 45
172	N/C	–	Table 15 on page 50
173	G_FX/$\overline{TP}$	I, ST, ID	Table 12 on page 46
174	PWRDWN	I, ST, ID	Table 12 on page 46
175	RESET	I, ST, IP	Table 12 on page 46
176	Section	I, ST, ID	Table 12 on page 46
177	ModeSel0	I, ST, ID	Table 12 on page 46
178	ModeSel1	I, ST, ID	Table 12 on page 46
179	SGND	–	Table 14 on page 49
180	LED4_1	OD, TS, SL, IP	Table 13 on page 48
181	LED4_2	OD, TS, SL, IP	Table 13 on page 48
182	LED4_3	OD, TS, SL, IP	Table 13 on page 48
183	GNDD	–	Table 14 on page 49
184	VCCD	–	Table 14 on page 49
185	LED5_1	OD, TS, SL, IP	Table 13 on page 48
186	LED5_2	OD, TS, SL, IP	Table 13 on page 48
187	LED5_3	OD, TS, SL, IP	Table 13 on page 48
188	GNDIO	–	Table 14 on page 49
189	LED6_1	OD, TS, SL, IP	Table 13 on page 48
190	LED6_2	OD, TS, SL, IP	Table 13 on page 48
191	LED6_3	OD, TS, SL, IP	Table 13 on page 48
192	LED7_1	OD, TS, SL, IP	Table 13 on page 48
193	LED7_2	OD, TS, SL, IP	Table 13 on page 48
194	LED7_3	OD, TS, SL, IP	Table 13 on page 48
195	GNDD	–	Table 14 on page 49
196	VCCD	–	Table 14 on page 49
197	N/C	O, TS, ID	Table 4 on page 39
198	RxData7	O, TS	Table 6 on page 41
199	GNDIO	–	Table 14 on page 49
200	N/C	–	Table 15 on page 50
201	N/C	–	Table 15 on page 50
202	N/C	–	Table 15 on page 50
203	TxData7	I, ID	Table 5 on page 41

1. AI=Analog Input, AO=Analog Output, I=Input, O=Output, OD=Open Drain output, ST=Schmitt Triggered input, TS=Tri-State-able output, SL=Slew-rate Limited output, IP=Weak Internal Pull-up, ID=Weak Internal Pull-down

Table 2. SMII PQFP Pin List (Continued)

Pin	Symbol	Type[1]	Reference for Full Description
204	SYNC1	I, ID	Table 6 on page 41
205	N/C	–	Table 15 on page 50
206	RxData6	O, TS	Table 6 on page 41
207	GNDIO	–	Table 14 on page 49
208	VCCIO	–	Table 14 on page 49

1. AI=Analog Input, AO=Analog Output, I=Input, O=Output, OD=Open Drain output, ST=Schmitt Triggered input, TS=Tri-State-able output, SL=Slew-rate Limited output, IP=Weak Internal Pull-up, ID=Weak Internal Pull-down

Table 3. SS-SMII PQFP Pin List

Pin	Symbol	Type[1]	Reference for Full Description
1	N/C	–	Table 15 on page 50
2	N/C	–	Table 15 on page 50
3	N/C	–	Table 15 on page 50
4	TxData6	I, ID	Table 5 on page 41
5	N/C	I, ID	Table 15 on page 50
6	REFCLK1	I	Table 5 on page 41
7	RxData5	O, TS, ID	Table 7 on page 42
8	N/C	–	Table 15 on page 50
9	GNDIO	–	Table 14 on page 49
10	N/C	–	Table 15 on page 50
11	N/C	–	Table 15 on page 50
12	N/C	–	Table 15 on page 50
13	TxData5	I, ID	Table 5 on page 41
14	N/C	–	Table 15 on page 50
15	RxData4	O, TS, ID	Table 7 on page 42
16	N/C	–	Table 15 on page 50
17	RxSYNC1	O, TS, ID	Table 7 on page 42
18	VCCIO	–	Table 14 on page 49
19	GNDIO	–	Table 14 on page 49
20	N/C	–	Table 15 on page 50
21	RxCLK1	O, TS, ID	Table 7 on page 42
22	TxData4	I, ID	Table 5 on page 41
23	N/C	–	Table 15 on page 50
24	MDC1	I, ST, ID	Table 8 on page 43
25	MDIO1	I/O, TS, SL, IP	Table 8 on page 43
26	$\overline{\text{MDINT1}}$	OD, TS, SL, IP	Table 8 on page 43
27	RxData3	O, TS, ID	Table 7 on page 42
28	N/C	–	Table 15 on page 50
29	VCCIO	–	Table 14 on page 49
30	GNDIO	–	Table 14 on page 49
31	N/C	–	Table 15 on page 50
32	TxCLK0	I, ID	Table 7 on page 42
33	N/C	–	Table 15 on page 50

1. AI=Analog Input, AO=Analog Output, I=Input, O=Output, OD=Open Drain output, ST=Schmitt Triggered input, TS=Tri-State-able output, SL=Slew-rate Limited output, IP=Weak Internal Pull-up, ID=Weak Internal Pull-down

Table 3. SS-SMII PQFP Pin List (Continued)

Pin	Symbol	Type[1]	Reference for Full Description
34	TxData3	I, ID	Table 5 on page 41
35	TxSYNC0	I, ID	Table 7 on page 42
36	RxData2	O, TS, ID	Table 7 on page 42
37	N/C	–	Table 15 on page 50
38	GNDIO	–	Table 14 on page 49
39	N/C	–	Table 15 on page 50
40	N/C	–	Table 15 on page 50
41	N/C	–	Table 15 on page 50
42	TxData2	I, ID	Table 5 on page 41
43	N/C	–	Table 15 on page 50
44	REFCLK0	I	Table 5 on page 41
45	RxData1	O, TS, ID	Table 7 on page 42
46	N/C	–	Table 15 on page 50
47	VCCIO	–	Table 14 on page 49
48	GNDIO	–	Table 14 on page 49
49	N/C	–	Table 15 on page 50
50	PAUSE	I, ID	Table 12 on page 46
51	N/C	–	Table 15 on page 50
52	TxData1	I, ID	Table 5 on page 41
53	N/C	–	Table 15 on page 50
54	RxData0	O, TS, ID	Table 7 on page 42
55	N/C	–	Table 15 on page 50
56	VCCIO	–	Table 14 on page 49
57	GNDIO	–	Table 14 on page 49
58	RxSYNC0	O, TS, ID	Table 7 on page 42
59	MDIX	I, ID	Table 12 on page 46
60	RxCLK0	–	Table 7 on page 42
61	TxData0	I, ID	Table 5 on page 41
62	N/C	–	Table 15 on page 50
63	MDC0	I, ST, ID	Table 8 on page 43
64	MDIO0	I/O, TS, SL, IP	Table 8 on page 43
65	VCCD	–	Table 14 on page 49
66	GNDD	–	Table 14 on page 49
67	$\overline{\text{MDINT0}}$	OD, TS, SL, IP	Table 8 on page 43

1. AI=Analog Input, AO=Analog Output, I=Input, O=Output, OD=Open Drain output, ST=Schmitt Triggered input, TS=Tri-State-able output, SL=Slew-rate Limited output, IP=Weak Internal Pull-up, ID=Weak Internal Pull-down

Table 3. SS-SMII PQFP Pin List (Continued)

Pin	Symbol	Type[1]	Reference for Full Description
68	LED3_3	OD, TS, SO, IP	Table 13 on page 48
69	LED3_2	OD, TS, SL, IP	Table 13 on page 48
70	LED3_1	OD, TS, SL, IP	Table 13 on page 48
71	LED2_3	OD, TS, SL, IP	Table 13 on page 48
72	LED2_2	OD, TS, SL, IP	Table 13 on page 48
73	LED2_1	OD, TS, SL, IP	Table 13 on page 48
74	GNDIO	–	Table 14 on page 49
75	LED1_3	OD, TS, SL, IP	Table 13 on page 48
76	LED1_2	OD, TS, SL, IP	Table 13 on page 48
77	LED1_1	OD, TS, SL, IP	Table 13 on page 48
78	VCCD	–	Table 14 on page 49
79	GNDD	–	Table 14 on page 49
80	LED0_3	OD, TS, SL, IP	Table 13 on page 48
81	LED0_2	OD, TS, SL, IP	Table 13 on page 48
82	LED0_1	OD, TS, SL, IP	Table 13 on page 48
83	AMDIX_EN	I, ST, IP	Table 12 on page 46
84	MDDIS	I, ST, ID	Table 8 on page 43
85	CFG_3	I, ST, ID	Table 12 on page 46
86	CFG_2	I, ST, ID	Table 12 on page 46
87	CFG_1	I, ST, ID	Table 12 on page 46
88	ADD_4	I, ST, ID	Table 12 on page 46
89	ADD_3	I, ST, ID	Table 12 on page 46
90	ADD_2	I, ST, ID	Table 12 on page 46
91	ADD_1	I, ST, ID	Table 12 on page 46
92	ADD_0	I, ST, ID	Table 12 on page 46
93	TxSLEW_1	I, ST, ID	Table 12 on page 46
94	TxSLEW_0	I, ST, ID	Table 12 on page 46
95	SD_2P5V	I, ST, ID	Table 9 on page 44
96	SD0	I	Table 9 on page 44
97	SD1	I	Table 9 on page 44
98	VCCPECL	–	Table 14 on page 49
99	GNDPECL	–	Table 14 on page 49
100	SD2	I	Table 9 on page 44
101	SD3	I	Table 9 on page 44

1. AI=Analog Input, AO=Analog Output, I=Input, O=Output, OD=Open Drain output, ST=Schmitt Triggered input, TS=Tri-State-able output, SL=Slew-rate Limited output, IP=Weak Internal Pull-up, ID=Weak Internal Pull-down

Table 3. SS-SMII PQFP Pin List (Continued)

Pin	Symbol	Type[1]	Reference for Full Description
102	N/C	–	Table 15 on page 50
103	VCCR0	–	Table 14 on page 49
104	TPFIP0	AI/AO	Table 10 on page 44
105	TPFIN0	AI/AO	Table 10 on page 44
106	GNDR0	–	Table 14 on page 49
107	TPFOP0	AO/AI	Table 10 on page 44
108	TPFON0	AO/AI	Table 10 on page 44
109	VCCT0/1	–	Table 14 on page 49
110	TPFON1	AO/AI	Table 10 on page 44
111	TPFOP1	AO/AI	Table 10 on page 44
112	GNDR1	–	Table 14 on page 49
113	GNDT0/1	–	Table 14 on page 49
114	TPFIN1	AI/AO	Table 10 on page 44
115	TPFIP1	AI/AO	Table 10 on page 44
116	VCCR1	–	Table 14 on page 49
117	VCCR2	–	Table 14 on page 49
118	TPFIP2	AI/AO	Table 10 on page 44
119	TPFIN2	AI/AO	Table 10 on page 44
120	GNDR2	–	Table 14 on page 49
121	TPFOP2	AO/AI	Table 10 on page 44
122	TPFON2	AO/AI	Table 10 on page 44
123	VCCT2/3	–	Table 14 on page 49
124	TPFON3	AO/AI	Table 10 on page 44
125	TPFOP3	AO/AI	Table 10 on page 44
126	GNDR3	–	Table 14 on page 49
127	GNDT2/3	–	Table 14 on page 49
128	TPFIN3	AI/AO	Table 10 on page 44
129	TPFIP3	AI/AO	Table 10 on page 44
130	VCCR3	–	Table 14 on page 49
131	VCCR4	–	Table 14 on page 49
132	TPFIP4	AI/AO	Table 10 on page 44
133	TPFIN4	AI/AO	Table 10 on page 44
134	GNDT4/5	–	Table 14 on page 49
135	GNDR4	–	Table 14 on page 49

1. AI=Analog Input, AO=Analog Output, I=Input, O=Output, OD=Open Drain output, ST=Schmitt Triggered input, TS=Tri-State-able output, SL=Slew-rate Limited output, IP=Weak Internal Pull-up, ID=Weak Internal Pull-down

Table 3. SS-SMII PQFP Pin List (Continued)

Pin	Symbol	Type[1]	Reference for Full Description
136	TPFOP4	AO/AI	Table 10 on page 44
137	TPFON4	AO/AI	Table 10 on page 44
138	VCCT4/5	–	Table 14 on page 49
139	TPFON5	AO/AI	Table 10 on page 44
140	TPFOP5	AO/AI	Table 10 on page 44
141	GNDR5	–	Table 14 on page 49
142	TPFIN5	AI/AO	Table 10 on page 44
143	TPFIP5	AI/AO	Table 10 on page 44
144	VCCR5	–	Table 14 on page 49
145	VCCR6	–	Table 14 on page 49
146	TPFIP6	AI/AO	Table 10 on page 44
147	TPFIN6	AI/AO	Table 10 on page 44
148	GNDT6/7	–	Table 14 on page 49
149	GNDR6	–	Table 14 on page 49
150	TPFOP6	AO/AI	Table 10 on page 44
151	TPFON6	AO/AI	Table 10 on page 44
152	VCCT6/7	–	Table 14 on page 49
153	TPFON7	AO/AI	Table 10 on page 44
154	TPFOP7	AO/AI	Table 10 on page 44
155	GNDR7	–	Table 14 on page 49
156	TPFIN7	AI/AO	Table 10 on page 44
157	TPFIP7	AI/AO	Table 10 on page 44
158	VCCR7	–	Table 14 on page 49
159	N/C	–	Table 15 on page 50
160	N/C	–	Table 15 on page 50
161	SD4	I	Table 9 on page 44
162	SD5	I	Table 9 on page 44
163	GNDPECL	–	Table 14 on page 49
164	VCCPECL	–	Table 14 on page 49
165	SD6	I	Table 9 on page 44
166	SD7	I	Table 9 on page 44
167	TDI	I, ST, IP	Table 11 on page 45
168	TDO	O, TS	Table 11 on page 45
169	TMS	I, ST, IP	Table 11 on page 45

1. AI=Analog Input, AO=Analog Output, I=Input, O=Output, OD=Open Drain output, ST=Schmitt Triggered input, TS=Tri-State-able output, SL=Slew-rate Limited output, IP=Weak Internal Pull-up, ID=Weak Internal Pull-down

Table 3. SS-SMII PQFP Pin List (Continued)

Pin	Symbol	Type[1]	Reference for Full Description
170	TCK	I, ST, ID	Table 11 on page 45
171	TRST	I, ST, IP	Table 11 on page 45
172	N/C	–	Table 15 on page 50
173	G_FX/$\overline{TP}$	I, ST, ID	Table 12 on page 46
174	PWRDWN	I, ST, ID	Table 12 on page 46
175	RESET	I, ST, IP	Table 12 on page 46
176	Section	I, ST, ID	Table 12 on page 46
177	ModeSel0	I, ST, ID	Table 12 on page 46
178	ModeSel1	I, ST, ID	Table 12 on page 46
179	SGND	–	Table 14 on page 49
180	LED4_1	OD, TS, SL, IP	Table 13 on page 48
181	LED4_2	OD, TS, SL, IP	Table 13 on page 48
182	LED4_3	OD, TS, SL, IP	Table 13 on page 48
183	GNDD	–	Table 14 on page 49
184	VCCD	–	Table 14 on page 49
185	LED5_1	OD, TS, SL, IP	Table 13 on page 48
186	LED5_2	OD, TS, SL, IP	Table 13 on page 48
187	LED5_3	OD, TS, SL, IP	Table 13 on page 48
188	GNDIO	–	Table 14 on page 49
189	LED6_1	OD, TS, SL, IP	Table 13 on page 48
190	LED6_2	OD, TS, SL, IP	Table 13 on page 48
191	LED6_3	OD, TS, SL, IP	Table 13 on page 48
192	LED7_1	OD, TS, SL, IP	Table 13 on page 48
193	LED7_2	OD, TS, SL, IP	Table 13 on page 48
194	LED7_3	OD, TS, SL, IP	Table 13 on page 48
195	GNDD	–	Table 14 on page 49
196	VCCD	–	Table 14 on page 49
197	RxData7	O, TS, ID	Table 7 on page 42
198	N/C	–	Table 15 on page 50
199	GNDIO	–	Table 14 on page 49
200	N/C	–	Table 15 on page 50
201	TxCLK1	I, ID	Table 7 on page 42
202	N/C	–	Table 15 on page 50
203	TxData7	I, ID	Table 5 on page 41

1. AI=Analog Input, AO=Analog Output, I=Input, O=Output, OD=Open Drain output, ST=Schmitt Triggered input, TS=Tri-State-able output, SL=Slew-rate Limited output, IP=Weak Internal Pull-up, ID=Weak Internal Pull-down

Table 3. SS-SMII PQFP Pin List (Continued)

Pin	Symbol	Type[1]	Reference for Full Description
204	TxSYNC1	I, ID	Table 7 on page 42
205	RxData6	O, TS, ID	Table 7 on page 42
206	N/C	–	Table 15 on page 50
207	GNDIO	–	Table 14 on page 49
208	VCCIO	–	Table 14 on page 49

1. AI=Analog Input, AO=Analog Output, I=Input, O=Output, OD=Open Drain output, ST=Schmitt Triggered input, TS=Tri-State-able output, SL=Slew-rate Limited output, IP=Weak Internal Pull-up, ID=Weak Internal Pull-down

1.1 Signal Name Conventions

Signal names may contain either a port designation or a serial designation, or a combination of the two designations. Signal naming conventions are as follows:

- **Port Number Only.** Individual signals that apply to a particular port are designated by the Signal Mnemonic, immediately followed by the Port Designation. For example, Transmit Enable signals would be identified as TxEN0, TxEN1, and TxEN2.
- **Serial Number Only.** A set of signals which are not tied to any specific port are designated by the Signal Mnemonic, followed by an underscore and a serial designation. For example, a set of three Global Configuration signals would be identified as CFG_1, CFG_2, and CFG_3.
- **Port and Serial Number.** In cases where each port is assigned a set of multiple signals, each signal is designated in the following order: Signal Mnemonic, Port Designation, an underscore, and the serial designation. For example, a set of three Port Configuration signals would be identified as RxData0_0 and RxData0_1, RxData1_0 and RxData1_1, and RxData2_0 and RxData2_1.

Table 4. LXT9785/9785E RMII Signal Descriptions

Pin-Ball Designation		Symbol	Type[1]	Signal Description[2,3]
PQFP	PBGA			
44 6	E6, E12	REFCLK0 REFCLK1	I	**Reference Clock**. 50 MHz RMII reference clock is always required. RMII inputs are sampled on the rising edge of REFCLK, RMII outputs are sourced on the falling edge. See "Clock/SYNC Requirements" on page 58 *for detailed CLK requirements.*
61 62	E2, F4	TxData0_0 TxData0_1	I, ID	**Transmit Data - Port 0**. Inputs containing 2-bit parallel di-bits to be transmitted from port 0 are clocked in synchronously to REFCLK.
52 53	C3, D4	TxData1_0 TxData1_1	I, ID	**Transmit Data - Port 1**. Inputs containing 2-bit parallel di-bits to be transmitted from port 1 are clocked in synchronously to REFCLK
42 43	B5 A4	TxData2_0 TxData2_1	I, ID	**Transmit Data - Port 2**. Inputs containing 2-bit parallel di-bits to be transmitted from port 2 are clocked in synchronously to REFCLK.
34 35	D8, A6	TxData3_0 TxData3_1	I, ID	**Transmit Data - Port 3**. Inputs containing 2-bit parallel di-bits to be transmitted from port 3 are clocked in synchronously to REFCLK.
22 23	A11, C10	TxData4_0 TxData4_1	I, ID	**Transmit Data - Port 4**. Inputs containing 2-bit parallel di-bits to be transmitted from port 4 are clocked in synchronously to REFCLK.
13 14	B13, D11	TxData5_0 TxData5_1	I, ID	**Transmit Data - Port 5**. Inputs containing 2-bit parallel di-bits to be transmitted from port 5 are clocked in synchronously to REFCLK.
4 5	D13, A16	TxData6_0 TxData6_1	I, ID	**Transmit Data - Port 6**. Inputs containing 2-bit parallel di-bits to be transmitted from port 6 are clocked in synchronously to REFCLK.
203 204	E14, C16	TxData7_0 TxData7_1	I, ID	**Transmit Data - Port 7**. Inputs containing 2-bit parallel di-bits to be transmitted from port 7 are clocked in synchronously to REFCLK.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Tri-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode. If a Pin is an output or an I/O, the IP/ID resistors are also disabled when the output is enabled.
3. RxData[0:7]_0, RxData[0:7]_1, CRS_DV[0:7] and RxER[0:7] outputs are tri-stated in Isolation and H/W Power-Down modes and during H/W reset.

Table 4. LXT9785/9785E RMII Signal Descriptions (Continued)

Pin-Ball Designation		Symbol	Type[1]	Signal Description[2,3]
PQFP	PBGA			
60 51 41 33 21 12 3 202	E3, B2, C6, A7, B11, A14, C14, D16	TxEN0 TxEN1 TxEN2 TxEN3 TxEN4 TxEN5 TxEN6 TxEN7	I, ID	**Transmit Enable - Ports 0-7**. Active High input enables respective port transmitter. This signal must be synchronous to the REFCLK.
55 54	C2, B1	RxData0_0 RxData0_1	O, TS O, TS, ID	**Receive Data - Port 0**. Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
46 45	A3, B4	RxData1_0 RxData1_1	O, TS O, TS, ID	**Receive Data - Port 1**. Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
37 36	B6, C7	RxData2_0 RxData2_1	O, TS O, TS, ID	**Receive Data - Port 2**. Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
28 27	D9, B9	RxData3_0 RxData3_1	O, TS O, TS, ID	**Receive Data - Port 3**. Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
16 15	A13, C12	RxData4_0 RxData4_1	O, TS O, TS, ID	**Receive Data - Port 4**. Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
8 7	B14, B15	RxData5_0 RxData5_1	O, TS O, TS, ID	**Receive Data - Port 5**. Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
206 205	C15, B17	RxData6_0 RxData6_1	O, TS O, TS, ID	**Receive Data - Port 6**. Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
198 197	E16, F14	RxData7_0 RxData7_1	O, TS O, TS, ID	**Receive Data - Port 7**. Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
58 49 39 31 17 10 1 200	E4, C4, A5, B8, B12, D12, B16, E15	CRS_DV0 CRS_DV1 CRS_DV2 CRS_DV3 CRS_DV4 CRS_DV5 CRS_DV6 CRS_DV7	O, TS, SL, ID	**Carrier Sense/Receive Data Valid - Ports 0-7**. On detection of valid carrier, these signals are asserted asynchronously with respect to REFCLK. CRS_DVn is de-asserted on loss of carrier, synchronous to REFCLK.
59 50 40 32 20 11 2 201	D2, D5, D7, C8, A12, A15, A17, D17	RxER0 RxER1 RxER2 RxER3 RxER4 RxER5 RxER6 RxER7	O, TS, SL, ID	**Receive Error - Ports 0-7**. These signals are synchronous to the respective REFCLK. Active High indicates that received code group is invalid, or that PLL is not locked.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Tri-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode. If a Pin is an output or an I/O, the IP/ID resistors are also disabled when the output is enabled.
3. RxData[0:7]_0, RxData[0:7]_1, CRS_DV[0:7] and RxER[0:7] outputs are tri-stated in Isolation and H/W Power-Down modes and during H/W reset.

Table 5. LXT9785/9785E SMII / SS-SMII Common Signal Descriptions

Pin/Ball Designation		Symbol	Type[1]	Signal Description[2]
PQFP	PBGA			
61 52 42 34 22 13 4 203	E2, C3, B5, D8, A11, B13, D13, E14	TxData0 TxData1 TxData2 TxData3 TxData4 TxData5 TxData6 TxData7	I, ID	**Transmit Data - Ports 0-7**. These serial input streams provide data to be transmitted to the network. The LXT9785/9785E clocks the data in synchronously to REFCLK.
44 6	E6, E12	REFCLK0 REFCLK1	I	**Reference Clock**. The LXT9785/9785E always requires a 125 MHz reference clock input. Refer to Functional Description for detailed clock requirements. REFCLK0 and REFCLK1 are always connected regardless of sectionalization mode.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Tri-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode.

Table 6. LXT9785/9785E SMII Specific Signal Descriptions

Pin/Ball Designation		Symbol	Type[1]	Signal Description[2,3]
PQFP	PBGA			
35 204	A6, C16	SYNC0 SYNC1	I, ID	**SMII Synchronization.** The MAC must generate a SYNC pulse every 10 REFCLK cycles to synchronize the SMII. SYNC0 is used when 1x8 port sectionalization is selected. SYNC0 and SYNC1 are to be used when 2x4 port sectionalization is chosen.
55 46 37 28 16 8 206 198	C2, A3, B6, D9, A13, B14, C15, E16	RxData0 RxData1 RxData2 RxData3 RxData4 RxData5 RxData6 RxData7	O, TS	**Receive Data - Ports 0-7**. These serial output streams provide data received from the network. The LXT9785/9785E drives the data out synchronously to REFCLK.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Tri-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode.
3. RxData[0:7] outputs are tri-stated in Isolation and H/W Power-Down modes, and during H/W reset.

Table 7. LXT9785/9785E SS-SMII Specific Signal Descriptions

Pin/Ball Designation		Symbol	Type[1]	Signal Description[2,3]
PQFP	PBGA			
35 204	A6, C16	TxSYNC0 TxSYNC1	I, ID	**SS-SMII Transmit Synchronization.** The MAC must generate a TxSYNC pulse every 10 TxCLK cycles to mark the start of TxData segments. TxSYNC0 is used when 1x8 port sectionalization is selected.
58 17	E4, B12	RxSYNC0 RxSYNC1	O, TS, ID	**SS-SMII Receive Synchronization.** The LXT9785/9785E generates these pulses every 10 RxCLK cycles to mark the start of RxData segments for the MAC. RxSYNC1 is used and RxSYNC0 is tri-stated when 1x8 port sectionalization is selected. These outputs are only enabled when SS-SMII mode is enabled.
32 201	C8, D17	TxCLK0 TxCLK1	I, ID	**SS-SMII Transmit Clock**. The MAC sources this 125 MHz clock as the timing reference for TxData and TxSYNC. Only TxCLK0 is used when 1x8 port sectionalization is selected. *See "Clock/SYNC Requirements" on page 58 for detailed clock requirements*.
60 21	E3, B11	RxCLK0 RxCLK1	O, TS, ID	**SS-SMII Receive Clock**. The LXT9785/9785E generates these clocks, based on REFCLK, to provide a timing reference for RxData and RxSYNC to the MAC. RxCLK1 used and RxCLK0 is tri-stated when 1x8 port sectionalization is selected. *See "Clock/SYNC Requirements" on page 58 for detailed clock requirements.* These outputs are only enabled when SS-SMII mode is enabled.
54 45 36 27 15 7 205 197	B1, B4, C7, B9, C12, B15, B17, F14	RxData0 RxData1 RxData2 RxData3 RxData4 RxData5 RxData6 RxData7	O, TS, ID	**Receive Data - Ports 0-7**. These serial output streams provide data received from the network. The LXT9785/9785E drives the data out synchronously to REFCLK.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Tri-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode. If a Pin is an output or an I/O, the IP/ID resistors are also disabled when the output is enabled.
3. RxData[0:7], RxSYNC[0:1], and RxCLK[0:1] outputs are tri-stated in Isolation and H/W Power-Down modes, and during H/W reset.

Table 8. MDIO Control Interface Signals

Pin/Ball Designation		Symbol	Type[1]	Signal Description[2,3,4]
PQFP	PBGA			
64 25	F3, A10	MDIO0 MDIO1	I/O, TS, SL, IP	**Management Data Input/Output**. Bidirectional serial data channel for communication between the PHY and MAC or switch ASIC. Only MDIO0 is used when 1x8 port sectionalization is selected. In 2x4 port sectionalization mode, MDIO0 accesses ports 0-3 and MDIO1 accesses ports 4-7. Refer to Figure 22 on page 72.
67 26	F1, C9	$\overline{\text{MDINT0}}$ $\overline{\text{MDINT1}}$	OD,TS, SL, IP	**Management Data Interrupt**. When Register bit 18.1 = 1, an active Low output on this pin indicates status change. Only $\overline{\text{MDINT0}}$ is used when 1x8 port sectionalization is selected. In 2x4 port sectionalization mode, $\overline{\text{MDINT0}}$ is associated with ports 0-3 and $\overline{\text{MDINT1}}$ is associated with ports 4-7. Refer to Figure 22 on page 72.
63 24	E1, B10	MDC0 MDC1	I, ST, ID	**Management Data Clock**. Clock for the MDIO serial data channel. Maximum frequency is 20 MHz. Only MDC0 is used when 1x8 port sectionalization is selected. In 2x4 port sectionalization mode, MDC0 clocks ports 0-3 register accesses and MDC1 clocks ports 4-7 register accesses. Refer to Figure 22 on page 72.
84	L1	MDDIS	I, ST, ID	**Management Disable**. When MDDIS is tied High, the MDIO port is completely disabled and the Hardware Control Interface pins set their respective bits at power-up and reset. When MDDIS is pulled Low at power-up or reset, via the internal pull-down resistor or by tieing it to ground, the Hardware Control Interface pins control only the initial or “default” values of their respective register bits. After the power-up/reset cycle is complete, bit control reverts to the MDIO serial channel.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Tri-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode. If a Pin is an output or an I/O, the IP/ID resistors are also disabled when the output is enabled.
3. MDIO[0:1] and $\overline{\text{MDINT}}$[0:1] outputs are tri-stated in H/W Power-Down mode and during H/W reset.
4. Supports the 802.3 MDIO register set. Specific bits in the registers are referenced using an “X.Y” notation, where X is the register number (0-32) and Y is the bit number (0-15).

Table 9. LXT9785/9785E Signal Detect

Pin/Ball Designation		Symbol	Type[1]	Signal Description[2,3]
PQFP	PBGA			
95	P1	SD_2P5V	I, ST, ID	**Signal Detect 2.5 Volt Interface.** When the SD interface is at 2.5V, tie this input to VCCPECL. Floating this input or tieing it to GNDPECL indicates that a 3.3V SD interface is being used.
96 97 100 101 161 162 165 166	P2, N4, P3, N5, P15, P16, P17, N17	SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7	I	**Signal Detect - Ports 0-7**. The SD inputs are only applicable for ports set in Fiber mode. When SD is high, the process of searching for receive idles for the purpose of bringing link up is initiated. If SD is Low, link is declared lost.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Tri-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode.
3. Tie SD[0:7] inputs to GNDPECL if unused.

Table 10. LXT9785/9785E Network Interface Signal Descriptions

Pin/Ball Designation		Symbol	Type[1]	Signal Description
PQFP	PBGA			
107, 108 111, 110 121, 122 125, 124 136, 137 140, 139 150, 151 154, 153	T2, U1, T3, R4, T6, U5, U7, T7, T10, R10, T11, U11, T14,U15, R14, T15	TPFOP0, TPFON0 TPFOP1, TPFON1 TPFOP2, TPFON2 TPFOP3, TPFON3 TPFOP4, TPFON4 TPFOP5, TPFON5 TPFOP6, TPFON6 TPFOP7, TPFON7	AO/AI	Twisted-Pair/Fiber Outputs[2], Positive & Negative, Ports 0-7. During 100BASE-TX or 10BASE-T operation, TPFO pins drive 802.3 compliant pulses onto the line. During 100BASE-FX operation, TPFO pins produce differential PECL outputs for fiber transceivers.
104, 105 115, 114 118, 119 129, 128 132, 133 143, 142 146, 147 157, 156	R2, T1, U3, T4, R6, T5, T8, R8, T9, U9, U13, T12, R12, T13, R16, T16	TPFIP0, TPFIN0 TPFIP1, TPFIN1 TPFIP2, TPFIN2 TPFIP3, TPFIN3 TPFIP4, TPFIN4 TPFIP5, TPFIN5 TPFIP6, TPFIN6 TPFIP7, TPFIN7	AI/AO	Twisted-Pair/Fiber Inputs[3], Positive & Negative, Ports 0-7. During 100BASE-TX or 10BASE-T operation, TPFI pins receive differential 100BASE-TX or 10BASE-T signals from the line. During 100BASE-FX operation, TPFI pins receive differential PECL inputs from fiber transceivers.

1. Type Column Coding: AI = Analog Input, AO = Analog Output.
2. Switched to Inputs (see TPFIP/N desc.) when not in Fiber mode and MDIX is not active [i.e., Twisted-Pair, non-crossover MDI mode].
3. Switched to Outputs (see TPFOP/N desc.) when not in Fiber mode and MDIX is not active [i.e., Twisted-Pair, non-crossover MDI mode].

Table 11. LXT9785/9785E JTAG Test Signal Descriptions

Pin/Ball Designation		Symbol	Type[1]	Signal Description[2,3]
PQFP	PBGA			
167	N14	TDI	I, ST, IP	**Test Data Input**. Test data sampled with respect to the rising edge of TCK.
168	N15	TDO	O, TS	**Test Data Output**. Test data driven with respect to the falling edge of TCK.
169	N16	TMS	I, ST, IP	**Test Mode Select**.
170	M16	TCK	I, ST, ID	**Test Clock**. Clock input for JTAG test.
171	M17	TRST	I, ST, IP	**Test Reset**. Reset input for JTAG test.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain, TS = Tri-State-able output, SMT = Schmitt Triggered input, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode. If a pin is an output or an I/O, the IP/ID resistors are also disabled when the output is enabled.
3. TDO output is tri-stated in H/W Power-Down mode and during H/W reset.

Table 12. LXT9785/9785E Miscellaneous Signal Descriptions

<table>
<tr><th colspan="2">Pin/Ball Designation</th><th rowspan="2">Symbol</th><th rowspan="2">Type[1]</th><th rowspan="2">Signal Description[2]</th></tr>
<tr><th>PQFP</th><th>PBGA</th></tr>
<tr><td>94
93</td><td>N3,
M4</td><td>TxSLEW_0
TxSLEW_1</td><td>I, ST, ID</td><td>Tx Output Slew Controls 0 and 1 Defaults.
These pins are read at startup or reset. Their value at that time is used to set the default state of Register bits 27.11:10 for all ports. These register bits can be read and overwritten after startup / reset.
These pins select the TX output slew rate for all ports (rise and fall time) as follows:
<table><tr><th>TxSLEW_1</th><th>TxSLEW_0</th><th>Slew Rate (Rise and Fall Time)</th></tr><tr><td>0</td><td>0</td><td>3.3 ns</td></tr><tr><td>0</td><td>1</td><td>3.6 ns</td></tr><tr><td>1</td><td>0</td><td>3.9 ns</td></tr><tr><td>1</td><td>1</td><td>4.2 ns</td></tr></table></td></tr>
<tr><td>50</td><td>D5</td><td>PAUSE</td><td>I, ID</td><td>Pause Default. This pin is read at startup or reset. Its value at that time is used to set the default state of Register bit 4.10 for all ports. This register bit can be read and overwritten after startup / reset.
When High, the LXT9785/9785E advertises Pause capabilities on all ports during auto-negotiation.
This pin is shared with RMII-RxER1. An external pull-up resistor (see applications section for value) can be used to set Pause active while RxER1 is tri-stated during H/W reset. If no pull-up is used, the default Pause state is set inactive via the internal pull-down resistor.</td></tr>
<tr><td>174</td><td>L14</td><td>PWRDWN</td><td>I, ST, ID</td><td>Power-Down. When High, forces the LXT9785/9785E into global power-down mode.
Pin is not on JTAG chain.</td></tr>
<tr><td>175</td><td>M15</td><td>RESET</td><td>I, ST, IP</td><td>Reset. This active Low input is OR’ed with the control register Reset Register bit 0.15. When held Low, all outputs are forced to inactive state.
Pin is not on JTAG chain.</td></tr>
<tr><td>88
89
90
91
92</td><td>L4,
M2,
M3,
N1,
N2</td><td>ADD_4
ADD_3
ADD_2
ADD_1
ADD_0</td><td>I, ST, ID</td><td>Address <4:0>. Sets base address. Each port adds its port number (starting with 0) to this address to determine its PHY address.
Port 0 Address = Base
Port 1 Address = Base + 1
Port 2 Address = Base + 2
Port 3 Address = Base + 3
Port 4 Address = Base + 4
Port 5 Address = Base + 5
Port 6 Address = Base + 6
Port 7 Address = Base + 7</td></tr>
<tr><td>178
177</td><td>L17,
L16</td><td>MODESEL_1
MODESEL_0</td><td>I, ST, ID</td><td>Mode Select[1:0]
00 = RMII
01 = SMII
10 = SS-SMII
11= Reserved
All ports are configured the same. Interfaces cannot be mixed and must be all RMII, SMII, or SS-SMII.</td></tr>
<tr><td colspan="5">1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Tri-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode.</td></tr>
</table>

Table 12. LXT9785/9785E Miscellaneous Signal Descriptions (Continued)

Pin/Ball Designation		Symbol	Type[1]	Signal Description[2]
PQFP	PBGA			
176	L15	SECTION	I, ST, ID	Sectionalization Select. This pin selects sectionalization into separate ports. 0 = 1x8 ports, 1 = 2x4 ports
83	K1	AMDIX_EN	I, ST, IP	**Auto-MDIX Enable Default**. This pin is read at startup or reset. Its value at that time is used to set the default state of Register bit 27.9 for all ports. These register bits can be read and overwritten after startup / reset. Refer to Table 16 on page 53. When active (high), automatic MDI crossover (MDIX) (regardless of segmentation) is selected for all ports. When inactive (Low) MDIX is selected according to the MDIX pin.
59	D2	MDIX	I, ID	**MDIX Select Default.** This pin is read at startup or reset. Its value at that time is used to set the default state of Register bit 27.8 for all ports. These register bits can be read and overwritten after startup / reset. Refer to Table 16 on page 53. When AMDIX_EN is active this pin is ignored. When AMDIX_EN is inactive, all ports are forced to the MDI or the MDIX function regardless of segmentation. If this pin is active (high), MDI crossover (MDIX) is selected. If this pin is inactive, non-crossover MDI mode is set. This pin is shared with RMII-RxER0. An external pull-up resistor (see applications section for value) can be used to set MDIX active while RxER0 is tri-stated during H/W reset. If no pull-up is used, the default MDIX state is set inactive via the internal pull-down resistor. Do not tie this pin directly to VCCIO (vs. using a pull-up) in non-RMII modes.
85 86 87	L2, L3, M1	CFG_3 CFG_2 CFG_1	I, ST, ID	**Global Port Configuration Defaults 1-3.** These pins are read at startup or reset. Their value at that time is used to set the default state of register bits shown in Table 18 on page 62 for all ports. These register bits can be read and overwritten after startup/reset. When operating in Hardware Control Mode, these pins provide configuration control options for all the ports (refer to page 62 for details).
173	M14	G_FX/$\overline{\text{TP}}$	I, ST, ID	Global FX/$\overline{\text{TP}}$ Enable Default. This pin is read at startup or reset. Its value at that time is used to set the default state of Register bit 16.0 for all ports. These register bits can be read and overwritten after startup / reset. *Refer to "Port Configuration Register (Address 16, Hex 10)" on page 133*. This input selects whether all the ports are defaulted to TP vs. FX mode.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Tri-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode.

Table 13. LXT9785/9785E LED Signal Descriptions

Pin/Ball Designation		Symbol	Type[1]	Signal Description[2,3]
PQFP	PBGA			
82 81 80	K3, K2, J1	LED0_1 LED0_2 LED0_3	OD, TS, SL, IP	**Port 0 LED Drivers 1-3.** These pins drive LED indicators for Port 0. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 71 on page 137 for details).
77 76 75	J4, J3, H1	LED1_1 LED1_2 LED1_3	OD, TS, SL, IP	**Port 1 LED Drivers 1-3.** These pins drive LED indicators for Port 1. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 71 on page 137 for details).
73 72 71	H2, H3, G1	LED2_1 LED2_2 LED2_3	OD, TS, SL, IP	**Port 2 LED Drivers 1-3.** These pins drive LED indicators for Port 2. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 71 on page 137 for details).
70 69 68	F2, G3, G4	LED3_1 LED3_2 LED3_3	OD, TS, SL, IP	**Port 3 LED Drivers 1-3.** These pins drive LED indicators for Port 3. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 71 on page 137 for details).
180 181 182	K16, K17, J17	LED4_1 LED4_2 LED4_3	OD, TS, SL, IP	**Port 4 LED Drivers 1-3.** These pins drive LED indicators for Port 4. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 71 on page 137 for details).
185 186 187	J15, J16, H17	LED5_1 LED5_2 LED5_3	OD, TS, SL, IP	**Port 5 LED Drivers 1-3.** These pins drive LED indicators for Port 5. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 71 on page 137 for details).
189 190 191	H15, H16, G17	LED6_1 LED6_2 LED6_3	OD, TS, SL, IP	**Port 6 LED Drivers 1-3.** These pins drive LED indicators for Port 6. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 71 on page 137 for details).
192 193 194	G15, F17, F16	LED7_1 LED7_2 LED7_3	OD, TS, SL, IP	**Port 7 LED Drivers 1-3.** These pins drive LED indicators for Port 7. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 71 on page 137 for details).

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Tri-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode. If a pin is an output or an I/O, the IP/ID resistors are also disabled when the output is enabled.
3. The LED outputs are tri-stated in H/W Power-Down mode and during H/W reset.

Table 14. LXT9785/9785E Power Supply Signal Descriptions

Pin/Ball Designation		Symbol	Type	Signal Description
PQFP	PBGA			
65, 78, 184, 196	G13, J14, F5, J5	VCCD	-	**Digital Power Supply - Core.** +2.5V supply for core digital circuits.
18, 29, 47, 56, 208	A2, A8, C1, C11, D14	VCCIO	-	**Digital Power Supply - I/O Ring.** +2.5/3.3V supply for digital I/O circuits. The digital input circuits running off of this rail, having a TTL-level threshold and over-voltage protection, may be interfaced with 3.3/5.0V, when the IO supply is 3.3V, and 2.5/3.3/5.0V when 2.5V.
98, 164	L13, L5	VCCPECL	-	**Digital Power Supply - PECL Signal Detect Inputs.** +2.5/3.3V supply for PECL Signal Detect input circuits. If Fiber Mode is not used, tie these pins to GNDPECL to save power.
103, 116, 117, 130, 131, 144, 145, 158	N13, P4, P7, P8, P9, P10, P11, P12	VCCR	-	**Analog Power Supply - Receive.** +2.5V supply for all analog receive circuits.
109, 123, 138, 152	N6, N7, N9, N11, N12	VCCT	-	**Analog Power Supply - Transmit.** +2.5V supply for all analog transmit circuits.
66, 79, 183, 195	A1, A9, B3, B7, C5, C13, C17, D1, D3, D6, D10, D15, E5, E7, E9, E11, E13, E17, F13, H8, H9, H10, J8, J9, J10, K8, K9, K10	GNDD	-	**Digital Ground**. Ground return for core digital supplies (VCCD). All ground pins can be tied together using a single ground plane.
9, 19, 30, 38, 48, 57, 74, 188, 199, 207		GNDIO	-	**Digital GND - I/O Ring.** Ground return for digital I/O circuits (VCCIO).
99, 163	M5, M13	GNDPECL	-	**Digital GND - PECL Signal Detect Inputs.** Ground return for PECL Signal Detect input circuits.
106, 112, 120, 126, 135, 141, 149, 155	P5, P6, P13, R7, R9, R11, R13, U8	GNDR	-	**Analog Ground - Receive**. Ground return for receive analog supply. All ground pins can be tied together using a single ground plane.
113, 127, 134, 148	P14, R1, R3, R5, R15, R17, T17, U2, U4, U6, U10, U12, U14, U16, U17	GNDT	-	**Analog Ground - Transmit**. Ground return for transmit analog supply. All ground pins can be tied together using a single ground plane.
179	K14	SGND	-	**Substrate Ground**. Ground for chip substrate. All ground pins can be tied together using a single ground plane.

Table 15. Unused / Reserved Pins

Pin/Ball Designation		Symbol	Type[1]	Signal Description
PQFP	PBGA			
N/C	F15, G2, G5, G14, G16, H4, H14, J2, J13, K4, K15	N/C		No Connection.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Tri-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.

2.0 Functional Description

2.1 Introduction

The LXT9785/9785E is an 8-port Fast Ethernet 10/100 PHY transceiver that supports 10 Mbps and 100 Mbps networks, complying with all applicable requirements of IEEE 802.3 standards. The device incorporates a Serial Media Independent Interface (SMII), Source Synchronous-Serial Media Independent Interface (SS-SMII), and a Reduced Serial Independent Interface (RMII) to enable each individual network port to interface with multiple 10/100 MACs. Each port directly drives either a 100BASE-TX line or a 10BASE-T line. The LXT9785/9785E also supports 100BASE-FX operation via a Pseudo-ECL (PECL) interface. The device has a 241-pin BGA or a 208-pin QFP package.

Unless otherwise noted, all information in this document applies to both the LXT9785 and LXT9785E.

2.1.1 OSP™ Architecture

The Intel LXT9785/9785E incorporates high-efficiency Optimal Signal Processing™ design techniques, combining the best properties of digital and analog signal processing to produce a truly optimal device.

The receiver utilizes decision feedback equalization to increase noise and cross-talk immunity by as much as 3 dB over an ideal all-analog equalizer. Using OSP mixed-signal processing techniques in the receive equalizer avoids the quantization noise and calculation truncation errors found in traditional DSP-based receivers (typically complex DSP engines with A/D converters). The result is improved receiver noise and cross-talk performance.

The OSP architecture also requires substantially less computational logic than traditional DSP-based designs. The result is lower power consumption and reduced logic switching noise generated by DSP engines clocked at speeds up to 125 MHz. The logic switching noise can be a considerable source of EMI when generated from the device's power supplies.

The OSP-based LXT9785/9785E provides improved data recovery, EMI performance and power consumption.

2.1.2 Comprehensive Functionality

The LXT9785/9785E performs all functions of the Physical Coding Sublayer (PCS) and Physical Media Attachment (PMA) sublayer as defined in the IEEE 802.3 100BASE-X specification. This device also performs all functions of the Physical Media Dependent (PMD) sublayer for 100BASE-TX connections.

On power-up, the LXT9785/9785E reads its configuration inputs to check for forced operation settings. If not configured for forced operation, each port uses auto-negotiation/parallel detection to automatically determine line operating conditions. If the PHY device on the other side of the link supports auto-negotiation, the LXT9785/9785E auto-negotiates with it using Fast Link Pulse (FLP) Bursts. If the PHY partner does not support auto-negotiation, the LXT9785/9785E automatically detects the presence of either link pulses (10 Mbps PHY) or Idle symbols (100 Mbps PHY) and set its operating conditions accordingly.

The LXT9785/9785E provides half-duplex and full-duplex operation at 100 Mbps and 10 Mbps.

2.1.2.1 Sectionalization

The LXT9785/9785E's sectional design allows flexibility with large multiport MACs and ASICs. With the use of the Section pin, the LXT9785/9785E can be configured into a single 8-port or two separate 4-port sections, each with its own MDIO (with separate MDC clock) and MII data (with separate REFCLK/TxCLK/RxCLK clocks) interfaces. See Figure 17 on page 66, Figure 22 on page 72, and Figure 27 on page 77.

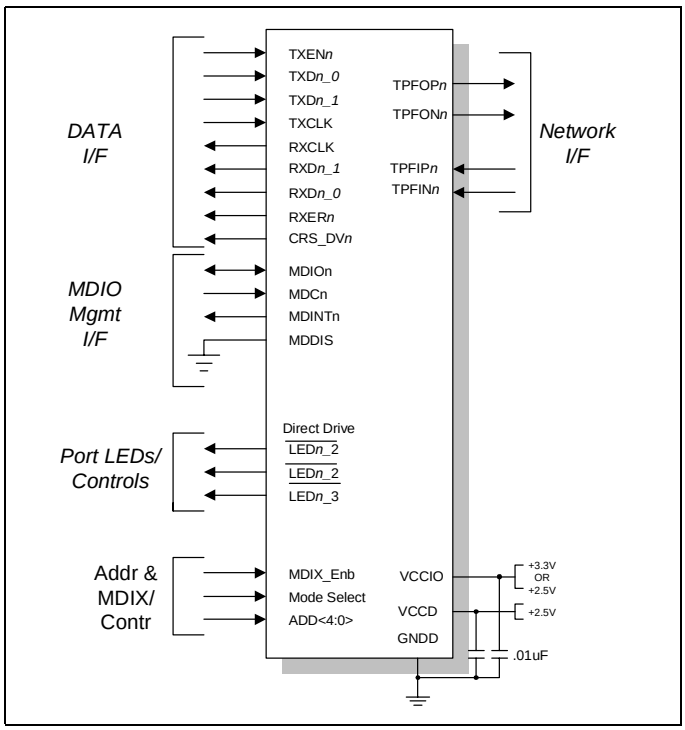
2.2 Interface Descriptions

2.2.1 10/100 Network Interface

The LXT9785/9785E supports 10 Mbps and 100 Mbps (10BASE-T and 100BASE-TX) Ethernet over twisted-pair, or 100 Mbps (100BASE-FX) Ethernet over fiber media. Each network interface port consists of four external pins (two differential signal pairs). The pins are shared between twisted-pair (TP) and fiber. The LXT9785/9785E pinout is designed to interface seamlessly with dual-high stacked RJ-45 connectors. Refer to Table 10 on page 44 for specific pin assignments.

The LXT9785/9785E output drivers generate either 100BASE-TX, 10BASE-T, or 100BASE-FX output. When not transmitting data, the device generates IEEE 802.3-compliant link pulses or Idle code. Input signals are decoded either as a 100BASE-TX, 100BASE-FX, or 10BASE-T input, depending on the mode selected. Auto-negotiation/parallel detection or manual control is used to determine the speed of this interface.

Figure 8. LXT9785/9785E Interfaces



2.2.1.1 Twisted-Pair Interface

The LXT9785/9785E supports either 100BASE-TX or 10BASE-T connections over 100Ω, Category 5, Unshielded Twisted-Pair (UTP). Only a transformer, RJ-45, and bypass capacitors are required to complete this interface. Using Intel's patented waveshaping technology, the transmitter shapes the outgoing signal to help reduce the need for external EMI filters. Four slew rate settings (refer to Table 12 on page 46) allow the designer to match the output waveform to the magnetic characteristics. Both transmit and receive terminations are built into the LXT9785/9785E so no external components are required between the LXT9785/9785E and the external transformer. The transmitter uses a transformer with a center tap to help reduce power consumption.

When operating at 100 Mbps, MLT3 symbols are continuously transmitted and received. When not transmitting data, the LXT9785/9785E generates "IDLE" symbols.

During 10 Mbps operation, LXT9785/9785E encoded data is exchanged. When no data are being exchanged, the line is left in an idle state with NLPs transmitted to maintain link.

2.2.1.2 MDI Crossover (MDIX)

The LXT9785/9785E crossover function, which is compliant to the IEEE 802.3, clause 23 standard, connects the transmit output of the device to the far-end receiver in a link segment. This function can be disabled via Register bit 27.9:8 or by using the hardware configuration pins.

Table 16. MDIX Selection

AMDIX_EN	MDIX	MDIX Mode
0	0	MDI forced
0	1	MDIX forced
1	X	Auto-MDIX

2.2.1.3 Fiber Interface

The LXT9785/9785E provides a PECL interface that complies with the ANSI X3.166 specification. This interface is suitable for driving a fiber-optic coupler (see Figure 37 on page 99).

Fiber ports cannot be enabled via auto-negotiation and must be enabled via the Global Hardware Control Interface pins or MDIO registers. All ports are selected for fiber or twisted-pair when configured via hardware, and can only be intermixed via software. Using external circuitry, the LXT9785/9785E can interface the fiber transceiver with 2.5V, 3.3V, or 5V supply voltages. Fiber mode per port may be selected using Register bit 16.0. Please refer to Table 10 on page 44 for correct pin assignments.

2.3 Media Independent Interface (MII) Interfaces

The LXT9785/9785E supports Reduced MII or Serial MII, but not concurrently. The interface mode selection pins configures the device for either RMII or SMII/SS-SMII on all eight ports. Refer to Table 17 for the mode select settings.

2.3.1 Global MII Mode Select

The mode select pins are used for MII interface configuration settings upon power-up sequencing. All ports are configured the same and cannot be intermixed.

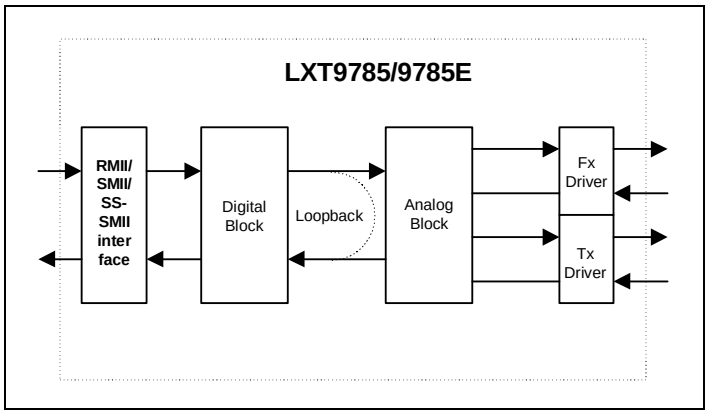
Table 17. MII Mode Select

	ModeSel1	ModeSel0
RMII	0	0
SMII	0	1
SS-SMII	1	0
Reserved	1	1

2.3.2 Internal Loopback

A test loopback function is available for 10 Mbps and 100 Mbps mode testing. Register bits 0.8, 0.13, and 0.14 must be set to 1 for correct operation. When data is looped back, whatever the MAC transmits is looped back in its entirety, including the preamble.

Figure 9. Internal Loopback



2.3.3 RMII Data Interface

The LXT9785/9785E provides a separate RMII for each network port, each complying with the RMII standard. The RMII includes both a data interface and an MDIO management interface. The RMII Data Interface exchanges data between the LXT9785/9785E and up to eight Media Access Controllers (MACs).

2.3.4 Serial Media Independent Interface (SMII) and Source Synchronous-Serial Media Independent Interface (SS-SMII)

2.3.4.1 SMII Interface

The LXT9785/9785E provides an independent serial interface for each network port. All SMII ports use a common reference clock and SYNC signal. The SMII Data Interface exchanges data between the LXT9785/9785E and multiple Media Access Controllers (MACs). All signals are

synchronous to the reference clock. One SYNC control stream is sourced by the MAC to the PHY. Both the transmit and receive data streams are segmented into boundaries delimited by the SYNC pulses. This interface is expected to drive up to 6 inches of trace lengths.

2.3.4.2 Source Synchronous-Serial Media Independent Interface

The new revision to the SMII interface, SS-SMII, allows for a longer trace length and helps to relieve timing constraints, requiring the addition of four new signals, TxCLK, TxSYNC, RxCLK, and RxSYNC. The transmit TxCLK and TxSYNC are sourced from the MAC to the PHY and referenced to the REFCLK input. The receive RxCLK and RxSYNC are sourced by the PHY to the MAC and in reference to the REFCLK.

2.3.5 Configuration Management Interface

The LXT9785/9785E provides an MDIO Management Interface and a Hardware Control Interface (via the CFG pins) for device configuration and management. Mode control selection is provided via the MDDIS pin as shown in Table 8 on page 43. When sectionalization (2x4) is selected, separate MDIO interfaces are enabled (see Figure 14 on page 60).

2.3.6 MII Isolate

In applications where the MII needs to be isolated from the bus, the RMII and the SMII/SS-SMII configurations can be tri-stated using Register 0.10. Ports 0 and 1 control RxCLK0, RxCLK1, RxSYNC0, and RxSYNC1. When 2x4 sectionalization is selected, ports 1-3 and 5-7 can be individually port isolated. For global shut down, Ports 0 and 1 must be isolated to control the RxCLK*n* and RxSYNC*n* synchronization pins. If ports 0 and 1 are individually set to isolate, the remaining associated quad sectionalization ports must also be set to isolate.

2.3.6.1 MDIO Management Interface

The LXT9785/9785E supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input/Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the LXT9785/9785E. The MDIO interface consists of a physical connection, a specific protocol that runs across the connection, and an internal set of addressable registers. Some registers are required and their functions are defined by the IEEE 802.3 specification. Additional registers allow for expanded functionality. Specific bits in the registers are referenced using an “X.Y” notation, where X is the register number (0-32) and Y is the bit number (0-15).

The physical interface consists of a data line (MDIO) and clock line (MDC). Operation of this interface is controlled by the MDDIS input pin. When MDDIS is High, all the MDIOs are completely disabled. The Hardware Control Interface provides primary configuration control. When MDDIS is Low, the MDIO port is enabled for both read and write operations and the Hardware Control Interface is not used. The timing for the MDIO Interface is shown in Table 54 on page 123. MDIO read and (write) cycles are shown in Figure 10 (read) and Figure 11 (write) on page 56.

Figure 10. Management Interface Read Frame Structure

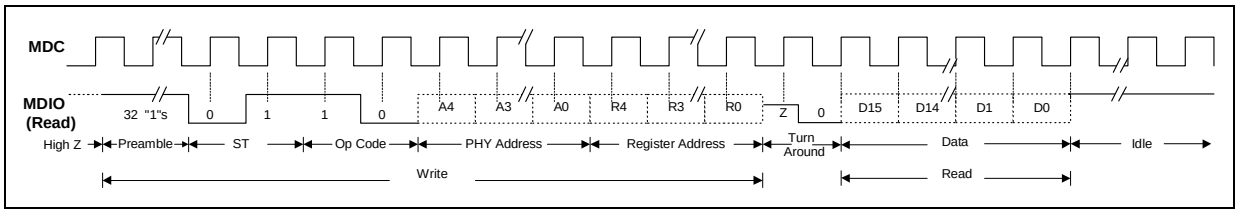
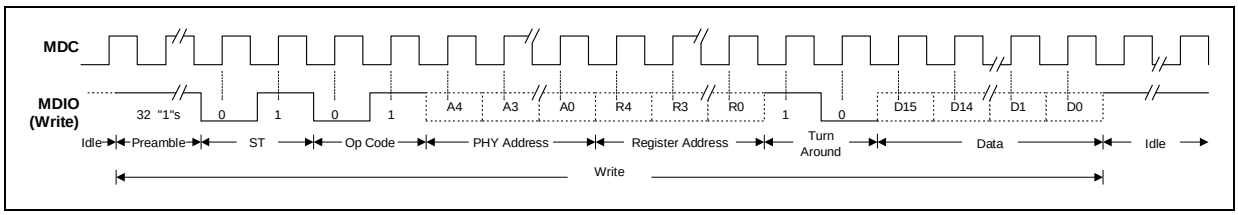
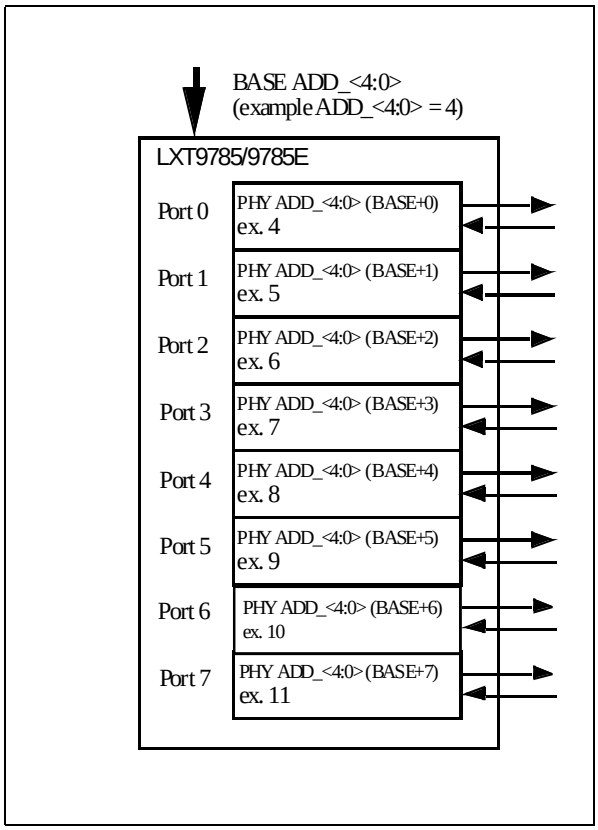


Figure 11. Management Interface Write Frame Structure



The protocol allows one controller to communicate with multiple LXT9785/9785E chips. Pins ADD_<4:0> determine the base address. Each port adds its port number to the base address to obtain its port address as shown in Figure 12.

Figure 12. Port Address Scheme



2.3.6.2 MII Sectionalization

When sectionalized into two quad sections, the MDIO bus splits into two separate PHY access ports. Ports 0-3 of the MDIO section operate independently of ports 4-7. The MII isolate function is unaffected and operates normally. Sectionalization is selected by pulling pin 176 (Section) High on the initial power-up sequence (refer to Figure 14). In applications that need sectionalization, such as 1x8 and 2x4 and have a single MDIO bus structure, it is necessary that the addressing scheme be contiguous. For example, the first eight ports are addressed 0-7, so the next four ports must be addressed 8-11.

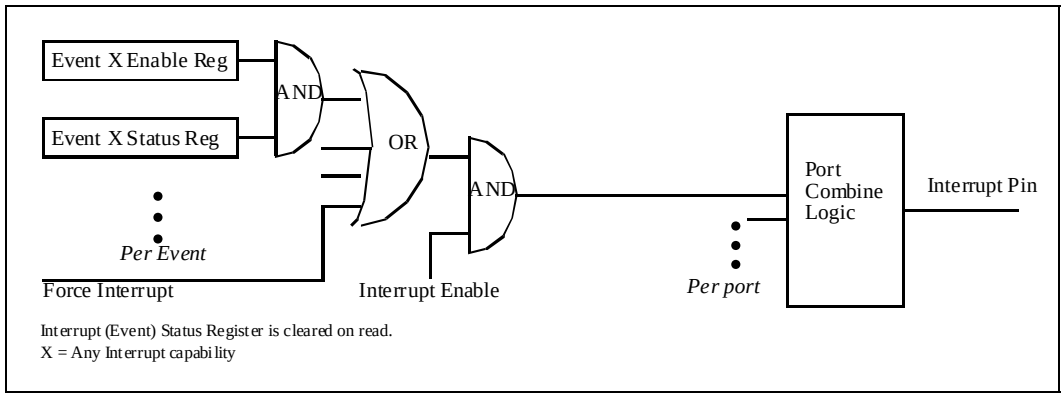
2.3.6.3 MII Interrupts

The LXT9785/9785E provides a single per-section interrupt pin that is available to all ports. Interrupt logic is shown in Figure 13. The LXT9785/9785E also provides two dedicated interrupt registers for each port. Register 18 provides interrupt enable and mask functions and Register 19 provides interrupt status. Setting Register bit 18.1 = 1 enables a port to request interrupt via the $\overline{\text{MDINT}}$ pin. An active Low on this pin indicates a status change on the device. Because it is a shared interrupt, there is no indication which port is requesting interrupt service (see Figure 13).

There are five conditions that may cause an interrupt:

- Auto-negotiation complete.
- Speed status change.
- Duplex status change.
- Link status change.
- Isolate status change.

Figure 13. Interrupt Logic



2.3.6.4 Global Hardware Control Interface

The LXT9785/9785E provides a Hardware Control Interface for applications where the MDIO is not desired. Refer to "Initialization" on page 59 for additional details.

2.4 Operating Requirements

2.4.1 Power Requirements

The LXT9785/9785E requires four power supply inputs: VCCD, VCCA, VCCPECL and VCCIO. The digital and analog circuits require 2.5V supplies (VCCD, VCCR, and VCCT). These inputs may be supplied from a single source although decoupling is required to each respective ground. The fiber VCCPECL supply can be connected to either 2.5V or 3.3V.

A separate power supply may be used for the MII, JTAG and MDIO (VCCIO) interfaces. The power supply may be either +2.5V or +3.3V. VCCIO should be supplied from the same power source used to supply the controller on the other side of the interface. Refer to Table 29 and Table 30 on page 102 for I/O characteristics.

As a matter of good practice, these supplies should be as clean as possible. Typical filtering and decoupling are shown in Figure 35 on page 98.

2.4.2 Clock/SYNC Requirements

2.4.2.1 Reference Clock

The LXT9785/9785E requires a constant enabled reference clock (REFCLK). REFCLK's frequency must be 50 MHz for RMII or 125 MHz for SMII/SS-SMII. The reference clock is used to generate transmit signals and recover receive signals. A crystal-based clock is recommended over a derived clock (i.e., PLL-based) to minimize transmit jitter. Refer to Table 31 on page 102 for clock timing requirements.

For applications that use a single 8-port sectionalization, REFCLK0 and REFCLK1 must always be tied together and to the source. In 2x4 applications, REFCLK0 and REFCLK1 are not tied together.

2.4.2.2 TxCLK Signal (SS-SMII only)

The LXT9785/9785E requires a 125 MHz input transmit clock synchronous with TxData*n* and frequency locked to REFCLK. See Figure 23 on page 73.

2.4.2.3 TxSYNC Signal (SMII/SS-SMII)

The LXT9785/9785E requires a 12.5 MHz input pulse for SMII synchronization. See Figure 23 on page 73.

2.4.2.4 RxSYNC Signal (SS-SMII only)

The LXT9785/9785E provides a 12.5 MHz output pulse synchronous with the RxData*n* outputs. See Figure 24 on page 73.

2.4.2.5 RxCLK Signal (SS-SMII only)

In SMII mode, the LXT9785/9785E provides a 125 MHz clock output in reference to the output RxData*n*. RxCLK is referenced and synchronized to the REFCLK. See Figure 24 on page 73.

2.5 Initialization

When the LXT9785/9785E is first powered on, reset, or encounters a link failure state, it checks the MDIO register configuration bits to determine the line speed and operating conditions to use for the network link. The configuration bits may be set by the Hardware Control or MDIO interface as shown in Figure 14 on page 60.

2.5.1 MDIO Control Mode

In the MDIO Control mode, the LXT9785/9785E reads the Hardware Control Interface pins to set the initial (default) values of the MDIO registers. Once the initial values are set, bit control reverts to the MDIO interface.

2.5.2 Hardware Control Mode

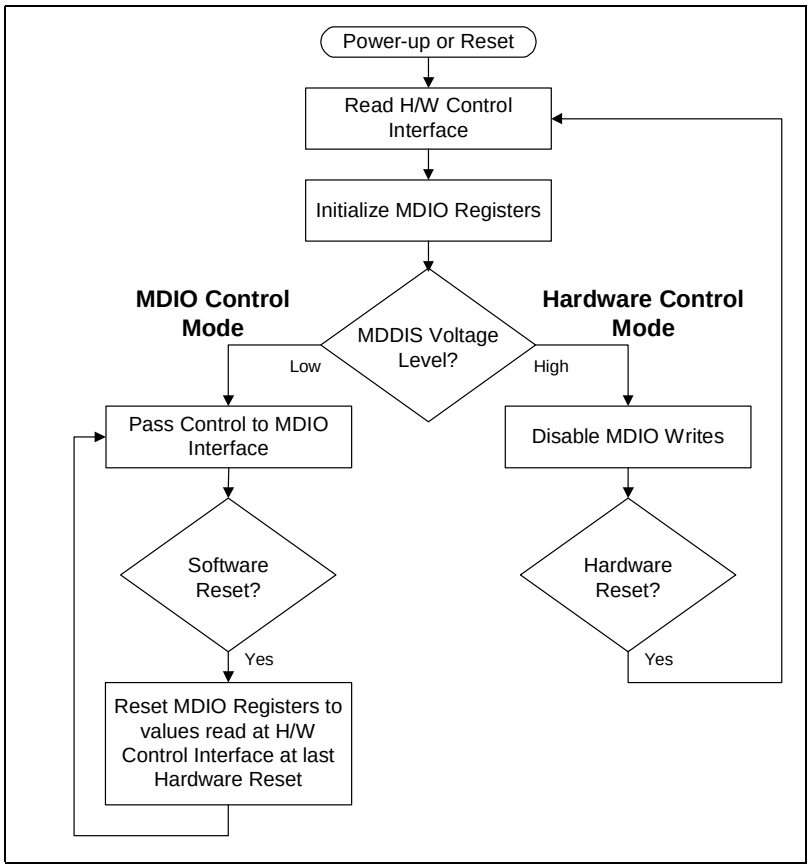
In the Hardware Control Mode, the LXT9785/9785E disables direct write operations to the MDIO registers via the MDIO Interface. On power-up or hardware reset, the LXT9785/9785E reads the Hardware Control Interface pins and sets the MDIO registers accordingly.

The following modes are available using either Hardware Control or MDIO Control:

- Force network link to 100BASE-FX (Fiber).
- Force network link operation to:
  - 100BASE-TX, Full-Duplex
  - 100BASE-TX, Half-Duplex
  - 10BASE-T, Full-Duplex
  - 10BASE-T, Half-Duplex
- Allow auto-negotiation/parallel-detection.
- Auto/Manual MDIX enable/disable.
- Pause for full duplex links operation.
- Global Output Slew Rate Control.

When the network link is forced to a specific configuration, the LXT9785/9785E immediately begins operating the network interface as commanded. When auto-negotiation is enabled, the LXT9785/9785E begins the auto-negotiation/ parallel-detection operation.

Figure 14. Initialization Sequence



2.5.3 Power-Down Mode

The LXT9785/9785E incorporates numerous features to maintain the lowest power possible. The device can be put into a low-power state via Register 0 as well as a near-zero power state with the power down pin. When in power-down mode, the device is not capable of receiving or transmitting packets.

The lowest power operation is achieved using the Global power-down pin, which is active High. This pin powers down every circuit in the device, including all clocks. All registers are unaltered and maintained when the Global PWRDWN pin is released.

Individual ports (software power down) can be powered down using Register bit 0.11. This bit powers down a significant portion of the port, but clocks to the register section remain active. This allows the management interface to remain active during register power-down. The power-down bit is active High.

2.5.3.1 Global (Hardware) Power Down

The global power-down mode is controlled by the PWRDWN pin. When PWRDWN is High, the following conditions are true:

- All LXT9785/9785E ports and the clock are shut down.

- All outputs are tri-stated.
- All weak pad pull-up and pull-down resistors are disabled.
- The MDIO registers are not accessible.
- Configuration pins are not read upon release of the PWRDWN pin, and registers are reloaded with the value of the last Hardware reset.

2.5.3.2 Port (Software) Power Down

Individual port power-down control is provided by Register bit 0.11 in the respective port Control Registers (refer to Table 58 on page 126). During individual port power-down, the following conditions are true:

- The individual port is shut down.
- The MDIO registers remain accessible.
- Pull-up and pull-down resisters are not affected and the outputs are not tri-stated.
- The register remains unchanged.

2.5.4 Reset

The LXT9785/9785E provides both hardware and software resets. Configuration control of Auto-Negotiation, speed, and duplex mode selection is handled differently for each. During a hardware reset, settings for Register bits 0.13, 0.12, 0.8, and 4.8:5 are read in from the pins (refer to Table 18 on page 62 for pin settings and Table 58 on page 126 and Table 62 on page 129 for register bit definitions).

During a software reset (Register bit 0.15 = 1), the bit settings are not re-read from the pins and revert back to the values that were read in during the last hardware reset. Any changes to pin values from the last hardware reset is not detected during a software reset.

During a hardware reset, register information is unavailable for 1 ms after de-assertion of the reset. All MII interface pins are disabled during a hardware reset and released to the bus on de-assertion of reset.

During a software reset (Register bit 0.15 = 1) the registers are available for reading. The reset bit should be polled to see when the part has completed reset (Register bit 0.15 = 0). Pull up and pull down resisters are not affected.

2.5.5 Hardware Configuration Settings

The LXT9785/9785E provides a hardware option to set the initial device configuration. The hardware option uses three Global CFG pins that provide control for all ports (see Table 18).

Table 18. Global Hardware Configuration Settings

Desired Mode			CFG Pin Settings[1]			Resulting Register Bit Values						
AutoNeg	Speed	Duplex	1	2	3	0.12	0.13	0.8	4.8	4.7	4.6	4.5
Disabled	10	Half	Low	Low	Low	0	0	0	N/A Auto-Negotiation Advertisement			
		Full	Low	Low	High			1				
	100	Half	Low	High	Low		1	0				
		Full	Low	High	High			1				
Enabled	100	Half	High	Low	Low	1	1	0	0	1	N/A	0
		Full	High	Low	High		1	1	1	1		
	10/100	Half	High	High	Low		1	0	0	1	0	1
		Full	High	High	High		1	1	1	1	1	1

1. Refer to for CFG pin assignments.

2.6 Link Establishment

2.6.1 Auto-Negotiation

The LXT9785/9785E attempts to auto-negotiate with its link partner by sending Fast Link Pulse (FLP) bursts. Each burst consists of 33 link pulses spaced 62.5 µs apart. Odd link pulses (clock pulses) are always present. Even link pulses (data pulses) may also be present or absent to indicate a “1” or a “0”. Each FLP burst exchanges 16 bits of data, referred to as a “page”. All devices that support auto-negotiation must implement the “Base Page”, defined by IEEE 802.3 (registers 4 and 5). The LXT9785/9785E also supports the optional “Next Page” function (Registers 7 and 8).

2.6.1.1 Base Page Exchange

By exchanging Base Pages, the LXT9785/9785E and its link partner communicate their capabilities to each other. Both sides must receive at least three identical base pages for negotiation to proceed. Each side finds their highest common capabilities, exchange more pages, and agree on the operating state of the line.

2.6.1.2 Next Page Exchange

Additional information, exceeding that required by base page exchange, is also sent via “Next Pages.” The LXT9785/9785E fully supports the IEEE 802.3 method of negotiation via Next Page exchange. The Next Page exchange uses Register 7 to send information and Register 8 to receive it. Next Page exchange occurs only if both ends of the link partners advertise their ability to exchange Next Pages. A special mode has been added to make next page exchange easier for software. When Register 6 “page” is received, it stays set until read. This bit should be cleared whenever a new negotiation occurs, preventing the user from reading an old value in Register 6 and assuming there is valid information in Registers 5 and 8. Additionally, Register 6 contains a new bit that indicates

when the current received page is the base page. This information is useful for recognizing when next pages must be resent due to the start of a new negotiation process. Register bit 16.1 and the page received bit are also cleared upon reading Register 6.

2.6.1.3 Controlling Auto-Negotiation

When auto-negotiation is controlled by software, the following steps are recommended:

- After power-up, power-down, or reset, the power-down recovery time, as specified in Table 55 on page 124, must be exhausted before proceeding.
- Set the auto-negotiation advertisement register bits.
- Enable auto-negotiation (set MDIO Register bit 0.12 = 1).

2.6.1.4 Link Criteria

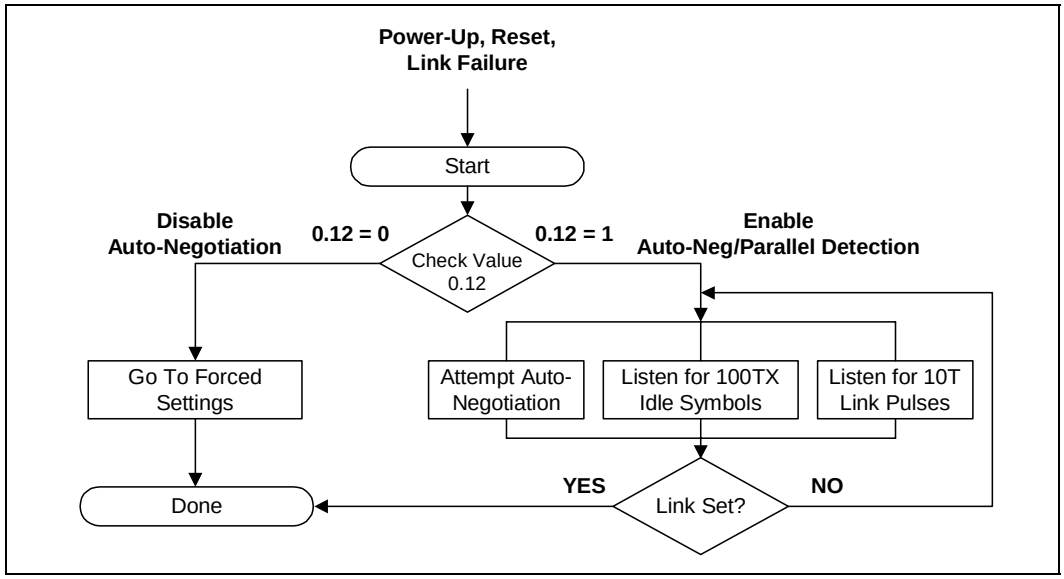
In 100 Mbps mode, link is established when the scrambler becomes locked and remains locked for approximately 50 ms. Link remains up unless the descrambler receives less than 12 consecutive idle symbols in any 2 ms period. This provides a very robust operation, filtering out any small noise hits that may disrupt the link.

In 10 Mbps mode, link is established based on the link state machine found in IEEE 802.3, 14.X. Receiving 100 Mbps idle patterns does not bring up a 10 Mbps link.

2.6.1.5 Parallel Detection

In parallel with auto-negotiation, the LXT9785/9785E also monitors for 10 Mbps Normal Link Pulses (NLP) or 100 Mbps Idle symbols. If either symbol is detected, the device automatically reverts to the corresponding operating mode. Parallel detection allows the LXT9785/9785E to communicate with devices that do not support auto-negotiation.

Figure 15. Auto-Negotiation Operation



2.7 Serial MII Operation

The LXT9785/9785E exchanges transmit and receive data with the controller via the Serial MII (SMII). The SMII performs the following functions:

- Conveys complete MII information between a 10/100 PHY and MAC with two pins per port.
- Allows a multi-port MAC/PHY communication with one system clock.
- Operates in both half-duplex and full duplex.
- Supports per-packet switching between 10 Mbps and 100 Mbps data rates.

The Serial MII operates at 125 MHz using a global reference clock and frame synchronization signal (REFCLK and SYNC). Each port has an individual two-line data interface (TxData*n* and RxData*n*). All signals are synchronous to REFCLK. Table 19 summarizes the SMII signals.

Data is exchanged in 10-bit serial words. Each word contains one data byte (two nibbles of 4B coded data) and two status bits. When the port is operating at 100 Mbps, each word contains a new data byte. When the port is operating at 10 Mbps, each data byte is repeated 10 times.

Table 19. SMII Signal Summary

Signal	To	From	Purpose
TxData	PHY	MAC	Transmit data & control
SYNC	PHY	MAC	Synchronization
RxData	MAC	PHY	Receive data & control
REFCLK	MAC & PHY	System	Synchronization

1. Refer to Table 5 on page 41 for detailed signal descriptions.

Figure 16. Typical SMII Interface Diagram

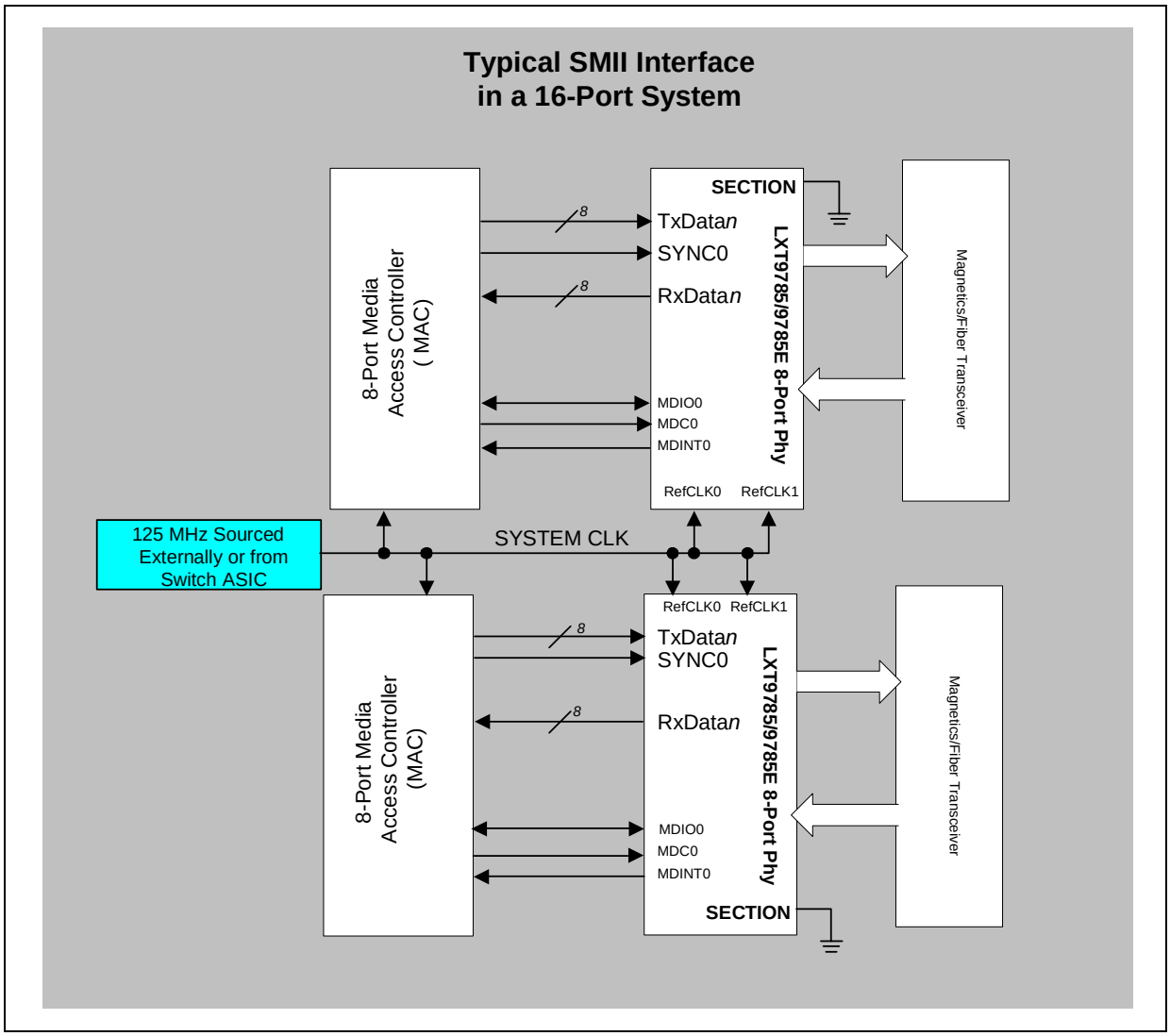


Figure 17. Typical SMII Quad Sectionalization Diagram

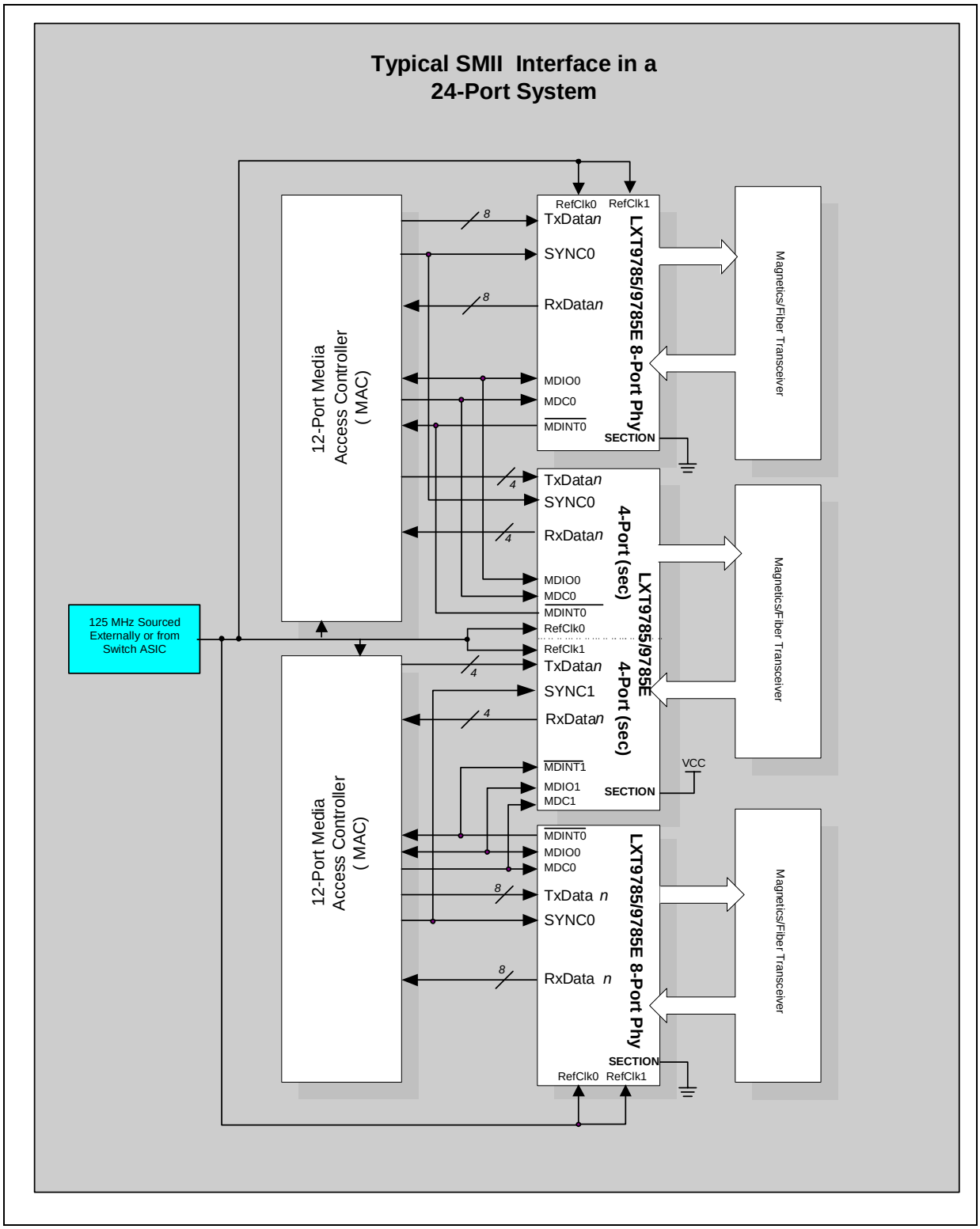
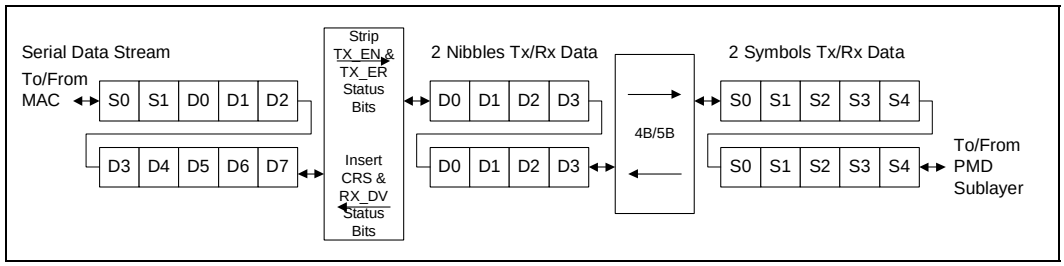


Figure 18. 100 Mbps Serial MII Data Flow



2.7.1 SMII Reference Clock

The REFCLK operates at 125 MHz. The transmit and receive data and control streams must always be synchronized to the REFCLK by the MAC and PHY. The LXT9785/9785E samples these signals on the rising edge of the REFCLK.

2.7.2 TxSYNC Pulse (SMII/SS-SMII)

The TxSYNC pulse delimits segment boundaries and synchronizes with REFCLK. The MAC must continuously generate a TxSYNC pulse once every 10 REFCLK cycles. The TxSYNC pulse signals the start of each new segment (see Figure 22 on page 72).

2.7.3 Transmit Data Stream

Transmit data and control information are signaled in ten-bit segments. In 100 Mbps mode, each segment contains a new byte of data. In 10 Mbps mode, the MAC must repeat a 10M serial word ten times on TxData. The LXT9785/9785E may sample that serial word at any point.

The TxSYNC pulse signals the start of a new segment as shown in Figure 19.

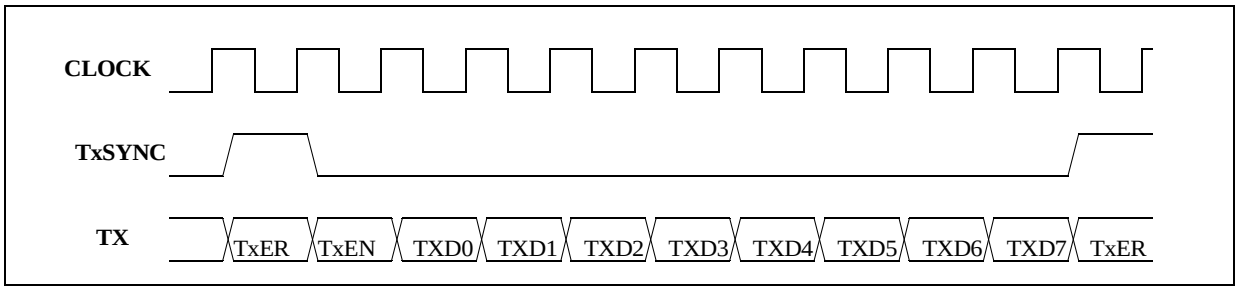
2.7.3.1 Transmit Enable

The MAC must assert the TxEN bit in each segment of TxData, and de-assert TxEN*n* after the last segment of the packet.

2.7.3.2 Transmit Error

When the MAC asserts the TxER bit in 100BASE-X mode, the LXT9785/9785E drives “H” symbols onto the network interface. TxER does not have any function in 10M operation.

Figure 19. Serial MII Transmit Synchronization



2.7.4 Receive Data Stream

Receive data and control information are signalled in ten-bit segments. In 100 Mbps mode, each segment contains a new byte of data. In 10 Mbps mode, each segment is repeated ten times (except for the CRS bit), and the MAC can sample any of the ten segments.

2.7.4.1 Carrier Sense

The CRS bit (slot 0) is generated when a packet is received from the network interface. The CRS bit is set in real time, even in 10 Mbps mode (all other bits are repeated in 10 sequential segments).

2.7.4.2 Receive Data Valid

The LXT9785/9785E asserts the RX_DV bit (slot 1) when it receives a valid packet. The assertion timing changes depending on line operating speed:

- For 100BASE-TX and 100BASE-FX links, the RX_DV bit is asserted from the first nibble of preamble to the last nibble of the data packet.
- For 10BASE-T links, the entire preamble is truncated. The RX_DV bit is asserted with the first nibble of the Start-of-Frame Delimiter (SFD) “5D” and remains asserted until the end of the packet.

2.7.4.3 Receive Error

When the LXT9785/9785E receives an invalid symbol from the network in 100BASE-TX mode, it drives “1110” on the associated RxData pin.

2.7.4.4 Receive Status Encoding

The LXT9785/9785E encodes status information onto the RxData line during IPG as seen in Table 20 on page 69. Status bit RxData<5> indicates the validity of the upper nibble (RxData<7:4> of the last byte of the previous frame). RxData and RX_DV are passed through the internal elasticity FIFO to smooth any clock rate differences between the recovered clock and the 125 MHz reference clock.

2.7.5 Collision

The SMII interface does not provide a collision output and relies on the MAC to interpret COL conditions using CRS and TxEN. CRS is unaffected by the transmit path.

Figure 20. Serial MII Receive Synchronization

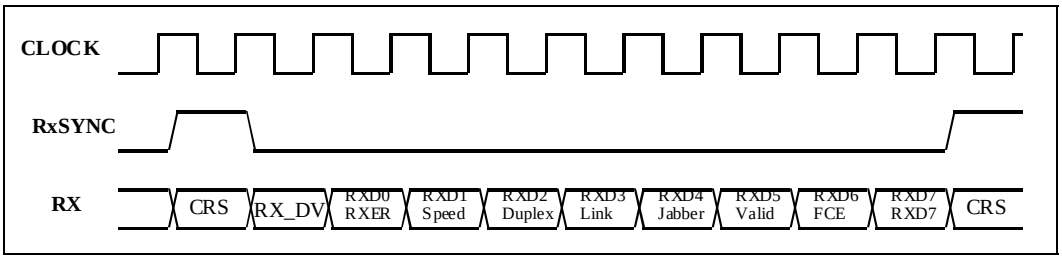


Table 20. RX Status Encoding Bit Definitions

Signal	Definition	
CRS	Carrier Sense - identical to MII, except that it is not an asynchronous signal.	
RxDV	Receive Data Valid - identical to MII. When RX_DV = 0, status information is transmitted to the MAC. When RX_DV = 1, received data is transmitted to the MAC.	0 = Status Byte 1 = Valid Data Byte
RxER (RxData0)	Inter-frame status bit RxData0 indicates whether or not the PHY detected an error somewhere in the previous frame.	0 = No Error 1 = Error
SPEED (RxData1)	Inter-frame status bit RxData1 indicates port operating speed.	0 = 10 Mbps 1 = 100 Mbps
DUPLEX (RxData2)	Inter-frame status bit RxData2 indicates port duplex condition.	0 = Half 1 = Full
LINK (RxData3)	Inter-frame status bit RxData3 indicates port link status.	0 = Down 1 = Up
JABBER (RxData4)	Inter-frame status bit RxData4 indicates port jabber status.	0 = OK 1 = Error
VALID (RxData5)	Inter-frame status bit RxData5 conveys the validity of the upper nibble of the last byte of the previous frame.	0 = Invalid 1 = Valid
False Carrier (RxData6)	Inter-frame status bit RxData6 indicates whether or not the PHY has detected a false carrier event.	0 = No FC detected 1 = FC detected
RxData7	This bit is set to 1.	Always = 1

1. Both RxData0 and RxData5 bits are valid in the segment immediately following a frame, and remain valid until the first data segment of the next frame begins.

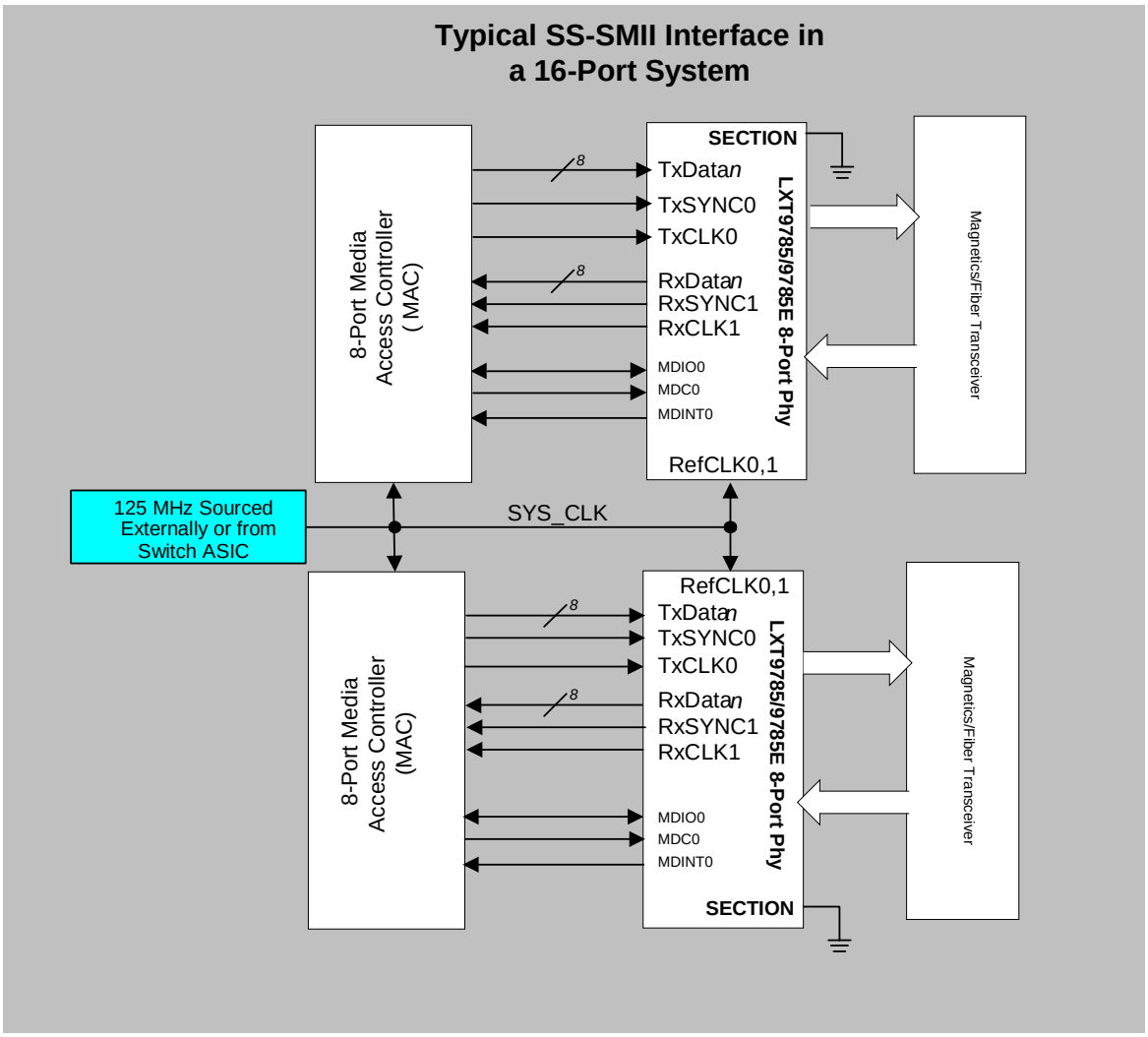
2.7.5.1 Source Synchronous-Serial Media Independent Interface

Some system designs require the PHY to be placed between 3 to 12 inches away from the MAC. A new Source Synchronous-Serial Media Independent Interface (SS-SMII) definition has been added because of this requirement. To provide a source synchronous interface between the PHY and MAC, the PHY must drive the RxCLK and the RxSYNC signals to the MAC. Also, the MAC must drive the TxCLK and the TxSYNC signal to the PHY. The REFCLK is also needed to synchronize the data to the PHY's core clock domain. TxData is clocked in using TxCLK and then synchronized to REFCLK and transmitted to the twisted-pair. The RxData is synchronized to the RxCLK. See Figure 24 on page 73.

Table 21. SS-SMII

Signal	To	From	Purpose
TxData	PHY	MAC	Transmit data & control
TxCLK	PHY	MAC	Transmit clock
TxSYNC	PHY	MAC	Synchronization pulses
RxData	MAC	PHY	Receive data & control
RxCLK	MAC	PHY	Receive clock
RxSYNC	MAC	PHY	Receive Synchronization
REFCLK	MAC	System	Synchronization

Figure 21. Typical SS-SMII Interface Diagram



NOTE: For SMII operation TxCLK1, RxSYNCn and RxCLKn pins are ignored

Figure 22. Typical SS-SMII Quad Sectionalization Diagram

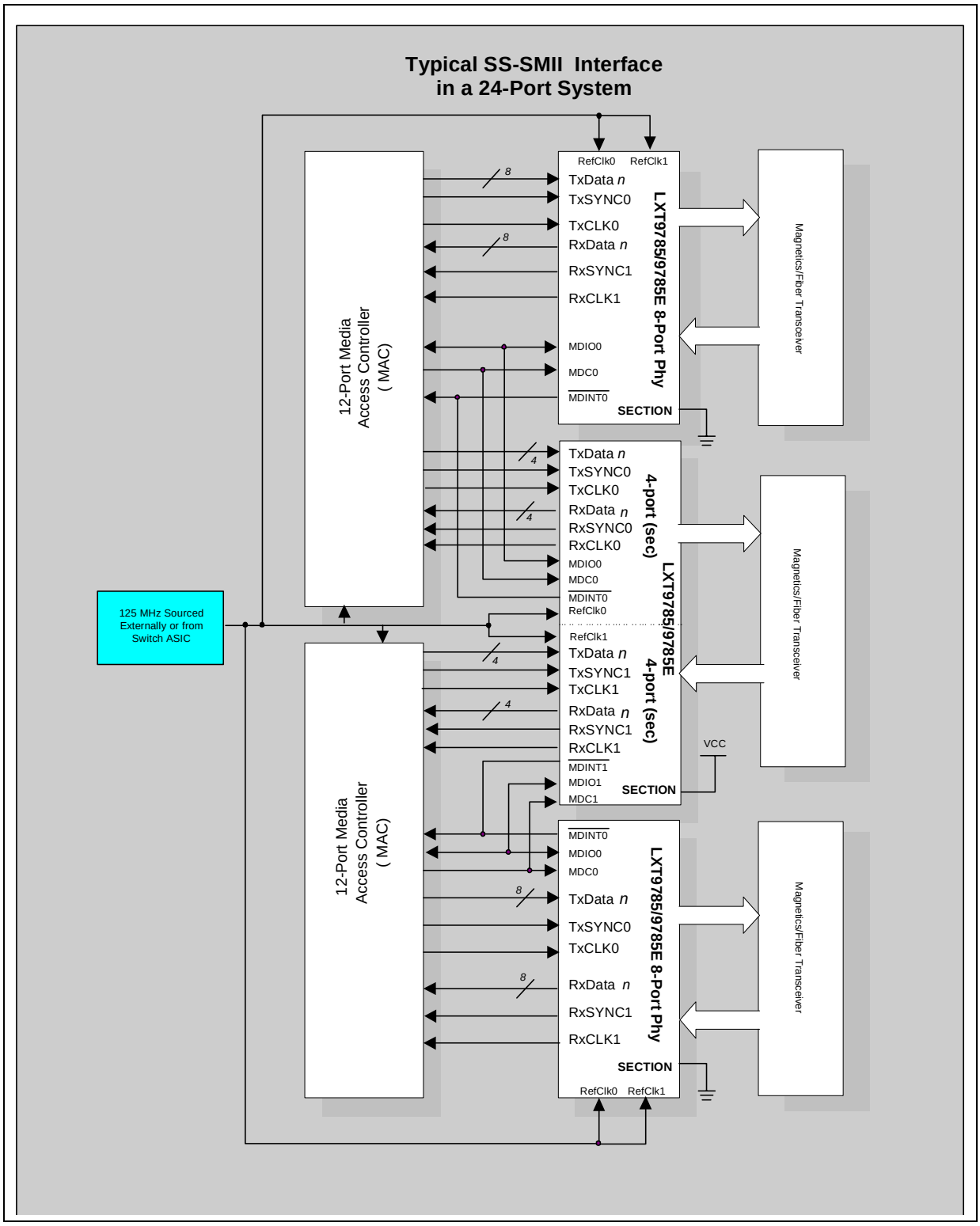


Figure 23. SS-SMII Transmit Timing

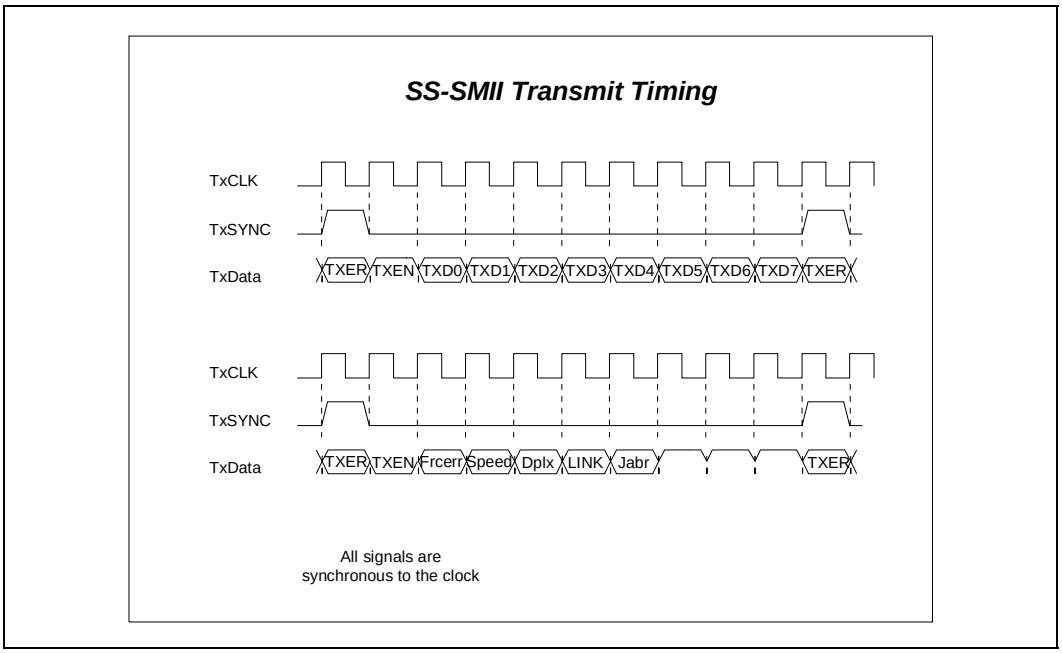
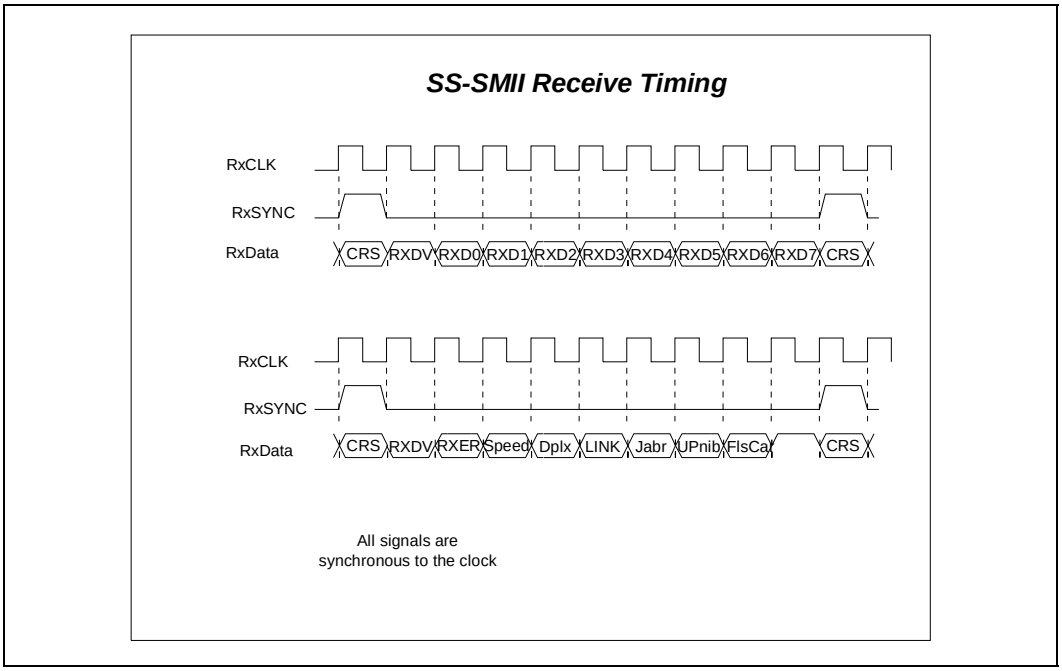


Figure 24. SS-SMII Receive Timing



2.8 RMII Operation

The LXT9785/9785E provides an independent Reduced MII port for each network port. Each RMII uses four signals to pass received data to the MAC: RxData*n*<1:0>, RxER*n*, and CRS_DV*n* (where *n* reflects the port number). Three signals are used to transmit data from the MAC: TxData*n*_<1:0> and TxEN*n*. Both receive and transmit signals are clocked by REFCLK. Data transmission across the RMII is implemented in di-bit pairs which equal a 4-bit wide nibble.

2.8.1 RMII Reference Clock

The LXT9785/9785E requires a 50 MHz reference clock (REFCLK). The device samples the RMII input signals on the rising edge of REFCLK and drives RMII output signals on the falling edge.

2.8.2 Transmit Enable

TxEN*n* must be asserted and de-asserted synchronously with REFCLK. The MAC must assert TxEN*n* at the same time as the first nibble of preamble. TxEN*n* must be de-asserted after the last bit of the packet.

2.8.3 Carrier Sense & Data Valid

The LXT9785/9785E asserts CRS_DV*n* when it detects activity on the line. However, RxData*n* outputs zeros until the received data is decoded and available for transfer to the controller.

2.8.4 Receive Error

Whenever the LXT9785/9785E receives an error symbol from the network, it asserts RxER*n*. When it detects a bad Start-of-Stream Delimiter (SSD) it drives a “10” jam pattern on the RxData pins to indicate a false carrier event.

2.8.5 Out-of-Band Signalling

The LXT9785/9785E has the capability of encoding status information in the RxData stream during IPG. See “Monitoring Operations” on page 91 for details.

2.8.6 4B/5B Coding Operations

The 100BASE-X protocol specifies the use of a 5-bit symbol code on the network media. However, data is normally transmitted across the RMII interface in 2-bit nibblets or “di-bits”. The LXT9785/9785E incorporates a parallel/serial converter that translates between di-bit pairs and 4-bit nibbles, and a 4B/5B encoder/decoder circuit that translates between 4-bit nibbles and 5-bit symbols for the 100BASE-X connection. Figure 25 on page 75 shows the data conversion flow from nibbles to symbols. Table 22 on page 80 shows 4B/5B symbol coding (not all symbols are valid).

Figure 25. RMII Data Flow

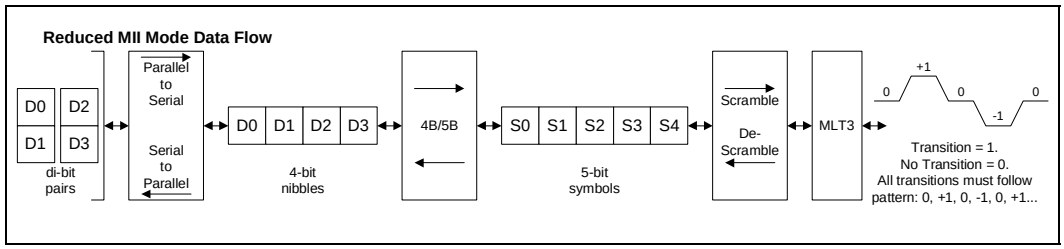


Figure 26. Typical RMII Interface Diagram

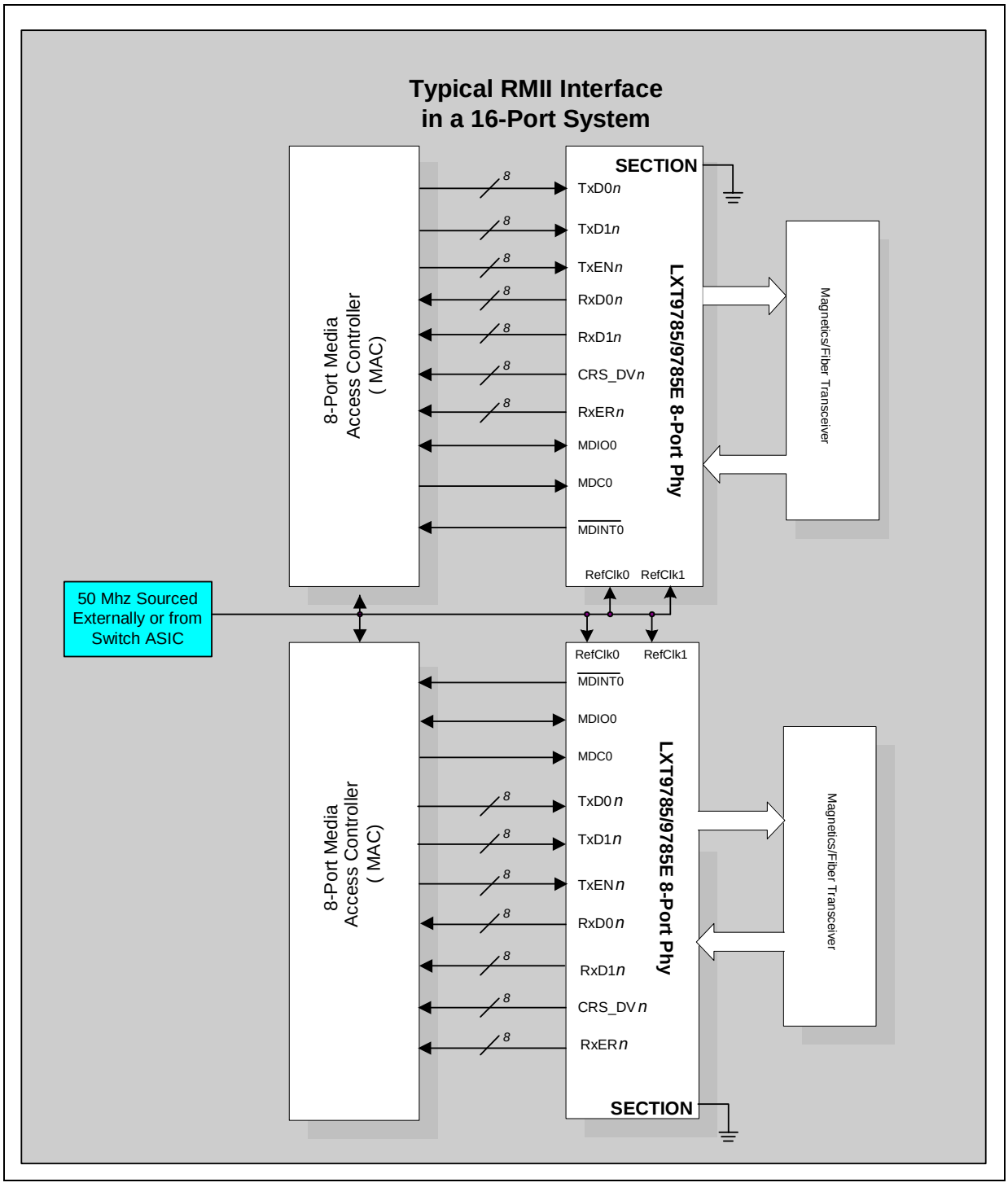
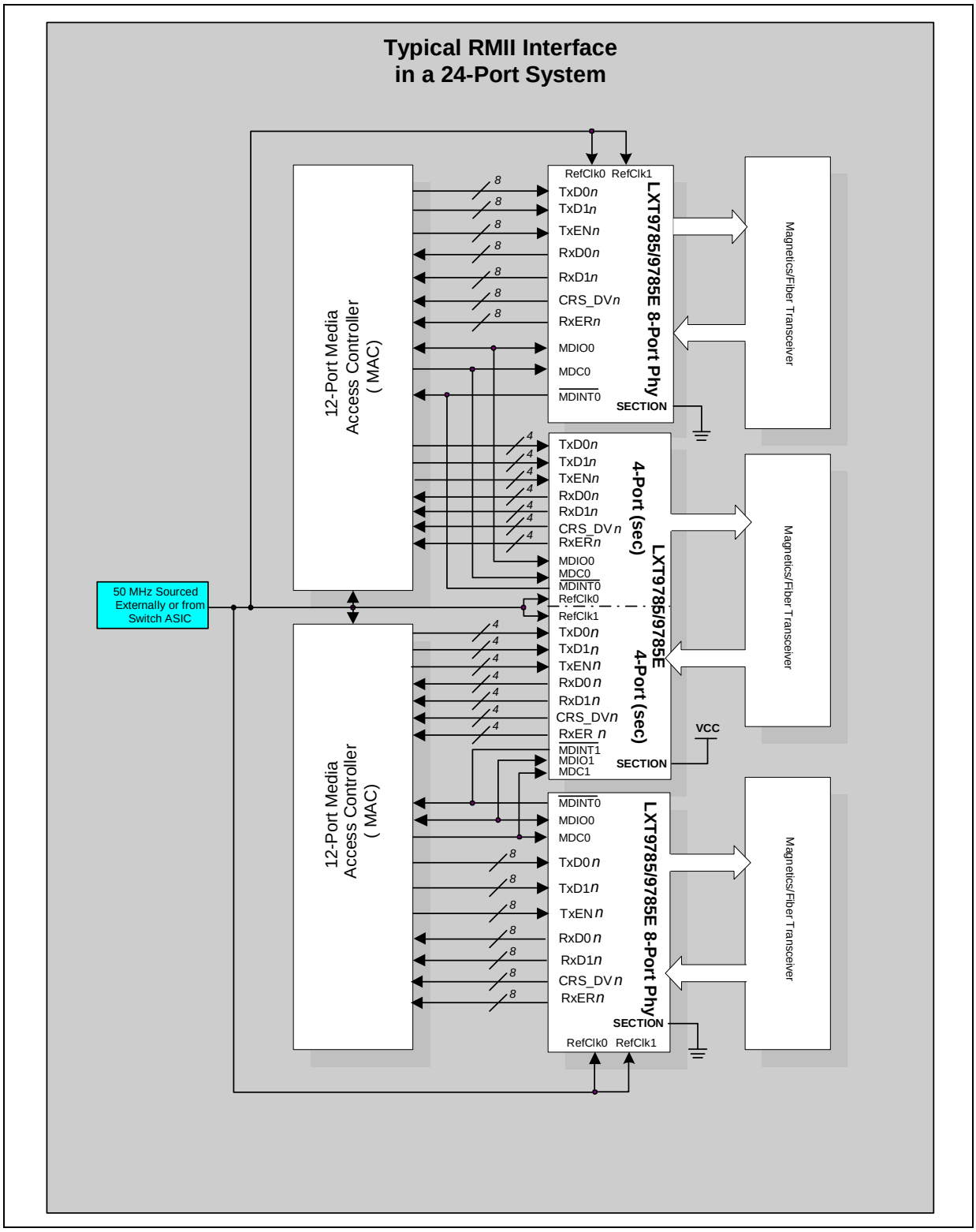


Figure 27. Typical RMII Quad Sectionalization Diagram



2.9 100 Mbps Operation

2.9.1 100BASE-X Network Operations

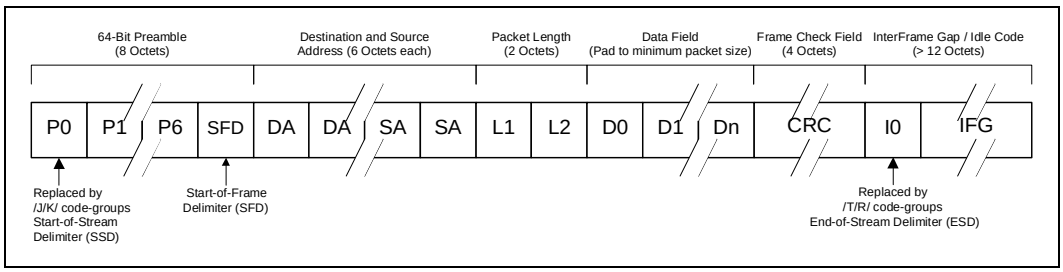
During 100BASE-X operation, the LXT9785/9785E transmits and receives 5-bit symbols across the network link. Figure 28 shows the structure of a standard frame packet. When the MAC is not actively transmitting data, the LXT9785/9785E sends out Idle symbols on the line.

In 100BASE-TX mode, the device scrambles the data and transmits it to the network using MLT-3 line code. The MLT-3 signals received from the network are de-scrambled and decoded, and sent across the RMII to the MAC.

In 100BASE-FX mode, the LXT9785/9785E transmits and receives NRZI signals across the PECL interface. An external 100BASE-FX transceiver module is required to complete the fiber connection.

As shown in Figure 28, the MAC starts each transmission with a preamble pattern. As soon as the LXT9785/9785E detects the start of preamble, it transmits a J/K Start-of-Stream Delimiter (SSD) symbol to the network. It then encodes and transmits the rest of the packet, including the balance of the preamble, the Start-of-Frame Delimiter (SFD), packet data, and CRC. Once the packet ends, the LXT9785/9785E transmits the T/R End-of-Stream Delimiter (ESD) symbol and then returns to transmitting Idle symbols.

Figure 28. 100BASE-X Frame Format



2.9.2 100BASE-X Protocol Sublayer Operations

In a 7-layer communications model, the LXT9785/9785E is a Physical Layer 1 (PHY) device. The LXT9785/9785E implements the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), and Physical Medium Dependent (PMD) sublayers of the reference model defined by the IEEE 802.3u specification. The following paragraphs discuss the LXT9785/9785E operation from the reference model point of view.

2.9.2.1 PCS Sublayer

The Physical Coding Sublayer (PCS) provides the RMII interface, as well as the 4B/5B encoding/decoding function. For 100BASE-TX and 100BASE-FX operation, the PCS layer provides IDLE symbols to the PMD-layer line driver as long as TxEN is de-asserted. For 10BASE-T operation, the PCS layer merely provides a bus interface and serialization/de-serialization function. 10BASE-T operation does not use the 4B/5B encoder.

2.9.2.1.1 Preamble Handling

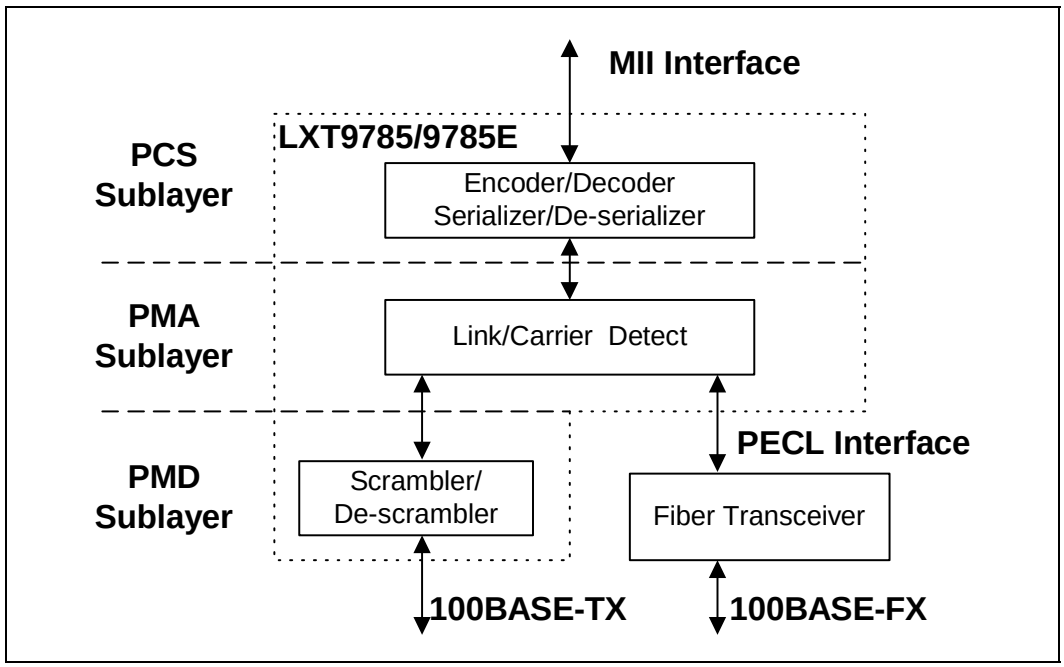
When the MAC asserts TxEN, the PCS substitutes a /J/K/ symbol pair, also known as the Start-of-Stream Delimiter (SSD), for the first two nibbles received across the RMII. The PCS layer continues to encode the remaining RMII data until TxEN is de-asserted (see Table 22 on page 80). It then returns to supplying IDLE symbols to the line driver.

The PCS layer performs the opposite function in the receive direction by substituting two preamble nibbles for the SSD.

2.9.2.1.2 Dribble Bits

The LXT9785/9785E handles dribble bits in all modes. If one through four dribble bits are received, the nibble is passed across the RMII, padded with ones if necessary. If five through seven dribble bits are received, the second nibble is not sent to the RMII bus.

Figure 29. Protocol Sublayers



2.9.3 PMA Sublayer

Table 22. 4B/5B Coding

Code Type	4B Code 3 2 1 0	Name	5B Code 4 3 2 1 0	Interpretation
	0 0 0 0	0	1 1 1 1 0	Data 0
	0 0 0 1	1	0 1 0 0 1	Data 1
	0 0 1 0	2	1 0 1 0 0	Data 2
	0 0 1 1	3	1 0 1 0 1	Data 3
	0 1 0 0	4	0 1 0 1 0	Data 4
	0 1 0 1	5	0 1 0 1 1	Data 5
	0 1 1 0	6	0 1 1 1 0	Data 6
DATA	0 1 1 1	7	0 1 1 1 1	Data 7
	1 0 0 0	8	1 0 0 1 0	Data 8
	1 0 0 1	9	1 0 0 1 1	Data 9
	1 0 1 0	A	1 0 1 1 0	Data A
	1 0 1 1	B	1 0 1 1 1	Data B
	1 1 0 0	C	1 1 0 1 0	Data C
	1 1 0 1	D	1 1 0 1 1	Data D
	1 1 1 0	E	1 1 1 0 0	Data E
	1 1 1 1	F	1 1 1 0 1	Data F
IDLE	undefined	I [1]	1 1 1 11	Idle. Used as inter stream fill code.
	0 1 0 1	J [2]	1 1 0 0 0	Start-of-Stream Delimiter (SSD), part 1 of 2.
CONTROL	0 1 0 1	K [2]	1 0 0 0 1	Start-of-Stream Delimiter (SSD), part 2 of 2.
	undefined	T [3]	0 1 1 0 1	End-of-Stream Delimiter (ESD), part 1 of 2.
	undefined	R [3]	0 0 1 1 1	End-of-Stream Delimiter (ESD), part 2 of 2.
	undefined	H [4]	0 0 1 0 0	Transmit Error. Used to force signalling errors.
	undefined	Invalid	0 0 0 0 0	Invalid
	undefined	Invalid	0 0 0 0 1	Invalid
	undefined	Invalid	0 0 0 1 0	Invalid
INVALID	undefined	Invalid	0 0 0 1 1	Invalid
	undefined	Invalid	0 0 1 0 1	Invalid
	undefined	Invalid	0 0 1 1 0	Invalid
	undefined	Invalid	0 1 0 0 0	Invalid
	undefined	Invalid	0 1 1 0 0	Invalid
	undefined	Invalid	1 0 0 0 0	Invalid
	undefined	Invalid	1 1 0 0 1	Invalid

1. The /I/ (Idle) code group is sent continuously between frames.
2. The /J/ and /K/ (SSD) code groups are always sent in pairs; /K/ follows /J/.
3. The /T/ and /R/ (ESD) code groups are always sent in pairs; /R/ follows /T/.
4. An /H/ (Error) code group is used to signal an error condition.

2.9.3.0.1 Link

In 100 Mbps mode, the LXT9785/9785E establishes a link whenever the scrambler becomes locked and remains locked for approximately 50 ms. Whenever the scrambler loses lock (<12 consecutive idle symbols during a 2 ms window), the link is taken down. This provides a robust link, filtering out any small noise hits that may otherwise disrupt the link. Furthermore, 100 Mbps idle patterns will not bring up a 10 Mbps link.

The LXT9785/9785E reports link failure via the RMII status Register bits (1.2, 17.10, and 19.4) and interrupt functions. If auto-negotiate is enabled, link failure causes the device to re-negotiate.

2.9.3.0.2 Link Failure Override

The LXT9785/9785E normally transmits 100 Mbps data packets or Idle symbols only if it detects the link is up, and transmits only FLP bursts if the link is not up. Setting Register bit 16.14 = 1 overrides this function, allowing the LXT9785/9785E to transmit data packets even when the link is down. This feature is provided as a diagnostic tool.

Note: Auto-negotiation must be disabled to transmit data packets in the absence of link. If auto-negotiation is enabled, the LXT9785/9785E automatically begins transmitting FLP bursts if the link goes down.

2.9.3.0.3 Carrier Sense/Data Valid (RMII)

The LXT9785/9785E asserts CRS_DV whenever the respective port receiver is in a non-idle state (as defined by the RMII Specification Revision 1.2), including false carrier events. Assertion of CRS_DV is asynchronous with respect to REFCLK. In the event that signal decoding is not complete when CRS_DV is asserted, the LXT9785/9785E outputs 00 on the RxData1:0 lines until the decoded data are available.

When the line returns to an idle state, CRS_DV is de-asserted asynchronously with respect to REFCLK. If the FIFO still contains data to be passed to the MAC via the RMII when CRS is de-asserted, CRS_DV toggles on nibble boundaries until the FIFO is empty. For 100BASE-X signals, CRS_DV toggles at 25 MHz. For 10BASE-T signals, CRS_DV toggles at 2.5 MHz.

2.9.3.0.4 Carrier Sense (SMII)

For 100BASE-TX and 100BASE-FX links, a Start-of-Stream Delimiter (SSD) or /J/K/ symbol pair causes assertion of carrier sense (CRS). An End-of-Stream Delimiter (ESD), or /T/R/ symbol pair causes de-assertion of CRS. The PMA layer also de-asserts CRS if IDLE symbols are received without /T/R/. In this event, the RxER bit in the RX Status Frame is asserted for one clock cycle when CRS is de-asserted.

For 10BASE-T links, CRS assertion is based on receipt of valid preamble, and de-assertion on receipt of an End-of-Frame (EOF) marker.

2.9.3.0.5 Receive Data Valid (SMII)

The LXT9785/9785E asserts the RX_DV bit when it receives a valid packet. However, RxData outputs zeros until the received data are decoded and available for transfer to the controller.

2.9.3.1 Twisted-Pair PMD Sublayer

The twisted-pair Physical Medium Dependent (PMD) layer provides the signal scrambling and descrambling, line coding and decoding (MLT-3 for 100BASE-TX, Manchester for 10BASE-T), as well as receiving, polarity correction, and baseline wander correction functions.

2.9.3.1.1 Scrambler/Descrambler (100BASE-TX Only)

The purpose of the scrambler is to spread the signal power spectrum and further reduce EMI using an 11-bit, non-data-dependent polynomial. The receiver automatically decodes the polynomial whenever IDLE symbols are received.

The scrambler/descrambler can be bypassed by setting Register bit 16.12 = 1. The scrambler is automatically bypassed when the fiber port is enabled. Scrambler bypass is provided for diagnostic and test support.

2.9.3.1.2 Baseline Wander Correction

The LXT9785/9785E provides a baseline wander correction function which makes the device robust under all network operating conditions. The MLT3 coding scheme used in 100BASE-TX is, by definition, “unbalanced”. This means that the DC average value of the signal voltage can “wander” significantly over short time intervals (tenths of seconds). This wander may cause receiver errors, particularly in less robust designs, at long line lengths (100 meters). The exact characteristics of the wander are completely data dependent.

The LXT9785/9785E baseline wander correction characteristics allow the device to recover error-free data while receiving worst-case “killer” packets over all cable lengths.

2.9.3.1.3 Polarity Correction

The LXT9785/9785E automatically detects and corrects for the condition where the receive signal (TPFIP/N) is inverted. Reversed polarity is detected if eight inverted link pulses or four inverted End-of-Frame (EOF) markers are received consecutively. If link pulses or data are not received by the maximum receive time-out period, the polarity state is reset to a non-inverted state.

2.9.3.2 Fiber PMD Sublayer

The LXT9785/9785E provides a PECL interface for connection to an external fiber-optic transceiver. (The external transceiver provides the PMD function for fiber media.) The device uses an NRZI format for the fiber interface. The fiber interface operates at 100 Mbps and does not support 10FL applications.

2.9.3.2.1 Far End Fault Indications

The LXT9785/9785E Signal Detect pins independently detect signal faults from the local fiber transceivers via the SD pins. The device also uses Register bit 1.4 to report Remote Fault indications received from its link partner. The device “ORs” both fault conditions to set Register bit 1.4. Register bit 1.4 is set once and clears when read.

Either fault condition causes the LXT9785/9785E to drop the link unless Forced Link Pass is selected (16.14 = 1). Link down condition is then reported via interrupts and status bits.

In response to locally detected signal faults (SD activated by the local fiber transceiver), the affected port can transmit the far end fault code if fault code transmission is enabled by Register bit 16.2.

- When Register bit 16.2 = 1, transmission of the far end fault code is enabled. The LXT9785/9785E transmits far end fault code if fault conditions are detected by the Signal Detect pins.
- When Register bit 16.2 = 0, the LXT9785/9785E does not transmit far end fault code. It continues to transmit idle code and may or may not drop link depending on the setting for Register bit 16.14.

The occurrence of a Far End Fault causes all transmission of data from the Reconciliation Sublayer to stop and the Far End Fault code to begin. The Far End Fault code consists of 84 ones's followed by a single "0" and is repeated until the Far End Fault condition is removed.

2.10 10 Mbps Operation

The LXT9785/9785E operates as a standard 10BASE-T transceiver and supports all the standard 10 Mbps functions. During 10BASE-T operation, the LXT9785/9785E transmits and receives Manchester-encoded data across the network link. When the MAC is not actively transmitting data, the device sends out link pulses on the line.

In 10BASE-T mode, the polynomial scrambler/descrambler is inactive. Manchester-encoded signals received from the network are decoded by the LXT9785/9785E and sent across the RMII to the MAC.

Note: The LXT9785/9785E does not support fiber connections at 10 Mbps.

2.10.1 Preamble Handling

The LXT9785/9785E offers two options for preamble handling, selected by Register bit 16.5. In 10BASE-T mode when Register bit 16.5 = 0, the device strips the entire preamble off the received packets. CRS_DV is asserted simultaneously with SFD. CRS_DV is held Low for the duration of the preamble. When CRS_DV is asserted, the very first two nibbles driven by the LXT9785/9785E are the SFD "5D" hex followed by the body of the packet.

When Register bit 16.5 = 1 in 10BASE-T mode, the LXT9785/9785E passes the preamble through the RMII and asserts CRS_DV simultaneously.

2.10.2 Dribble Bits

The LXT9785/9785E device handles dribble bits in all modes. If one through four dribble bits are received, the nibble is passed across the RMII. If five through seven dribble bits are received, the second nibble is not sent onto the RMII bus.

2.10.3 Link Test

The LXT9785/9785E always transmits link pulses in 10BASE-T mode. When enabled, the link test function monitors the connection for link pulses. Once link pulses are detected, data transmission is enabled and remains enabled as long as either the link pulses or data transmission continue. If link pulses stop, the data transmission is disabled.

If the link test function is disabled, the LXT9785/9785E transmits to the connection regardless of detected link pulses. The link test function is disabled by setting Register bit 16.14 = 1.

2.10.3.1 Link Failure

Link failure occurs if Link Test is enabled and link pulses or packets stop being received. If this condition occurs, the LXT9785/9785E returns to the auto-negotiation phase if auto-negotiation is enabled.

2.10.4 Jabber

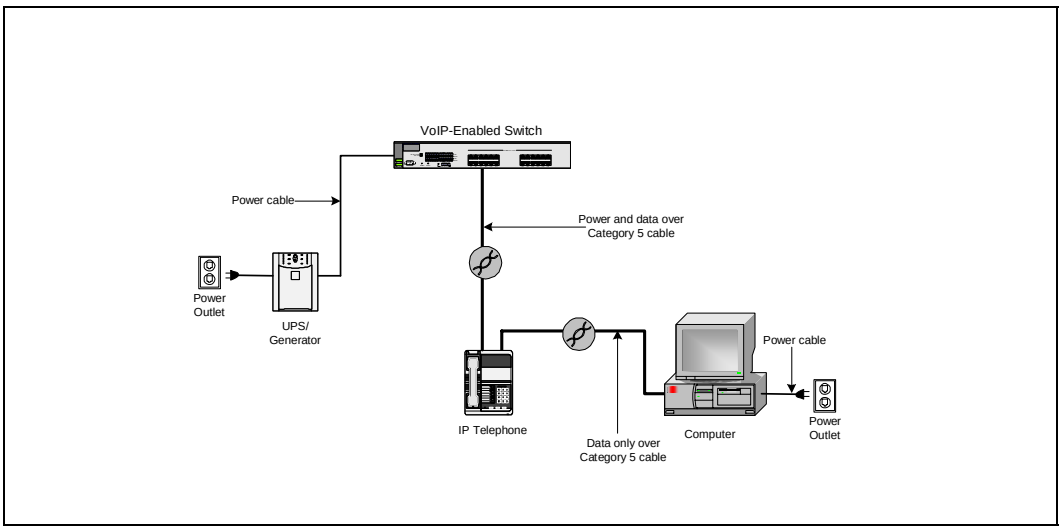
If a transmission exceeds the jabber timer, the LXT9785/9785E disables the transmit and loopback functions. The RMII does not include a Jabber pin, but the MAC may read Register 1 or 25 to determine Jabber status. The LXT9785/9785E automatically exits jabber mode after the unjab time has expired. This function is disabled by setting Register bit 16.10 = 1.

2.11 DTE Discovery Process

The DTE discovery process is port dependent and must be enabled through software. The process is implemented as a next page option to the auto-negotiation flow. This feature applies to the LXT9785E transceiver only.

The process depends upon an IP phone, or any other DTE capable of being powered remotely, having a specific filter that passes NLPs and FLPs. This filter should be non-polarized to ensure that the latest status of Auto-MDIX operation does not effect operation. This filter attenuates 100 Mbps MLT3 signals and 10 Mbps Manchester-encoded signals, and must be bypassed when power is applied to the IP phone. Figure 30 shows a typical IP telephone system connection.

Figure 30. Typical IP Telephone System Connection



2.11.1 Definitions

The following terms are used throughout the DTE discovery sections:

Negotiation Process:	This includes auto-negotiation and parallel detection processes
System:	The switch system using the LXT9785E for DTE Discovery
Link Partner:	A device connected to the LXT9785E through twisted pair cables
DTE:	Data Terminal Equipment; any end-of-link partner
Standard Link Partner:	A link partner that does not require power over a Category 5 cable; typically a PC
Remote-Power DTE:	Data Terminal Equipment requiring power over a Category 5 cable; typically an IP telephone
Discovery:	The process of identifying the type of link partner present

2.11.2 Interaction between Processor, MAC and PHY

The state machines that control the mechanics of the Discovery process reside within the LXT9785E device. However, control of the power supply and overall system control reside in the system processor. The processor communicates with the power supply unit (PSU) and switches it on and off dependant on the data that is supplied by the PHY. The PHY register data is read by the MAC using the MDIO interface. The required control bits are contained in the PHY device register map and are discussed in detail in the section labeled "Management Interface and Control" on page 87.

Note: The details of the processor/MAC interface and the processor/PSU interface are implementation specific and therefore are out of the scope of this specification.

The following is an overview of the system control for a successful Remote-Power DTE discovery:

1. The discovery process is enabled by the DTE Discovery Process Enable (Dis_EN) Register bit 27.6 and the Auto-Negotiation Enable Register bit 0.12.
2. The LXT9785E PHY then tests to see if a Remote-Power DTE is present as the link partner. If a Remote-Power DTE is found, the Power Enable (Power_EN) Register bit 27.4 is set. The processor polls this signal via the MAC.
3. Upon detecting a Remote-Power DTE, the processor instructs the power supply to switch on. Once power has been applied to the DTE, normal negotiation takes place. The processor must enable the required negotiation process by restarting auto-negotiation, or by setting forced speed mode after power has been applied. The processor must poll the link-up Register bit 1.2 for the corresponding LXT9785E port, or the link status change interrupt, to ensure that the link has been established.
4. A time-out must be connected with this feature so that if link is not established within a pre-determined time period (system dependant), the processor instructs the power supply to switch off. If link is not established prior to the expiration of the "link fail inhibit timer", the LXT9785E restarts negotiation with DTE detection if auto-negotiation mode was used to establish link with the phone, and the DTE process is still enabled. The LXT9785E restarts negotiation without DTE detection if either forced speed mode is used to establish link with the phone, or the DTE process is disabled.
5. If power is applied and link is established, the system must still poll the Link Status Register bit 1.2 for the corresponding LXT9785E port or the link status change interrupt. This is required since link status is the only way to know when the Remote-Power DTE is removed or unplugged. On seeing the Link_Down condition, the processor instructs the power supply to switch off, and the DTE Discovery begins again or is disabled.

2.11.3 Management Interface and Control

The management and control of the DTE discovery process is via the MDIO port. Each port on the LXT9785E is capable of running the discovery process, thus each port is independently controlled. This is achieved by each port having a dedicated set of control and status bits. These bits are found in Register 27 as follows:

DTE DISCOVERY PROCESS ENABLE - Register Bit 27.6 (Dis_EN)
R/W Default value = 0: Disabled.

Register bit 27.6 controls the operation of the process. The discovery process is disabled when Register bit 27.6 = 0, and enabled when Register bit 27.6 = 1. The MAC controller sets Register bit 27.6 to a 1 when a port search for a DTE requiring power is desired. Once set, Register bit 27.6 remains = 1 until the MAC clears it, either by directly clearing it or by resetting the PHY. This allows the discovery process to continue to function if unsuccessful in detecting a DTE, without being continually re-enabled by the MAC. If Register bit 27.6 is set after link is established, no action is taken until after the link goes down.

POWER ENABLE - Register Bit 27.4 (Power_EN)
RO Default value = 0: No Remote-Power DTE found.

Register bit 27.4 contains the result of the discovery process. When Register bit 27.4 = 0, the discovery process has not found a DTE requiring power, and when Register bit 27.4 = 1, the discovery process has potentially found a DTE requiring power. This indicates power should be applied to the Category 5 cable. Register bit 27.4 is polled by the MAC during the discovery process, and is cleared when the PHY is reset, when auto-negotiation is restarted, or when auto-negotiation is disabled. In the event of a discovery process being interrupted due to detection of an already powered link partner (auto-negotiation completion or Parallel Detection), Register bit 27.4 = 0.

STANDARD LINK PARTNER DETECTED - Register Bit 27.3 (SLP_Det)
R/W Clear on Read Default value = 0: No link partner found.

When Register bit 27.3 = 1, a standard link partner has been detected by the LXT9785E (NLPs, MLT3 data, FLPs without next page support, or FLPs with non-matching next pages). This indicates power should not be applied to the Category 5 cable. When Register bit 27.3 = 0, other bits are checked to determine overall status of the link partner. Register bit 27.3 is cleared on read, or DTE discovery is disabled, link is established, or auto-negotiation is either restarted or disabled.

LINK FAIL TIMEOUT - Register Bit 27.2 (LFIT Expired)
R/W Clear on Read Default value = 0 (Link Fail Inhibit timer has expired without establishment of link with a standard link partner). Valid only when Standard Link Partner Detected Register bit 27.3 = 1.

Register bit 27.2 is set if link is not established prior to the Link Fail Inhibit Timer expiring. This indicates that the Discovery process has restarted and the Standard Link Partner Detected Register bit may no longer be valid. Register bit 27.2 is cleared on read, or DTE discovery is disabled, link is established, or auto-negotiation is either restarted or disabled.

2.11.4 DTE Discovery Process Function Description

The following section describes the DTE Discovery process. See Figure 31 on page 90 for a flow chart of the discovery process.When DTE Discovery (27.6) and auto-negotiation (0.12) are enabled (auto-negotiation mode is required), the LXT9785E transmits the auto-negotiation base page with the next page ability bit set (Auto-Negotiation Advertisement Register (Address 4)).

System software polls Register 27 to determine if or when a Remote-Power DTE is detected. The receiver monitors the line to determine if NLPs, MLT3 data, or FLP bursts are being received. If the receive activity is FLP bursts, the status of the next page ability bit is checked. If the detected "link partner" also supports next page, then the LXT9785E transmits out the next page sequence associated with message code #5 (Organizationally Unique Identifier (OUI) Tag Code). The definition for the next pages to be sent out for this message code include some user-defined code values. These values are loaded with randomly created data from an internal LSFR that is free running and seeded with the PHY address of the LXT9785E port. The Next Pages are hard coded in the logic (the LXT9785E ignores any data written into Register 7) and are outlined in Table 23 on page 89. The receiver monitors the next pages to determine that the exact next page data (especially the random data) transmitted is received. The Power-Enable Register bit 27.4 is set when a Remote-Power DTE is detected as the link partner, and the last next page is repeatedly transmitted until software restarts the required negotiation process (auto-negotiation or forced-speed mode).

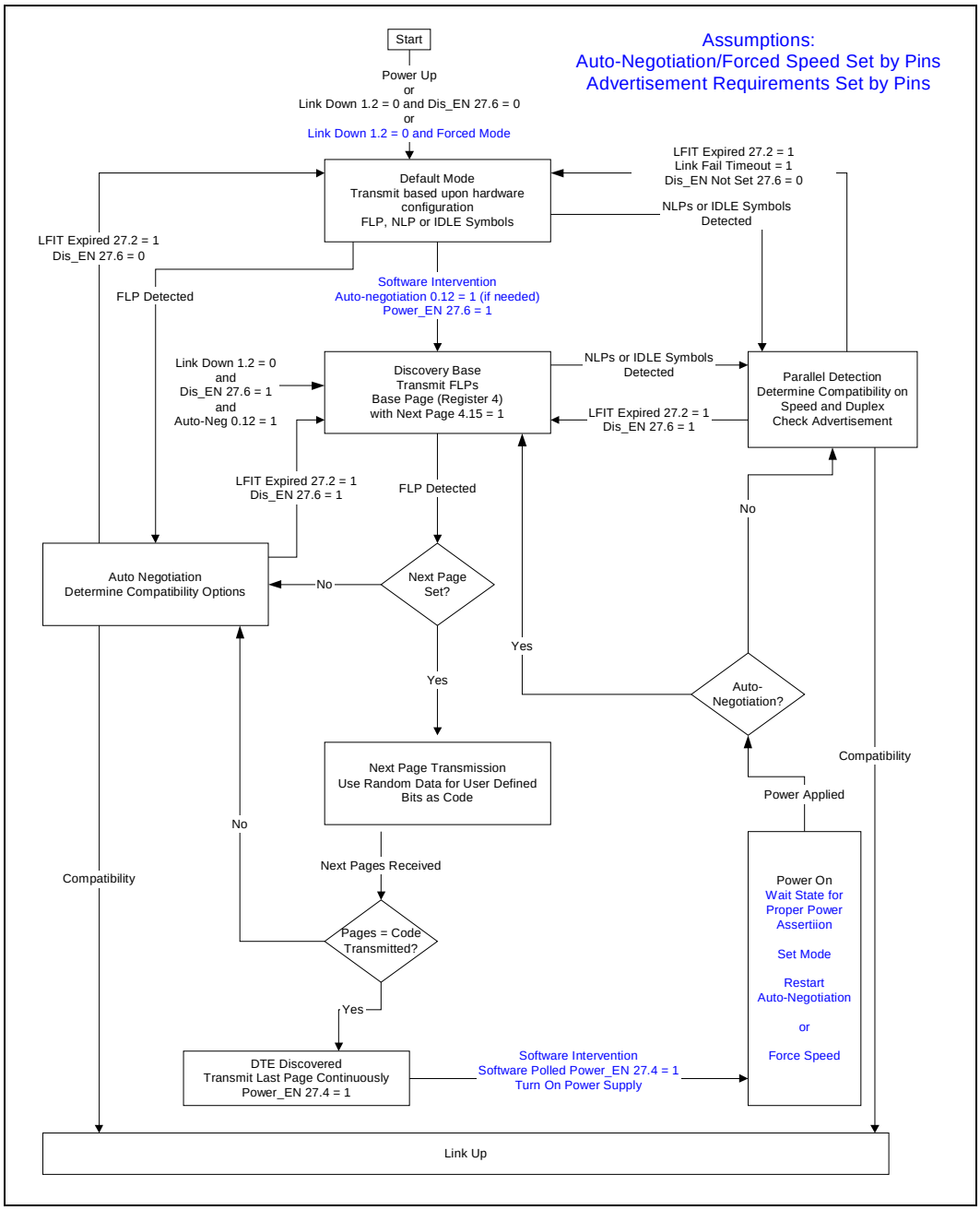
The software should be written so that the negotiation is not restarted until the DTE has been powered up over the Category 5 cable. The Power-Enable Register bit 27.4 is cleared upon restarting or disabling auto-negotiation (selecting forced mode). The system must be able to detect over-current conditions and be capable of disabling power in case the link partner is not a Remote-Power DTE. Some examples of devices that would mistakenly set Power-Enable Register bit 27.4 are a token-ring balun and a loopback cable. Once link partner power has been stabilized and sufficient time has passed for the link partner to initialize, the negotiation process may be restarted.

The negotiation process establishes link if a compatible mode exists between the LXT9785E and the link partner. If a compatible mode does not exist (not compatible or not established within the Link Fail Inhibit Timer period), the LXT9785E either restarts auto-negotiation/DTE discovery (discovery is enabled (Register bit 27.6=1) and auto-negotiation is enabled (Register bit 0.12 = 1)), or normal negotiation (discovery is disabled (Register bit 27.6=0) and auto-negotiation is enabled (Register bit 0.12 = 1)), or either 10 Mbps or 100 Mbps forced-mode operation (auto-negotiation is disabled (Register bit 0.12 = 0)). The software must detect this non-link state and disable power.

Table 23. Next Page Message #5 Code Word Definitions

Next Page Encoding	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OUI Tagged Message	1	a	1	0	t	0	0	0	0	0	0	0	0	1	0	1
User Page 1	1	a	0	0	t	3.10	3.11	3.12	3.13	3.14	3.15	2.0	2.1	2.2	2.3	2.4
User Page 2	1	a	0	0	t	2.5	2.6	2.7	2.8	2.9	2.10	2.11	2.12	2.13	2.14	2.15
User Page 3	1	a	0	0	t	0	0	L.8	L.7	L.6	L.5	L.4	L.3	L.2	L.1	L.0
User Page 4	1	a	0	0	t	L.10	L.9	L.8	L.7	L.6	L.5	L.4	L.3	L.2	L.1	L.0
1. a is the acknowledge bit; t is the toggle bit; L is the LFSR																

Figure 31. LXT9785E Negotiation Flow Chart



2.12 Monitoring Operations

2.12.1 Monitoring Auto-Negotiation

Auto-negotiation may be monitored as follows:

- Register bits 1.2 and 17.10 = 1 once the link is established.
- Additional bits in Register 1 (refer to Table 59 on page 127) and Register 17 (refer to Table 68 on page 134) can be used to determine the link operating conditions and status.

2.12.2 Per-Port LED Driver Functions

The LXT9785/9785E incorporates three direct drive LEDs per port ($\overline{\text{LED}n\_1}$, $\overline{\text{LED}n\_2}$, and $\overline{\text{LED}n\_3}$). On power up, all the LEDs lights up for approximately one second after reset de-asserts. Each LED may be programmed to one of several different display modes using the LED Configuration Register. Each per-port LED may be programmed (refer to Table 71 on page 137) to indicate one of the following conditions:

- Operating Speed
- Transmit Activity
- Receive Activity
- Collision Condition
- Link Status
- Duplex Mode
- Isolate Condition

The LEDs can also be programmed to display various combined status conditions. For example, setting Register bits 20.15:12 = 1101 produces the following combination of Link and Activity indications:

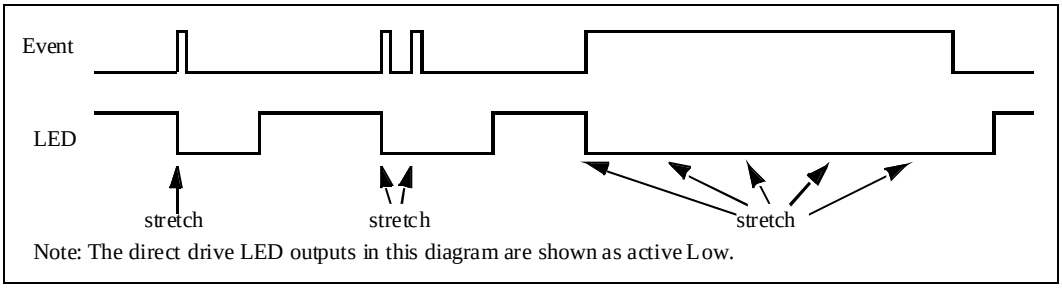
- If Link is down, LED is off.
- If Link is up, LED is on.
- If Link is up AND activity is detected, the LED blinks at the stretch interval selected by Register bits 20.3:2 and continues to blink as long as activity is present.

The LED driver pins are open drain circuits (10mA max current rating). Refer to "LED Circuit" on page 97 under the Application Information Section for LED circuit design details. The LED Configuration Register also provides optional LED pulse stretching to 30, 60, or 100 ms. If during this pulse stretch period, the event occurs again, the pulse stretch time is further extended (see Table 71 on page 137).

When an event such as receiving a packet occurs, it is edge detected and starts the stretch timer. The LED driver remains asserted until the stretch timer expires. If another event occurs before the stretch timer expires, the stretch timer is reset and the stretch time extended.

When a long event (such as duplex status) occurs, it is edge detected and starts the stretch timer. When the stretch timer expires, the edge detector is reset so that a long event causes another pulse to be generated from the edge detector. The edge detector resets the stretch timer, causing the LED driver to remain asserted. Figure 32 on page 92 shows how the stretch operation functions.

Figure 32. LED Pulse Stretching



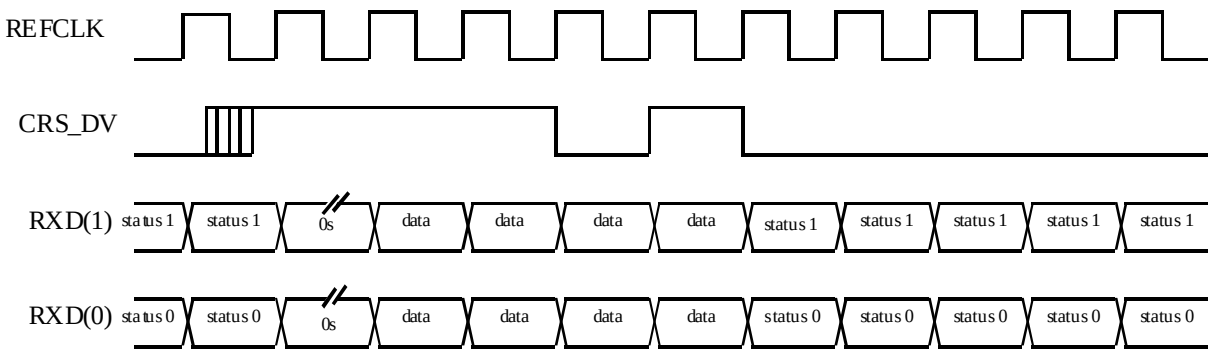
2.12.3 Out-of-Band Signalling

The LXT9785/9785E provides an out-of-band signalling option to transfer status information across the RMII receive interface. This feature is enabled when Register bit 25.0 = 1 and uses the RxData(1:0) data bus during the Inter-Packet Gap (IPG) time as shown in Figure 33.

The two status bits transferred across the RxData bus are software selectable via Register 25 (see Table 73 on page 139).

In normal operation, the LXT9785/9785E stuffs the RxData bus with zeros during the IPG. A software-selectable bit enables the RMII out-of-band signalling feature. Once this bit is set, the LXT9785/9785E replaces the zeros with selected status bits during the IPG.

Figure 33. RMII Programmable Out-of-Bank Signaling



1. When network activity is detected, the LXT9785/9785E asserts CRS_DV asynchronously with respect to REFCLK.
2. After CRS_DV is asserted, the LXT9785/9785E zero-stuffs the RxData bits until the received data has been processed through the FIFO.
3. When network activity ceases, the LXT9785/9785E de-asserts CRS_DV synchronously with respect to REFCLK. CRS_DV toggles until all data in the FIFO has been processed through the RMII. Once the FIFO is empty, LXT9785/9785E drives the status bits selected by the Out-of-Band Signalling Register (refer to Table 73 on page 139) on the RxData outputs.

The LXT9785/9785E includes an IEEE 1149.1 boundary scan test port for board level testing. All digital input, output, and input/output pins are accessible.

2.12.4 Boundary Scan Interface

This interface consists of five pins (TMS, TDI, TDO, TCK and $\overline{\text{TRST}}$). It includes a state machine, data register array, and instruction register. The TMS and TDI pins are internally pulled up and the TCK pin is internally pulled down. TDO does not have an internal pull-up or pull-down.

2.12.5 State Machine

The TAP controller is a 16-state machine driven by the TCK and TMS pins. Upon reset, the TEST_LOGIC_RESET state is entered. The state machine is also reset when TMS and TDI are High for five TCK periods.

2.12.6 Instruction Register

The IDCODE instruction is always invoked after the state machine resets. The decode logic ensures the correct data flow to the Data registers according to the current instruction. Valid instructions are listed in Table 25.

2.12.7 Boundary Scan Register

Each Boundary Scan Register (BSR) cell has two stages. A flip-flop and a latch are used for the serial shift stage and the parallel output stage. There are four modes of operation as listed in Table 24.

Table 24. BSR Mode of Operation

Mode	Description
1	Capture
2	Shift
3	Update
4	System Function

Table 25. Supported JTAG Instructions

Name	Code	Description	Data Register
EXTEST	0000 Hex	External Test	BSR
IDCODE	FFFE Hex	ID Code Inspection	ID REG
SAMPLE	FFF8 Hex	Sample Boundary	BSR
High Z	FFCF Hex	Force Float	Bypass
Clamp	FFEF Hex	Clamp	BSR
BYPASS	FFFF Hex	Bypass Scan	Bypass

3.0 Application Information

3.1 Design Recommendations

The LXT9785/9785E is designed to comply with IEEE 802.3 requirements to provide outstanding receive Bit Error Rate (BER), and long-line-length performance. To achieve maximum performance from the LXT9785/9785E, attention to detail and good design practices are required. *Refer to the LXT9785 Design and Layout Guide application note for detailed design and layout information*.

3.2 General Design Guidelines

Adherence to generally accepted design practices is essential to minimize noise levels on power and ground planes. Up to 50 mV maximum of noise is considered acceptable. High-frequency switching noise can be reduced, and its effects eliminated, by following these simple guidelines throughout the design:

- Fill in unused areas of the signal planes with solid copper and attach them with vias to a VCC or ground plane that is not located adjacent to the signal layer.
- Use ample bulk and decoupling capacitors throughout the design (a value of 0.01 µF is recommended for decoupling caps).
- Provide ample power and ground planes.
- Provide termination on all high-speed switching signals and clock lines.
- Provide impedance matching on long traces to prevent reflections.
- Route high-speed signals next to a continuous, unbroken ground plane.
- Filter and shield DC-DC converters, oscillators, etc.
- Do not route any digital signals between the LXT9785/9785E and the RJ-45 connectors at the edge of the board.
- Do not extend any circuit power and ground plane past the center of the magnetics or to the edge of the board. Use this area for chassis ground, or leave it void.

3.2.1 Power Supply Filtering

Power supply ripple and digital switching noise on the VCC plane may cause EMI problems and degrade line performance. The best approach to this problem is to minimize ground noise as much as possible using good general techniques and by filtering the VCC plane. It is generally difficult to predict in advance the performance of any design, although certain factors greatly increase the risk of having problems:

- Poorly-regulated or over-burdened power supplies.
- Wide data busses (32-bits+) running at a high clock rate.
- DC-to-DC converters.

Intel recommends filtering the power supply to the analog VCC pins of the LXT9785/9785E. This has two benefits. First, it keeps digital switching noise out of the analog circuitry inside the LXT9785/9785E, helping with line performance. Second, if the VCC planes are laid out correctly, digital switching noise is kept away from external connectors, reducing EMI problems.

The recommended implementation is to break the VCC plane into two sections. The digital section supplies power to the VCCD and VCCIO pins of the LXT9785/9785E. The analog section supplies power to the VCCA pins. The break between the two planes should run underneath the device. In designs with more than one the LXT9785/9785E, a single continuous analog VCC plane can be used to supply them all.

The digital and analog VCC planes should be joined at one or more points by ferrite beads. The beads should produce at least a 100Ω impedance at 100 MHz. Beads should be placed so that current flow is evenly distributed. The maximum current rating of the beads should be at least 150% of the current that is actually expected to flow through them. A bulk cap (2.2 -10 µF) should be placed on each side of each bead.

In addition, a high-frequency bypass cap (0.01uF) should be placed near each analog VCC pin.

3.2.2 Power and Ground Plane Layout Considerations

Great care needs to be taken when laying out the power and ground planes.

- Follow the guidelines in the *LXT9785 Design and Layout Guide (formerly Application Note 151)* for locating the split between the digital and analog VCC planes.
- Keep the digital VCC plane away from the TPFOP/N and TPFIP/N signals, the magnetics, and the RJ-45 connectors.
- Place the layers so that the TPFOP/N and TFPIP/N signals can be routed near or next to the ground plane. For EMI reasons, it is more important to shield TPFOP/N than TPFIP/N.

3.2.2.1 Chassis Ground

For ESD reasons, it is a good design practice to create a separate chassis ground that encircles the board and is isolated via moats and keep-out areas from all circuit-ground planes and active signals. Chassis ground should extend from the RJ-45 connectors to the magnetics, and can be used to terminate unused signal pairs (Bob Smith termination). In single-point grounding applications, provide a single connection between chassis and circuit grounds with a 2 kV isolation capacitor. In multi-point grounding schemes (chassis and circuit grounds joined at multiple points), provide 2 kV isolation to the Bob Smith termination.

3.2.3 MII Terminations

Series termination resistors are required on all the SS-SMII output signals driven by the LXT9785/9785E. Special trace layout consideration should be used when using the SMII interface. Keep all traces orthogonal and as short as possible. Whenever possible, route the clock and sync traces evenly between the longest and shortest data routes. This minimizes round-trip, clock-to-data delays and allows a larger margin to the setup and hold requirements.

3.2.4 Twisted-Pair Interface

Use the following standard guidelines for a twisted-pair interface:

- Place the magnetics as close as possible to the LXT9785/9785E.
- Keep transmit pair traces as short as possible; both traces should have the same length.
- Avoid vias and layer changes as much as possible.
- Keep the transmit and receive pairs apart to avoid cross-talk.
- Route the transmit pair adjacent to a ground plane. The optimum arrangement is to place the transmit traces two to three layers from the ground plane, with no intervening signals.
- Improve EMI performance by filtering the TPO center tap. A single ferrite bead rated at 400 mA may be used to supply center tap current to all ports.

3.2.4.1 Magnetic Requirements

The LXT9785/9785E requires a 1:1 ratio for both the receive transformers and the transmit transformers. The transmit isolation voltage should be rated at 1.5 kV to protect the circuitry from static voltages across the connectors and cables. The LXT9785/9785E is a current driven transceiver that requires an external voltage (center tap) to drive the transmit signal. In order to support the Auto-MDIX functionality of the LXT9785/9785E, the magnetic must provide a center tap for both the transmit and receive magnetic winding, with both connected to VCCT. See the LXT9785/9785E Design and Layout Guide (249509-001) for magnetic testing with the LXT9785/9785E. Before committing to a specific component, designers should contact the manufacturer for current product specifications, and validate the magnetics for the specific application. Table 26 provides the magnetics requirements.

Table 26. Magnetics Requirements

Parameter	Min	Nom	Max	Units	Test Condition
Rx turns ratio	–	1:1	–	–	
Tx turns ratio	–	1:1	–	–	
Insertion loss	0.0	0.6	1.1	dB	
Primary inductance	350	–	–	µH	
Transformer isolation	–	2	–	kV	
Differential to common mode rejection	40	–	–	dB	.1 to 60 MHz
	35	–	–	dB	60 to 100 MHz
Return Loss	-16	–	–	dB	30 MHz
	-10	–	–	dB	80 MHz

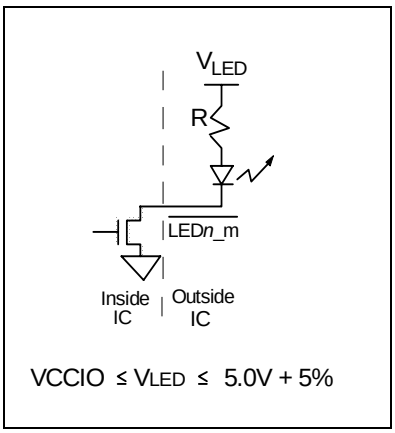
3.2.5 The Fiber Interface

The fiber interface consists of a PECL transmit and receive pair to an external fiber-optic transceiver. The transmit and receive pair should be DC-coupled to the transceiver, and biased appropriately. Refer to the fiber transceiver manufacturer's recommendations for termination circuitry. Figure 37 on page 99 shows a typical example.

3.2.6 LED Circuit

Each Direct Drive LED has a corresponding open-drain pin. The LEDs are connected via a current-limiting resistor to a positive-voltage rail. The LEDs are turned on when the output pin drives Low. The open-drain LED pins are 5V tolerant, allowing use of either a 3.3V or 5V rail (a 2.5V rail is unlikely to work with standard forward voltage LEDs). A 5V rail eases LED component selection by allowing more common, high-forward voltage LEDs to be used. Refer to Figure 34 for a circuit illustration.

Figure 34. LED Circuit



3.3 Typical Application Circuits

Figure 35 through Figure 37 on page 99 show typical application circuits for the LXT9785/9785E.

Figure 35. Power and Ground Supply Connections

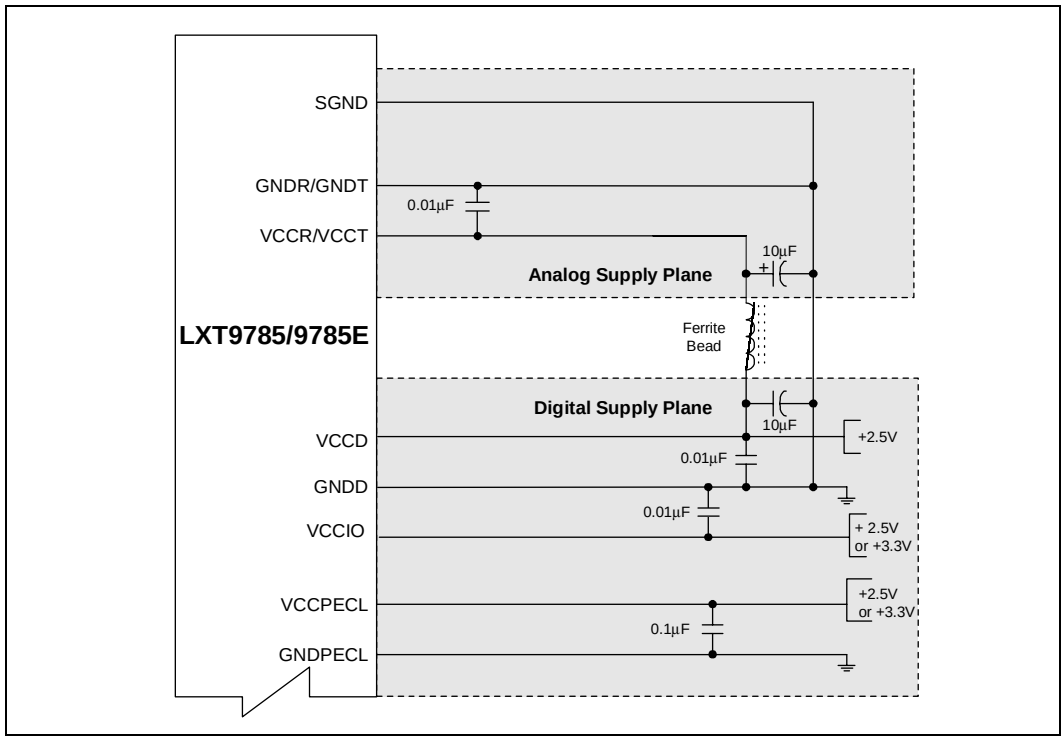
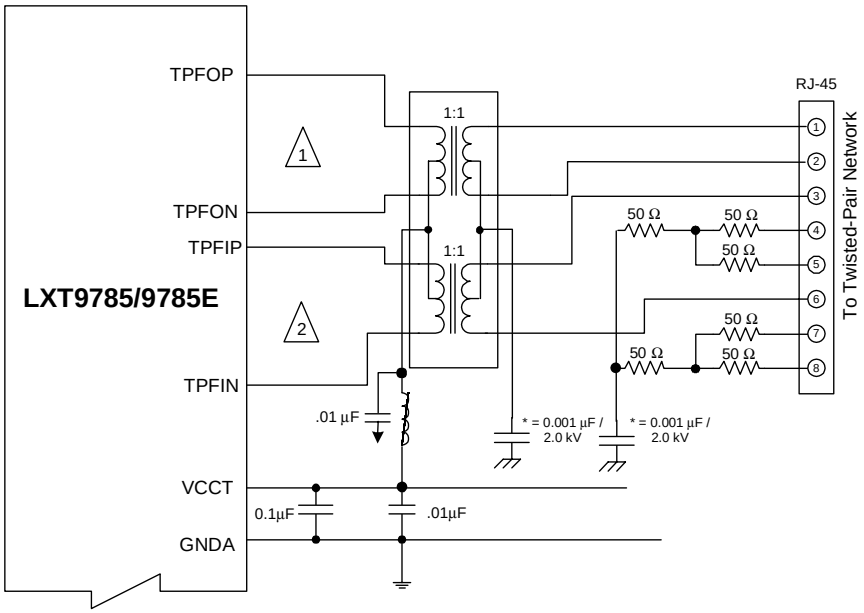
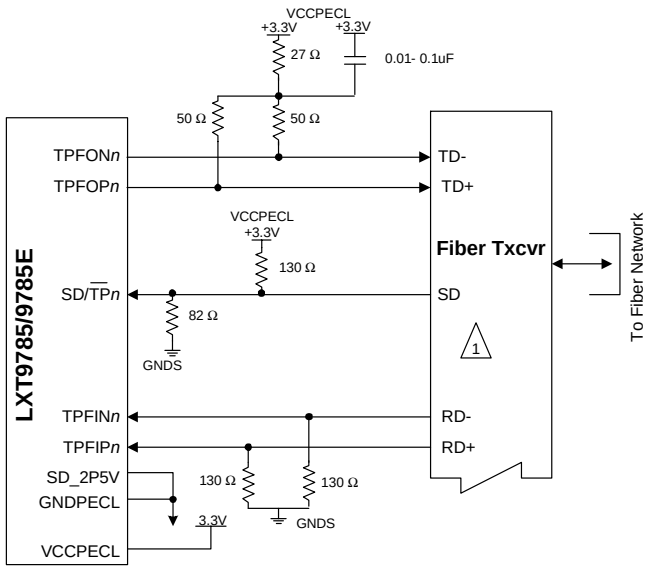


Figure 36. Typical Twisted-Pair Interface



1. The 100Ω transmit load termination resistor typically required is integrated in the LXT9785/9785E.
2. The 100Ω receive load termination resistor typically required is integrated in the LXT9785/9785E.

Figure 37. Typical Fiber Interface



1. The SD_2P5V pin must be connected to the VCCPECL supply.

4.0 Test Specifications

Note: Table 27 through Table 56 on page 124 and Figure 38 on page 104 through Figure 61 on page 124 represent the target specifications of the LXT9785/9785E. These specifications are not guaranteed and are subject to change without notice. Minimum and maximum values listed in Table 29 on page 101 through Table 56 on page 124 apply over the recommended operating conditions specified in Table 28.

Table 27. Absolute Maximum Ratings

Parameter		Sym	Min	Max	Units
Supply voltage		VCC	-0.3	3.46	V
Operating temperature	Ambient	TOPA	0	+85	ºC
	Case	TOPC	–	+120	ºC
Storage temperature		TST	-65	+150	ºC

Caution: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 28. Operating Conditions

Parameter		Sym	Min	Typ[1] (2.5 VCCIO)	Typ[1] (3.3 VCCIO)	Max	Units
Operating temperature	Ambient	TOPA	0	–	–	70	ºC
	Case	TOPC	0	–	–	108	ºC
Supply voltage[2]	Analog & Digital	Vcca, Vccd	2.38	2.5	2.5	2.63	V
	I/O	Vccio	2.38	2.5	3.3	3.46	V
	I/O (SD_2P5V = 0)	VCCPECL	3.14	N/A	3.3	3.46	V
	I/O (SD_2P5V = 1)		2.38	2.5	N/A	2.63	V
Operating Current - RMII	100BASE-TX	ICC	–	780		810	mA
		ICCIO	–	60	130	160	mA
	100BASE-FX	ICC	–	380		410	mA
		ICCIO	–	90	170	200	mA
	10BASE-T	ICC	–	710		765	mA
		ICCIO	–	30	70	90	mA
	Power-Down Mode Hardware	ICC	–	20		20	mA
		ICCIO	–	2	3	4	mA
	Auto-Negotiation	ICC	–	500		540	mA
		ICCIO	–	2	4	4	mA

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Voltages with respect to ground unless otherwise specified.

Table 28. Operating Conditions (Continued)

Parameter		Sym	Min	Typ[1] (2.5 VCCIO)	Typ[1] (3.3 VCCIO)	Max	Units
Operating Current - SMII	100BASE-TX	ICC	–	800		830	mA
		ICCIO	–	70	130	160	mA
	100BASE-FX	ICC	–	380		410	mA
		ICCIO	–	90	170	200	mA
	10BASE-T	ICC	–	740		770	mA
		ICCIO	–	60	110	130	mA
	Power-Down Mode Hardware	ICC	–	50		50	mA
		ICCIO	–	3	5	5	mA
	Auto-Negotiation	ICC	–	520		570	mA
		ICCIO	–	20	30	30	mA
Operating Current - SS-SMII	100BASE-TX	ICC	–	800		835	mA
		ICCIO	–	90	170	200	mA
	100BASE-FX	ICC	–	380		410	mA
		ICCIO	–	90	170	200	mA
	10BASE-T	ICC	–	740		770	mA
		ICCIO	–	90	150	180	mA
	Power-Down Mode Hardware	ICC	–	30		40	mA
		ICCIO	–	3	5	5	mA
	Auto-Negotiation	ICC	–	530		570	mA
		ICCIO	–	50	70	80	mA

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Voltages with respect to ground unless otherwise specified.

Table 29. Digital I/O DC Electrical Characteristics (VCCIO = 2.5V +/- 5%)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage	VIL	–	–	0.75	V	–
Input High voltage	VIH	1.75	–	–	V	–
Input current	II	-100	–	100	µA	0.0 < VI < VCC
Output Low voltage	VOL	–	–	0.2	V	IOL = 4 mA
Output Low voltage ($\overline{\text{LED}m\_n}$ pins)	VOL-LED	–	–	0.5	V	IOL = 10 mA
Output High voltage	VOH	2.07	–	–	V	IOH = -4 mA
Input Low voltage SD pins	VIL-SD	–	–	0.755	V	–
Input High voltage SD pins	VIH-SD	1.58	–	–	V	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 30. Digital I/O DC Electrical Characteristics (VCCIO = 3.3V +/- 5%)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage	V_{IL}	–	–	0.8	V	–
Input High voltage	V_{IH}	2.0	–	–	V	–
Input current	I_I	-100	–	100	µA	$0.0 < V_I < V_{CC}$
Output Low voltage	V_{OL}	–	–	0.2	V	I_{OL} = 4 mA
Output Low voltage ($\overline{LEDm\_n}$ pins)	V_{OL}-LED	–	–	0.4	V	I_{OL} = 10 mA
Output High voltage	V_{OH}	2.4	–	–	V	I_{OH} = -4 mA
Input Low voltage SD pins	V_{IL}-SD	–	–	1.515	V	–
Input High voltage SD pins	V_{IH}-SD	2.42	–	–	V	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 31. Required Clock Characteristics

Parameter	Sym	Min	Typ[2]	Max	Units	Test Conditions
SMII Input frequency	f	–	125	–	MHz	–
RMII Input frequency	f	–	50	–	MHz	–
Input clock frequency tolerance[1]	Δf	–	–	± 50	ppm	–
Input clock duty cycle[1]	Tdc	35	50	65	%	RMII selection
Input clock duty cycle - REFCLK, TxCLK[1]	Tdc	40	50	60	%	SMII/SS-SMII selection
Output RxCLK duty cycle	Tdc	45	50	55	%	SS-SMII only

1. Parameter is guaranteed by design; not subject to production testing.
2. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 32. 100BASE-TX Transceiver Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Peak differential output voltage	V_P	0.95	–	1.05	V	Note 2
Signal amplitude symmetry	Vss	98	–	102	%	Note 2
Signal rise/fall time	t_{rf}	3	–	5	ns	Note 2
Rise/fall time symmetry	t_{rfs}	–	–	0.5	ns	Note 2
Duty cycle distortion	–	–	–	+/- 0.5	ns	Offset from 16 ns pulse width at 50% of pulse peak
Overshoot	V_O	–	–	5	%	–
Jitter magnitude (measured differentially)	$t_{tx\text{-}jit}$	–	–	1.4	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Measured at the line side of the transformer, line replaced by 100Ω (+/-1%) resistor.

Table 33. 100BASE-FX Transceiver Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Transmitter						
Peak differential output voltage (single ended)	VOP	0.6	1.44	–	V	–
Signal rise/fall time	t_{rf}	–	–	1.6	ns	10 to 90%, 2.0 pF load
Jitter magnitude (measured differentially)	$t_{tx\text{-}jit}$	–	–	1.4	ns	–
Receiver						
Peak differential input voltage	VIP	0.55	–	–	V	–
Common mode input range	VCMIR	–	–	VCC - 0.5	V	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 34. 10BASE-T Transceiver Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Transmitter						
Peak differential output voltage	VOP	2.2	2.5	2.8	V	Note 2
Link transmit period	–	8	–	24	ms	–
Jitter magnitude added by the MAU and PLS sections [3, 4]	$t_{tx\text{-}jit}$	–	–	11	ns	–
Receiver						
Receive input impedance[3]	ZIN	–	100	–	W	Between TPFIP and TPFIN
Link min receive timer	TLRmin	2	–	7	ms	–
Link max receive timer	TLRmax	50	–	150	ms	–
Differential squelch threshold	VDS	–	475	–	mV Peak	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.
3. IEEE 802.3 specifies maximum jitter addition at 1.5 ns for the AUI cable, 0.5 ns from the encoder, and 3.5 ns from the MAU.
4. After line model specified by IEEE 802.3 for 10BASE-T MAU.

Figure 38. SMII - 100BASE-TX Receive Timing

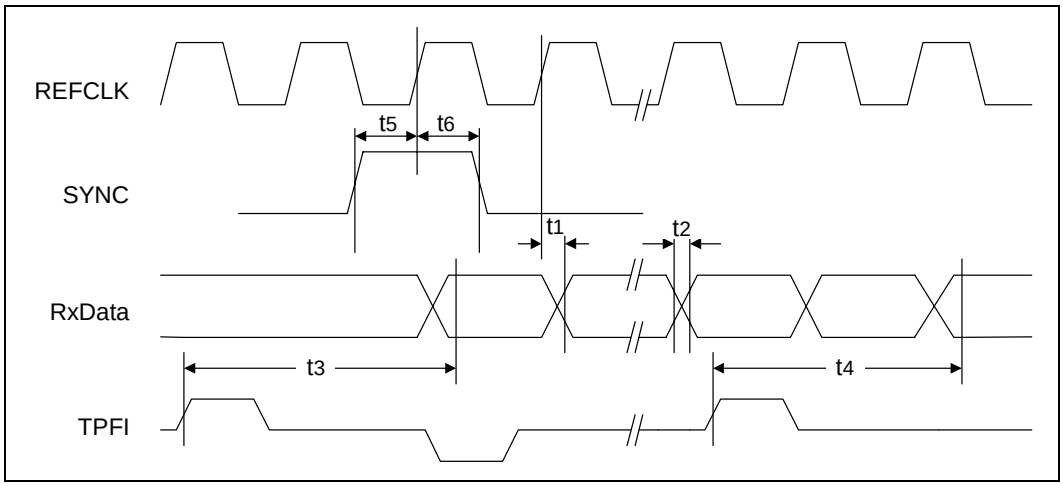


Table 35. SMII - 100BASE-TX Receive Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
RxData output delay from REFCLK rising edge	t1	1.5	–	5	ns	Minimum C_L = 5 pF Maximum C_L = 20 pF
RxData Rise/Fall Time	t2	–	1.0	–	ns	–
Receive start of /J/ to CRS asserted	t3	–	21	29	BT[2]	Synchronous sampling of SMII
Receive start of /T/ to CRS de-asserted	t4	–	25	30	BT[2]	Synchronous sampling of SMII
SYNC setup to REFCLK rising edge	t5	1.5	–	–	ns	–
SYNC hold from REFCLK rising edge	t6	1.0	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (i.e., BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Figure 39. SMII - 100BASE-TX Transmit Timing

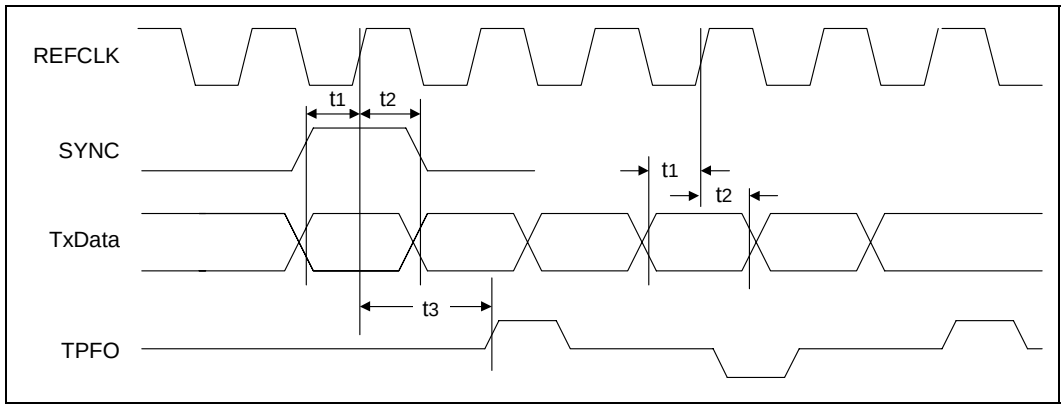


Table 36. SMII - 100BASE-TX Transmit Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
SYNC setup to REFCLK rising edge and TxData setup to REFCLK rising edge	t1	1.5	–	–	ns	–
SYNC hold from REFCLK rising edge and TxData hold from REFCLK rising edge	t2	1.0	–	–	ns	–
TxEN sampled to start of /J/	t3	–	11	14	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (i.e., BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Figure 40. SMII - 100BASE-FX Receive Timing

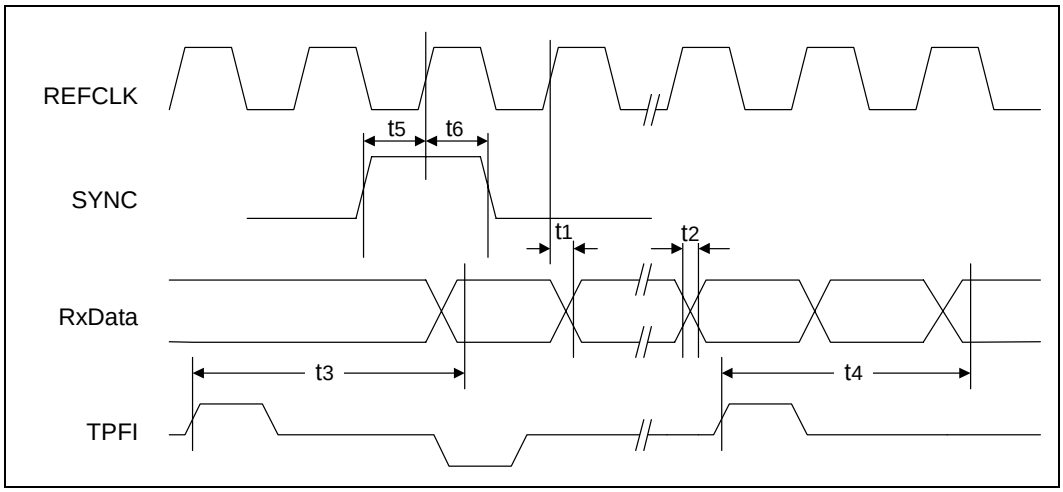


Table 37. SMII - 100BASE-FX Receive Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
RxData output delay from REFCLK rising edge	t1	1.5	–	5	ns	Minimum C_L = 5 pF Maximum C_L = 20 pF
RxData Rise/Fall Time	t2	–	1	–	ns	–
Receive start of /J/ to CRS asserted	t3	–	18	26	BT[2]	Synchronous sampling of SMII
Receive start of /T/ to CRS de-asserted	t4	–	23	27	BT[2]	Synchronous sampling of SMII
SYNC setup to REFCLK rising edge	t5	1.5	–	–	ns	–
SYNC hold from REFCLK rising edge	t6	1.0	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (i.e., BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Figure 41. SMII - 100BASE-FX Transmit Timing

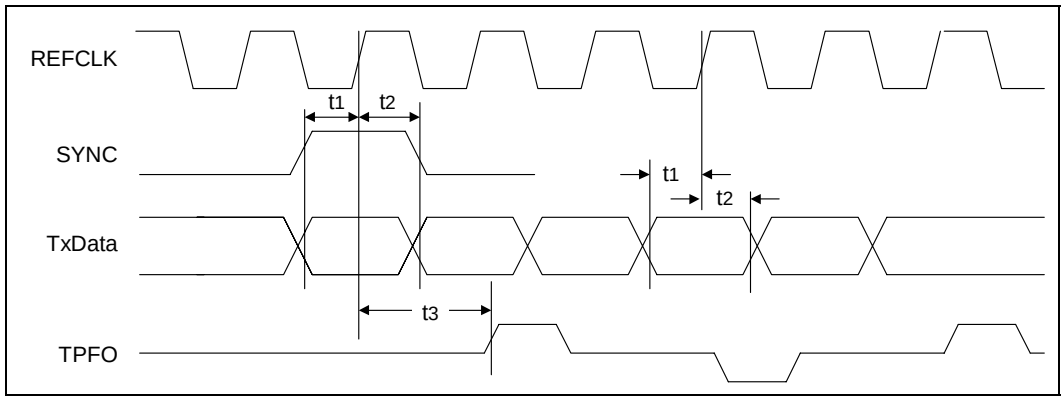


Table 38. SMII - 100BASE-FX Transmit Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
SYNC setup to REFCLK rising edge and TxData setup to REFCLK rising edge	t1	1.5	–	–	ns	–
SYNC hold from REFCLK rising edge and TxData hold from REFCLK rising edge	t2	1.0	–	–	ns	–
TxEN sampled to start of /J/	t3	–	10	13	BT[2]	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (i.e., BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Figure 42. SMII - 10BASE-T Receive Timing

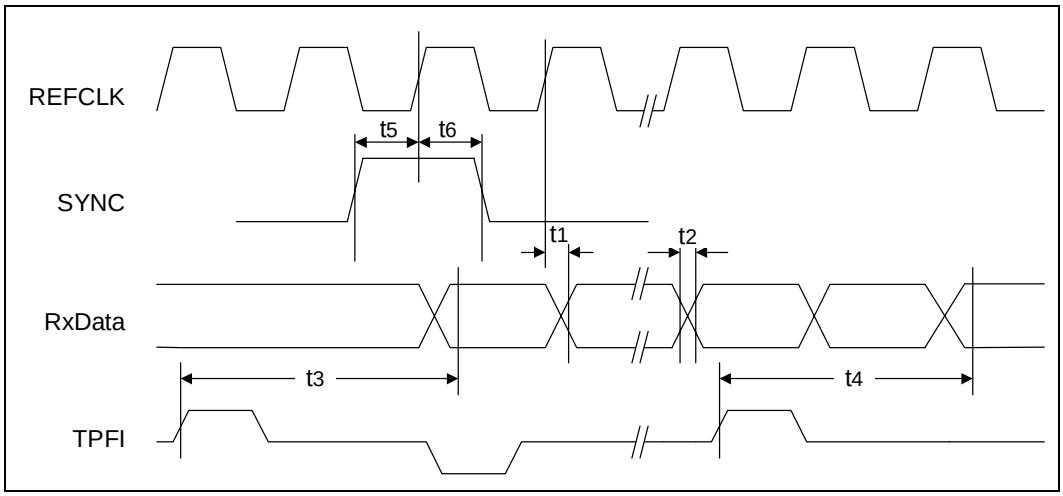


Table 39. SMII - 10BASE-T Receive Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
RxData output delay from REFCLK rising edge	t1	1.5	–	5	ns	Minimum C_L = 5 pF Maximum C_L = 20 pF
RxData Rise/Fall Time	t2	–	1	–	ns	–
Receive Start-of-Frame to CRS asserted	t3	–	17	18	BT[3]	Synchronous sampling of SMII[2]
Receive Start-of-Idle to CRS de-asserted	t4	–	17	18	BT[3]	Synchronous sampling of SMII[2]
SYNC setup to REFCLK rising edge	t5	1.5	–	–	ns	–
SYNC hold from REFCLK rising edge	t6	1.0	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Assumes each SMII segment is sampled for CRS.
3. “BT” signifies bit times at the line rate (i.e., BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Figure 43. SMII - 10BASE-T Transmit Timing

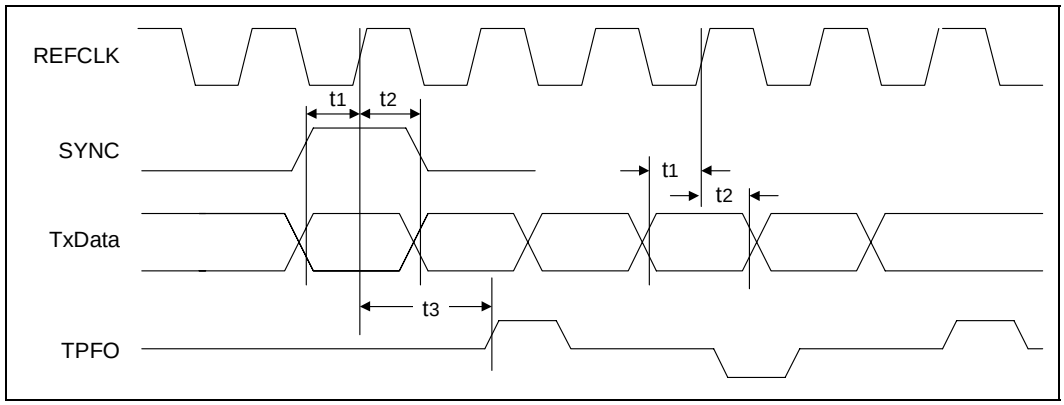


Table 40. SMII-10BASE-T Transmit Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
SYNC setup to REFCLK rising edge and TxData setup to REFCLK rising edge	t1	1.5	–	–	ns	–
SYNC hold to REFCLK rising edge and TxData hold from REFCLK rising edge	t2	1.0	–	–	ns	–
TxEN sampled to start-of-frame	t3	–	10	12.5	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (i.e., BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Figure 44. SS-SMII - 100BASE-TX Receive Timing

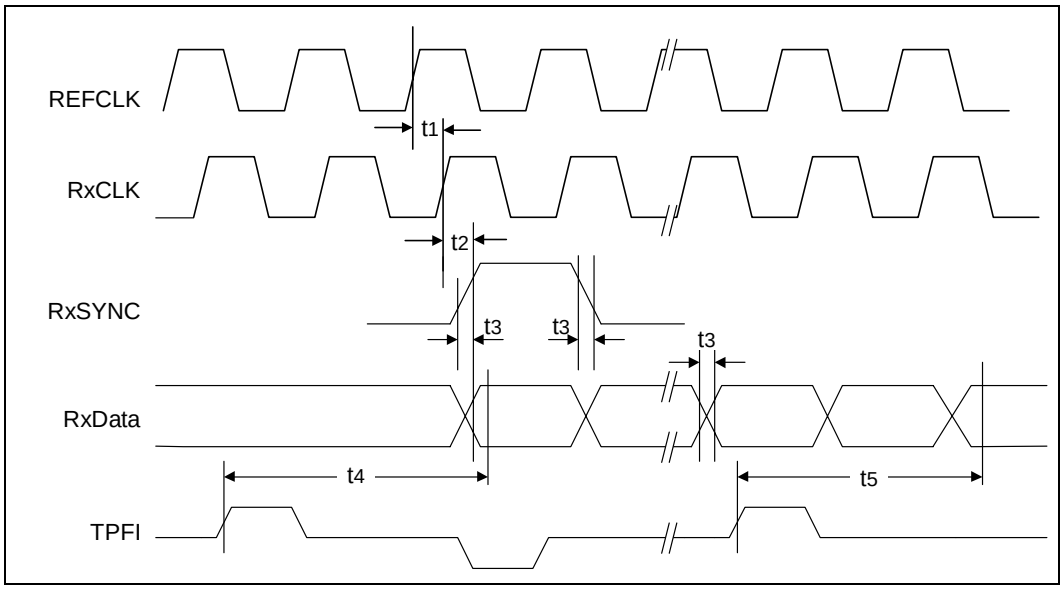


Table 41. SS-SMII - 100BASE-TX Receive Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
REFCLK rising edge to RxCLK rising edge	t1	–	1.5	–	ns	–
RxData/RxSYNC output delay from RxCLK rising edge	t2	1.5	–	5	ns	Minimum C_L = 5pF Maximum C_L = 40pF
RxData/RxSYNC Rise/Fall time	t3	–	1.0	–	ns	–
Receive start of /J/ to CRS asserted	t4	–	21	25	BT[2]	–
Receive start of /T/ to CRS de-asserted	t5	–	25	30	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (i.e., BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Figure 45. SS-SMII - 100BASE-TX Transmit Timing

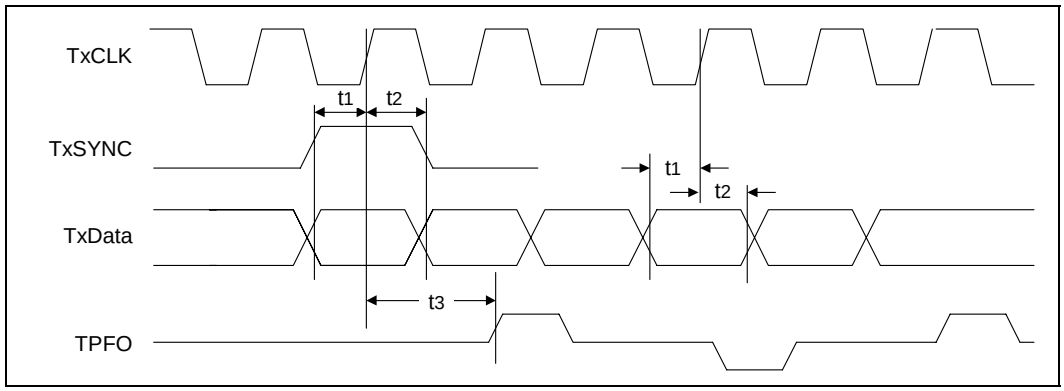


Table 42. SS-SMII - 100BASE-TX Transmit Timing

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
TxSYNC setup to TxCLK rising edge and TxData setup to TxCLK rising edge	t1	1.5	–	–	ns	–
TxSYNC hold from TxCLK rising edge and TxData hold to TxCLK rising edge	t2	1.0	–	–	ns	–
TxEN sampled to start of /J/	t3	–	11	14	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (i.e., BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Figure 46. SS-SMII - 100BASE-FX Receive Timing

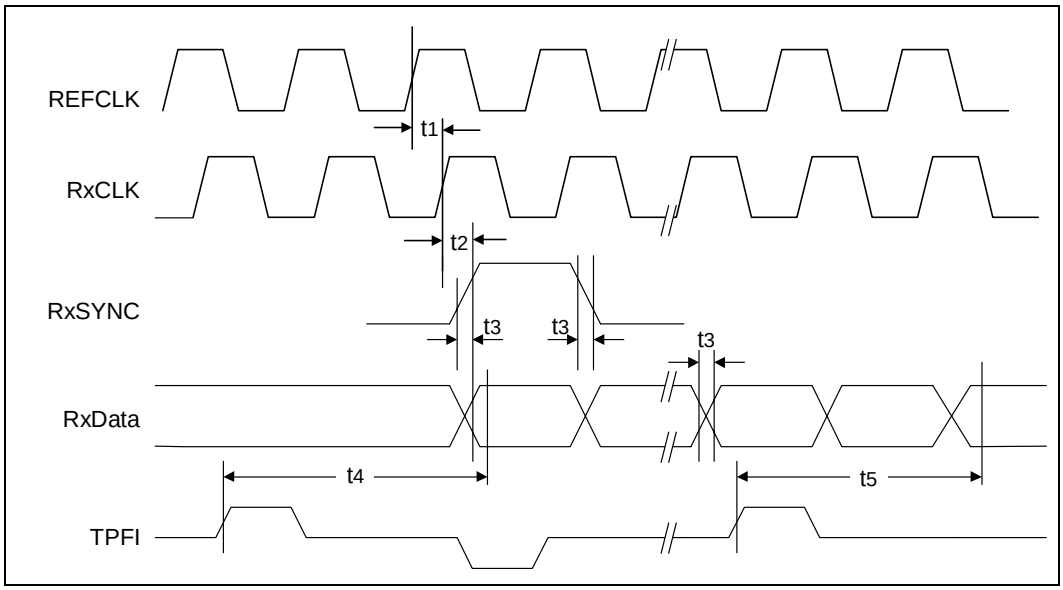


Table 43. SS-SMII - 100BASE-FX Receive Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
REFCLK rising edge to RxCLK rising edge	t1	–	1.5		ns	–
RxData/RxSYNC output delay from RxCLK rising edge	t2	1.5	–	5	ns	Minimum C_L = 5pF Maximum C_L = 40pF
RxData/RxSYNC Rise/Fall time	t3	–	1	–	ns	–
Receive start of /J/ to CRS asserted	t4	–	18	23	BT[2]	–
Receive start of /T/ to CRS de-asserted	t5	–	21	26	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (i.e., BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Figure 47. SS-SMII - 100BASE-FX Transmit Timing

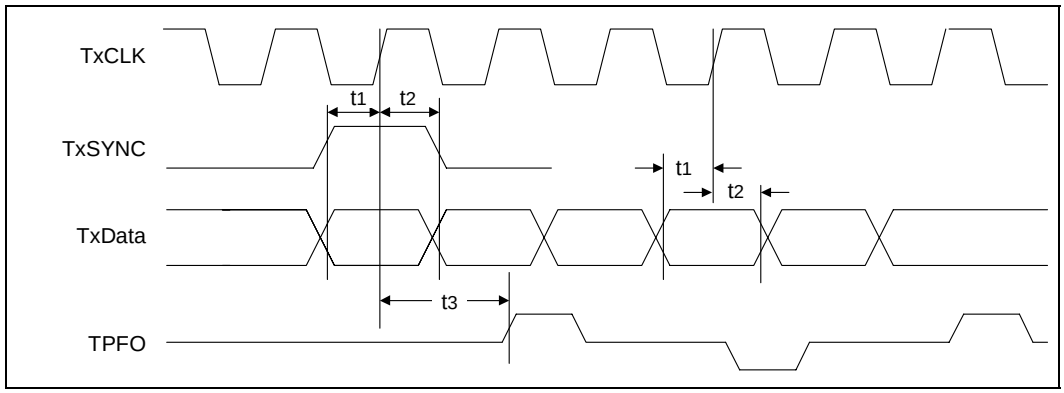


Table 44. SS-SMII - 100BASE-FX Transmit Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
TxSYNC setup to TxCLK rising edge and TxData setup to TxCLK rising edge	t1	1.5	–	–	ns	–
TxSYNC hold from TxCLK rising edge and TxData hold to TxCLK rising edge	t2	1.0	–	–	ns	–
TxData to TPFO Latency	t3	–	11	13	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (i.e., BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Figure 48. SS-SMII - 10BASE-T Receiving Timing

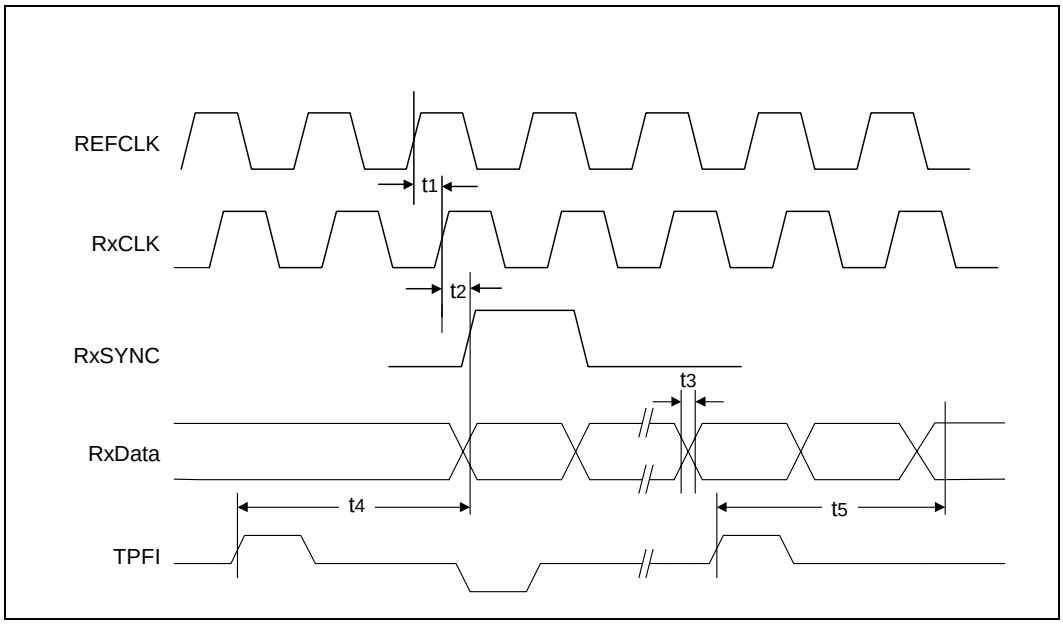


Table 45. SS-SMII - 10BASE-T Receive Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
REFCLK rising edge to RxCLK rising edge	t1	–	1.5	–	ns	–
RxData/RxSYNC output delay from RxCLK rising edge	t2	1.5	–	5	ns	Minimum C_L = 5pF Maximum C_L = 40pF
RxData/RxSYNC Rise/Fall time	t3	–	1	–	ns	–
Receive Start-of-Frame to CRS asserted	t4	–	10	11	BT[3]	Synchronous sampling of SMII[2]
Receive Start-of-Idle to CRS de-asserted	t5	–	18	19	BT[3]	Synchronous sampling of SMII[2]

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Assumes each SMII segment is sampled for CRS.
3. “BT” signifies bit times at the line rate (i.e., BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Figure 49. SS-SMII - 10BASE-T Transmit Timing

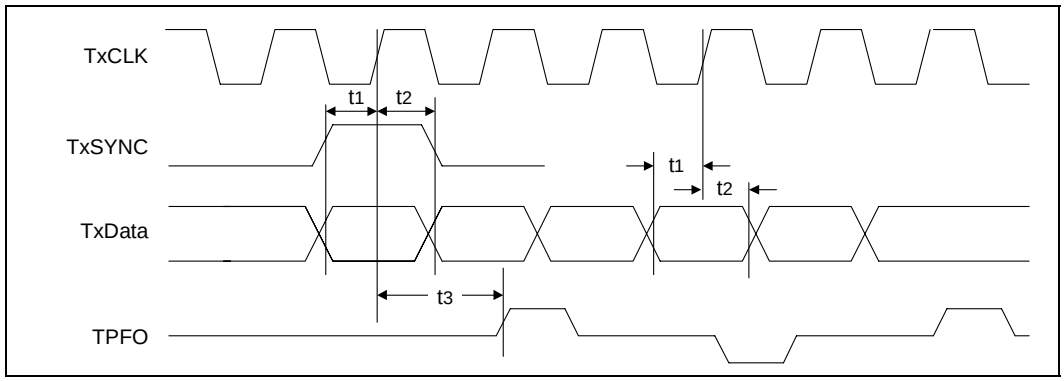


Table 46. SS-SMII - 10BASE-T Transmit Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
TxSYNC setup to TxCLK rising edge and TxData setup to TxCLK rising edge	t1	1.5	–	–	ns	–
TxSYNC hold to TxCLK rising edge and TxData hold from TxCLK rising edge	t2	1.0	–	–	ns	–
TxData to TPFO Latency	t3	–	10	12.5	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (i.e., BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Figure 50. RMII - 100BASE-TX Receive Timing

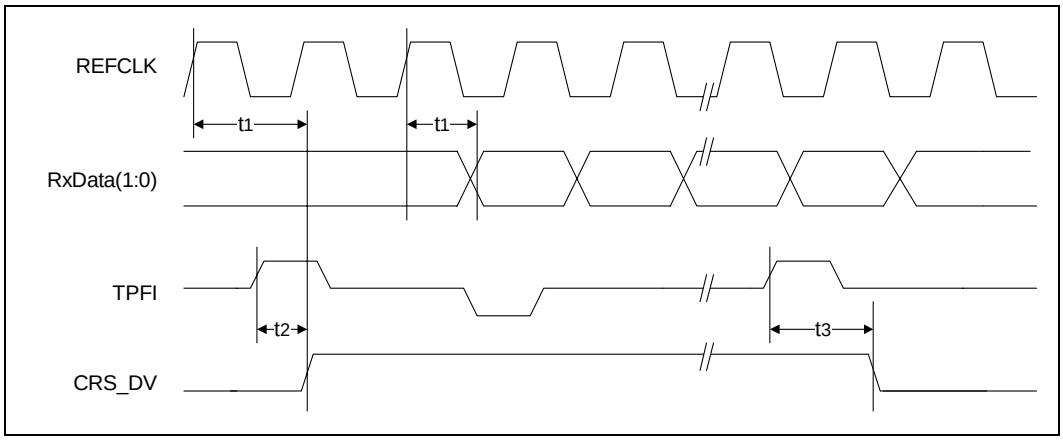


Table 47. RMII - 100BASE-TX Receive Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
RxData<1:0>/CRS_DV output delay from REFCLK rising edge[3]	t1	2	–	14	ns	–
Receive start of /J/ to CRS_DV asserted	t2	–	16	20	BT[2]	–
Receive start of /T/ to CRS_DV de-asserted	t3	–	20	27	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (i.e., BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).
3. Values and conditions from RMII Specification, Rev. 1.2.

Figure 51. RMII - 100BASE-TX Transmit Timing

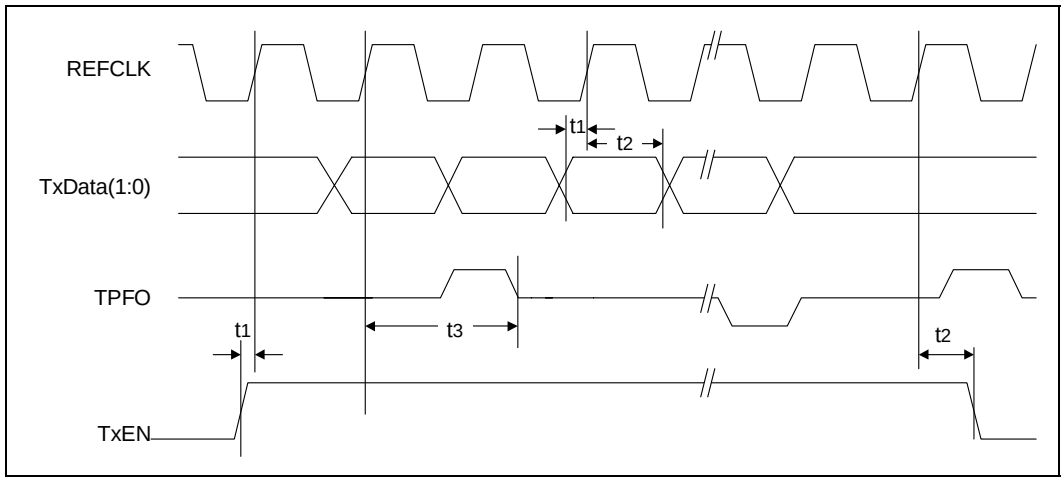


Table 48. RMII - 100BASE-TX Transmit Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
TxData<1:0>/TxEN setup to REFCLK rising edge	t1	4	–	–	ns	–
TxData<1:0>/TxEN hold from REFCLK rising edge	t2	2	–	–	ns	–
TxEN sampled to TPFO out (Tx latency)	t3	–	12	13	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (i.e., BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Figure 52. RMII - 100BASE-FX Receive Timing

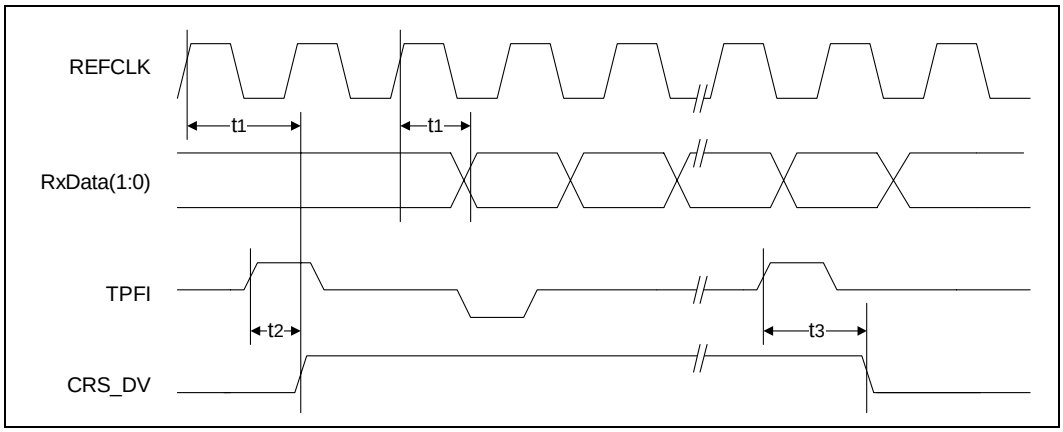


Table 49. RMII - 100BASE-FX Receive Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
RxData<1:0>/CRS_DV output delay from REFCLK rising edge[3]	t1	2	–	14	ns	–
Receive start of /J/ to CRS_DV asserted	t2	–	14	18	BT[2]	–
Receive start of /T/ to CRS_DV de-asserted	t3	–	18	25	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (i.e., BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).
3. Values and conditions from RMII Specification, Rev. 1.2.

Figure 53. RMII - 100BASE-FX Transmit Timing

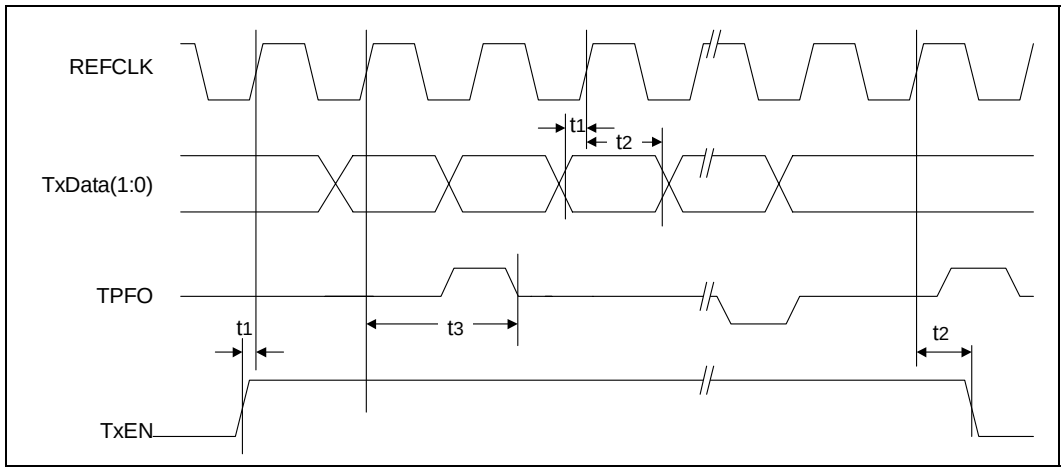


Table 50. RMII - 100BASE-FX Transmit Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
TxData<1:0>/TxEN setup to REFCLK rising edge	t1	4	–	–	ns	–
TxData<1:0>/TX-EN hold from REFCLK rising edge	t2	2	–	–	ns	–
TxEN sampled to TPFO out (Tx latency)	t3	–	10	12	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (i.e., BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Figure 54. RMII - 10BASE-T Receive Timing

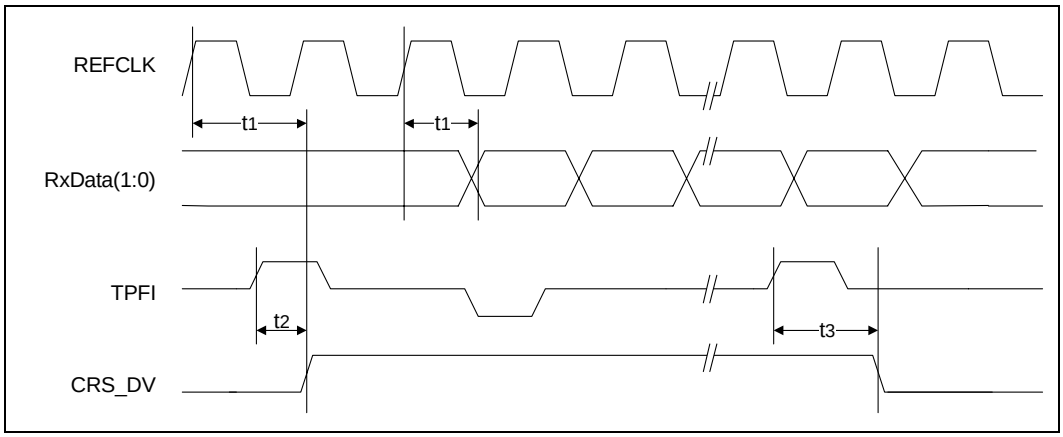


Table 51. RMII - 10BASE-T Receive Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
RxData<1:0>/CRS_DV output delay from REFCLK rising edge[3]	t1	2	–	14	ns	–
TPFI in to CRS_DV asserted	t2	1.5	3	4	BT[2]	–
TPFI quiet to CRS_DV de-asserted	t3	14	15	16	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (i.e., BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).
3. Values and conditions from RMII Specification, Rev. 1.2.

Figure 55. RMII - 10BASE-T Transmit Timing

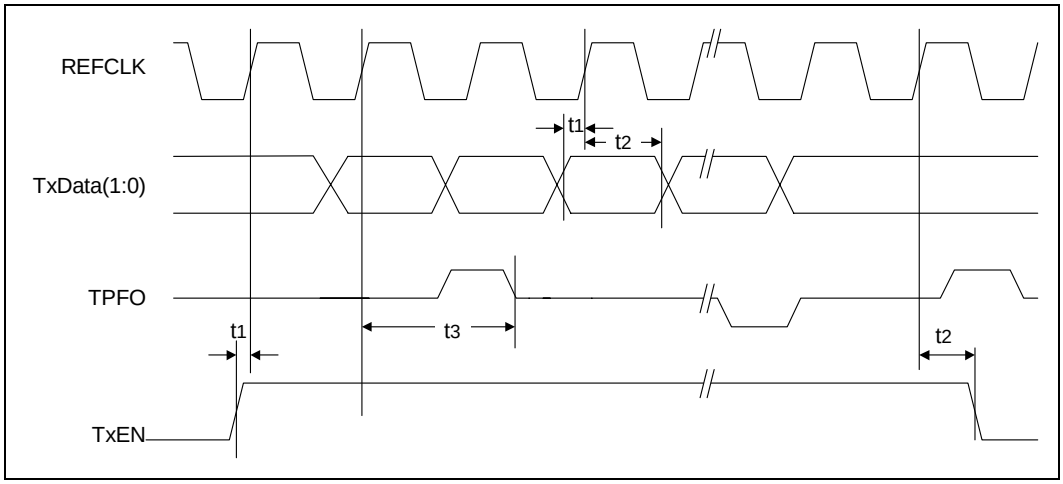


Table 52. RMII - 10BASE-T Transmit Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
TxData<1:0>/TxEN setup to REFCLK rising edge	t1	4	–	–	ns	–
TxData<1:0>/TxEN hold from REFCLK rising edge	t2	2	–	–	ns	–
TxEN sampled to TPFO out (Tx latency)	t3	–	8.5	10.5	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (i.e., BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Figure 56. Auto-Negotiation and Fast Link Pulse Timing

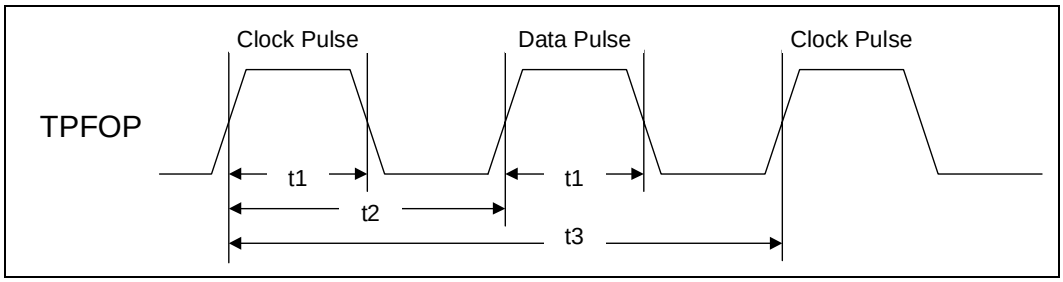


Figure 57. Fast Link Pulse Timing

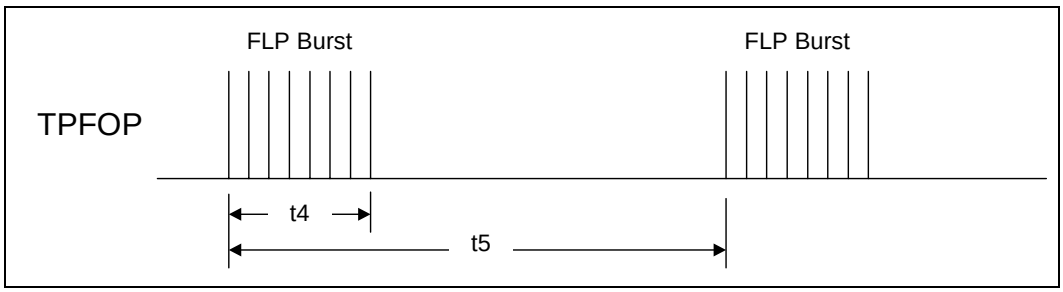


Table 53. Auto-Negotiation and Fast Link Pulse Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Clock/Data pulse width	t1	–	100	–	ns	–
Clock pulse to Data pulse	t2	55.5	–	69.5	µs	–
Clock pulse to Clock pulse	t3	111	–	139	µs	–
FLP burst width	t4	–	2	–	ms	–
FLP burst to FLP burst	t5	8	–	24	ms	–
Clock/Data pulses per burst	–	17	–	33	ea	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 58. MDIO Write Timing (MDIO Sourced by MAC)

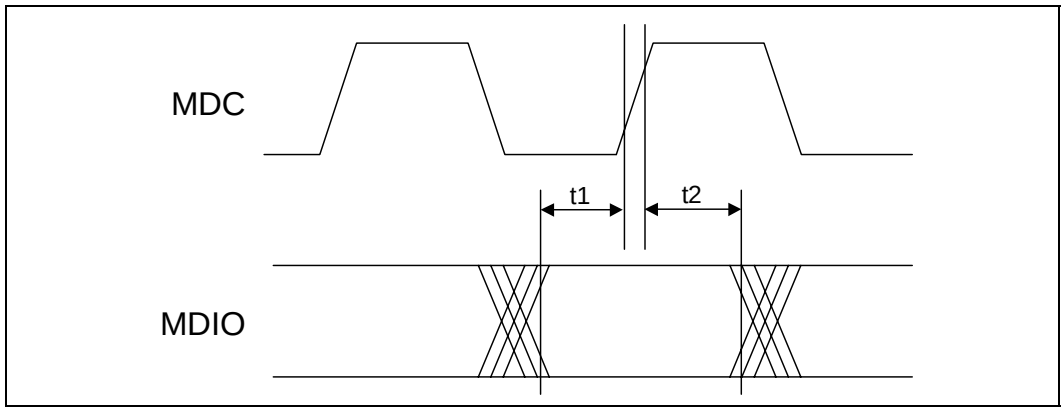


Figure 59. MDIO Read Timing (MDIO Sourced by PHY)

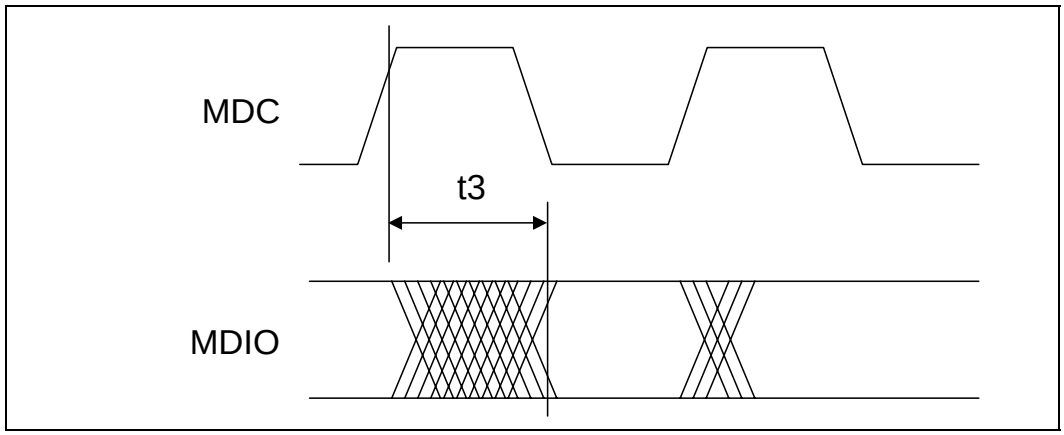


Table 54. MDIO Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
MDIO setup before MDC, sourced by STA	t1	10	–	–	ns	–
MDIO hold after MDC, sourced by STA	t2	10	–	–	ns	–
MDC to MDIO output delay, sourced by PHY	t3	0	–	40	ns	–

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Figure 60. Power-Up Timing

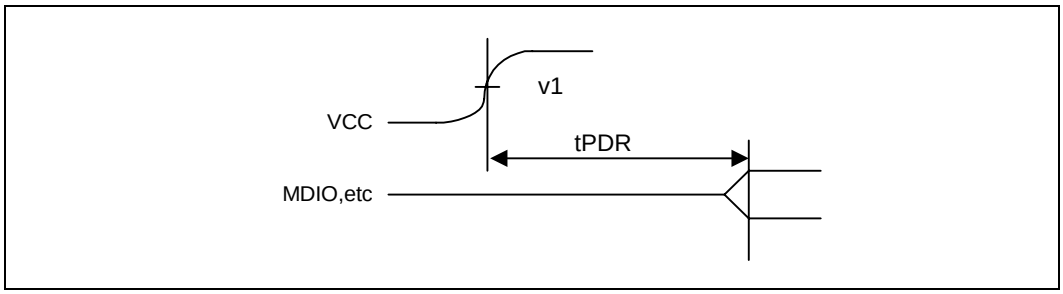


Table 55. Power-Up Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Voltage Threshold	v1	2.1	–	–	V	–
Power-Up recovery time	tPDR	100	–	–	ms	–

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Figure 61. $\overline{\text{Reset}}$ Recovery Timing

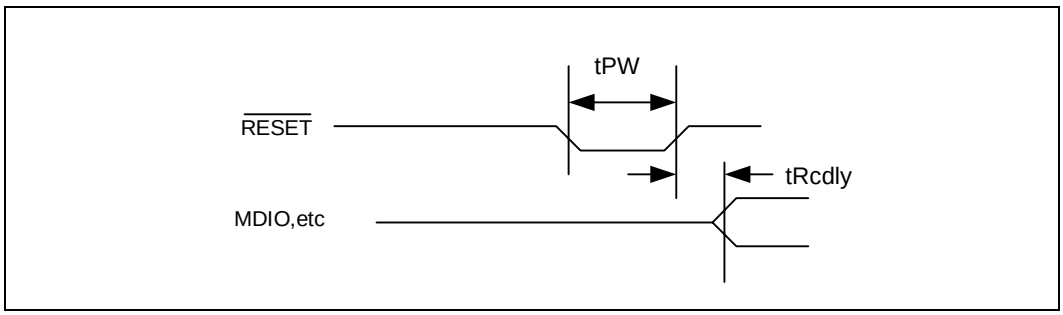


Table 56. $\overline{\text{Reset}}$ Recovery Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Reset pulse width	tPW	10	–	–	ns	–
Reset recovery delay	tRcdly	0.4	–	–	ms	–

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

5.0 Register Definitions

The LXT9785/9785E register set includes multiple 16-bit registers, 17 registers per port. Table 57 presents a complete register listing. Table 58 on page 126 through Table 73 on page 139 define individual registers and Table 76 on page 141 provides a consolidated memory map of all registers.

Base Registers (0 through 8) are defined in accordance with the “Reconciliation Sublayer and Media Independent Interface” and “Physical Layer Link Signalling for 10/100 Mbps Auto-Negotiation” sections of the IEEE 802.3 standard.

Additional Registers (16 through 20) are defined in accordance with the IEEE 802.3 standard for adding unique chip functions.

Table 57. Register Set

Address	Register Name	Bit Assignments
0	Control Register	Refer to Table 58 on page 126
1	Status Register	Refer to Table 59 on page 127
2	PHY Identification Register 1	Refer to Table 60 on page 128
3	PHY Identification Register 2	Refer to Table 61 on page 128
4	Auto-Negotiation Advertisement Register	Refer to Table 62 on page 129
5	Auto-Negotiation Link Partner Base Page Ability Register	Refer to Table 63 on page 130
6	Auto-Negotiation Expansion Register	Refer to Table 64 on page 131
7	Auto-Negotiation Next Page Transmit Register	Refer to Table 65 on page 131
8	Auto-Negotiation Link Partner Next Page Receive Register	Refer to Table 66 on page 132
9	1000BASE-T/100BASE-T2 Control Register	Not Implemented
10	1000BASE-T/100BASE-T2 Status Register	Not Implemented
15	Extended Status Register	Not Implemented
16	Port Configuration Register	Refer to Table 67 on page 133
17	Quick Status Register	Refer to Table 68 on page 134
18	Interrupt Enable Register	Refer to Table 69 on page 135
19	Interrupt Status Register	Refer to Table 70 on page 136
20	LED Configuration Register	Refer to Table 71 on page 137
21	Receive Error Count Register	Refer to Table 72 on page 138
22	Reserved	
23 - 24	Reserved	
25	RMII Out-of-Band Signalling Register	Refer to Table 73 on page 139
26	Reserved	
27	Trim Enable Register	Refer to Table 74 on page 140
28-31	Reserved	

Table 58. Control Register (Address 0)

Bit	Name	Description	Type [2]	Default
0.15	$\overline{\text{RESET}}$	1 = PHY reset 0 = normal operation	R/W SC	0[1]
0.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W	0
0.13	Speed Selection	0.6 / 0.13 1 / 1 = Reserved 1 / 0 = 1000 Mbps (not allowed) 0 / 1 = 100 Mbps 0 / 0 = 10 Mbps	R/W	LSHR[3,4]
0.12	Auto-Negotiation Enable	1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process	R/W	LSHR[3,4]
0.11	Power-Down	1 = power-down 0 = normal operation	R/W	0
0.10	Isolate	1 = Electrically isolate PHY from RMII or SMII interface 0 = normal operation	R/W	0
0.9	Restart Auto-Negotiation	1 = Restart Auto-Negotiation Process 0 = normal operation	R/W SC	0[1]
0.8	Duplex Mode	1 = Full Duplex 0 = Half Duplex	R/W	LSHR[3,4]
0.7	Collision Test	This bit is ignored by the LXT9785/9785E 1 = Enable COL signal test 0 = Disable COL signal test	R/W	0
0.6	Speed Selection 1000 Mbps	0.6 / 0.13 1 / 1 = Reserved 1 / 0 = 1000 Mbps (not allowed) 0 / 1 = 100 Mbps 0 / 0 = 10 Mbps	R/W	0
0.5:0	Reserved	Write as 0, ignore on Read	R/W	00000

1. During a hardware reset, all LHR information is latched in from the pins. During a software reset (0.15), the LHR information is not re-read from the pins. This information reverts back to the information that was read in during the hardware reset. During a hardware rest, register information is unavailable from 1 ms after de-assertion of the reset. During a software reset (0.15) the registers are available for reading. The reset bit should be polled to see when the part has completed reset.
2. R/W = Read/Write, RO = Read Only, SC = Self Clearing when read.
3. LSHR = Default value is derived from a single device input pin state or a group of device input pin states as the pin(s) are latched at startup or hardware reset.
4. Default value of bits 0.12, 0.13, and 0.8 are determined by the CFG pins as described in Table 18 on page 62.

Table 59. Status Register (Address 1)

Bit	Name	Description	Type [1]	Default
1.15	100BASE-T4	1 = PHY able to perform 100BASE-T4 0 = PHY not able to perform 100BASE-T4	RO	0
1.14	100BASE-X Full Duplex	1 = PHY able to perform full-duplex 100BASE-X 0 = PHY not able to perform full-duplex 100BASE-X	RO	1
1.13	100BASE-X Half Duplex	1 = PHY able to perform half-duplex 100BASE-X 0 = PHY not able to perform half-duplex 100BASE-X	RO	1
1.12	10 Mbps Full Duplex	1 = PHY able to operate at 10 Mbps in full-duplex mode 0 = PHY not able to operate at 10 Mbps full-duplex mode	RO	1
1.11	10 Mbps Half Duplex	1 = PHY able to operate at 10 Mbps in half-duplex mode 0 = PHY not able to operate at 10 Mbps in half-duplex	RO	1
1.10	100BASE-T2 Full Duplex	1 = PHY able to perform full-duplex 100BASE-T2 0 = PHY not able to perform full-duplex 100BASE-T2	RO	0
1.9	100BASE-T2 Half Duplex	1 = PHY able to perform half duplex 100BASE-T2 0 = PHY not able to perform half-duplex 100BASE-T2	RO	0
1.8	Extended Status	1 = Extended status information in Register 15 0 = No extended status information in Register 15	RO	0
1.7	Reserved	1 = Ignore on read	RO	0
1.6	MF Preamble Suppression	1 = PHY accepts management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed	RO	0
1.5	Auto-Negotiation complete	1 = Auto-negotiation complete 0 = Auto-negotiation not complete	RO	0
1.4	Remote Fault	1 = Remote fault condition detected 0 = No remote fault condition detected	RO/LH Note 2	0
1.3	Auto-Negotiation Ability	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation	RO	1
1.2	Link Status	1 = Link is up 0 = Link is down	RO/LL Note 2	0
1.1	Jabber Detect	1 = Jabber condition detected 0 = Jabber condition not detected	RO/LH Note 2	0
1.0	Extended Capability	1 = Extended register capabilities 0 = Basic register capabilities	RO	1

1. RO = Read Only
2. Bits that Latch High (LH) or Latch Low (LL) automatically clear when read.

Table 60. PHY Identification Register 1 (Address 2)

Bit	Name	Description	Type [1]	Default
2.15:0	PHY ID Number	The PHY identifier composed of bits 3 through 18 of the OUI	RO	0013 hex
1. RO = Read Only				

Table 61. PHY Identification Register 2 (Address 3)

Bit	Name	Description	Type [1]	Default
3.15:10	PHY ID Number	The PHY identifier composed of bits 19 through 24 of the OUI	RO	011110
3.9:4	Manufacturer's Model Number	6 bits containing manufacturer's part number	RO	001111
3.3:1	Manufacturer's Revision Number	3 bits containing manufacturer's revision number	RO	XXX *(See Table 3 in Specification Update)*
3.0	Model Variant	0 = LXT9785 1 = LXT9785E	RO	X
1. RO = Read Only				

Figure 62. PHY Identifier Bit Mapping

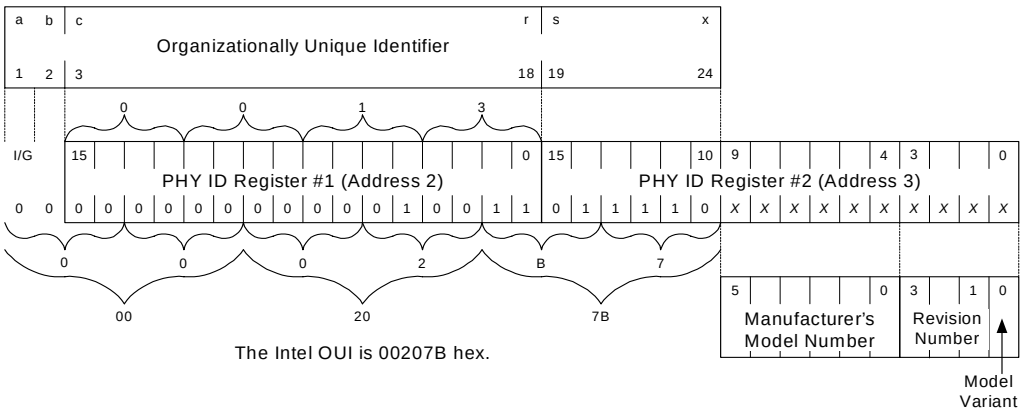


Table 62. Auto-Negotiation Advertisement Register (Address 4)[6]

Bit	Name	Description	Type [1]	Default
4.15	Next Page	1 = Port has ability to send multiple pages 0 = Port has no ability to send multiple pages	R/W	0
4.14	Reserved	Ignore on read	RO	0
4.13	Remote Fault	1 = Remote fault 0 = No remote fault	R/W	0
4.12	Reserved	Ignore	R/W	0
4.11	Asymmetric Pause	Pause operation defined in Clause 40 and 27	R/W	0
4.10	Pause[5]	1 = Pause operation enabled for full-duplex links 0 = Pause operation disabled	R/W	LSHR[2,3]
4.9	100BASE-T4	1 = 100BASE-T4 capability is available 0 = 100BASE-T4 capability is not available (The LXT9785/9785E does not support 100BASE-T4 but allows this bit to be set to advertise in the Auto-Negotiation sequence for 100BASE-T4 operation. An external 100BASE-T4 transceiver could be switched in if this capability is desired.)	R/W	0
4.8	100BASE-TX full duplex	1 = Port is 100BASE-TX full duplex capable 0 = Port is not 100BASE-TX full duplex capable.	R/W	LSHR[2,4]
4.7	100BASE-TX	1 = Port is 100BASE-TX capable 0 = Port is not 100BASE-TX capable	R/W	LSHR[2,4]
4.6	10BASE-T full duplex	1 = Port is 10BASE-T full duplex capable 0 = Port is not 10BASE-T full duplex capable	R/W	LSHR[2,4]
4.5	10BASE-T	1 = Port is 10BASE-T capable 0 = Port is not 10BASE-T capable	R/W	LSHR[243]
4.4:0	Selector Field, S<4:0>	<00001> = IEEE 802.3 <00010> = IEEE 802.9 ISLAN-16T <00000> = Reserved for future Auto-Negotiation development <11111> = Reserved for future Auto-Negotiation development Unspecified or reserved combinations should not be transmitted	R/W	00001

1. R/W = Read/Write, RO = Read Only
2. LSHR = Default value is derived from a single device input pin state or a group of device input pin states as the pin(s) are latched at startup or hardware reset.
3. The default setting of Register bit 4.10 is determined by the PAUSE pin.
4. Default settings for Register bits 4.5:8 are determined by CFG pins as described in Table 18 on page 62.
5. Pause operation is only valid for full-duplex modes.
6. Restart Auto-Negotiation process whenever Register 4 is written/modified.

Table 63. Auto-Negotiation Link Partner Base Page Ability Register (Address 5)

Bit	Name	Description	Type [1]	Default
5.15	Next Page	1 = Link Partner has ability to send multiple pages 0 = Link Partner has no ability to send multiple pages	RO	0
5.14	Acknowledge	1 = Link Partner has received Link Code Word from the LXT9785/9785E. 0 = Link Partner has not received Link Code Word from the the LXT9785/9785E	RO	0
5.13	Remote Fault	1 = Remote fault 0 = No remote fault	RO	0
5.12	Reserved	Ignore on read	RO	0
5.11	Asymmetric Pause	Pause operation defined in Clause 40 and 27 1 = Link Partner is Pause capable 0 = Link Partner is not Pause capable	RO	0
5.10	Pause	1 = Link Partner is Pause capable 0 = Link Partner is not Pause capable	RO	0
5.9	100BASE-T4	1 = Link Partner is 100BASE-T4 capable 0 = Link Partner is not 100BASE-T4 capable	RO	0
5.8	100BASE-TX full duplex	1 = Link Partner is 100BASE-TX full duplex capable 0 = Link Partner is not 100BASE-TX full duplex capable	RO	0
5.7	100BASE-TX	1 = Link Partner is 100BASE-TX capable 0 = Link Partner is not 100BASE-TX capable	RO	0
5.6	10BASE-T full duplex	1 = Link Partner is 10BASE-T full duplex capable 0 = Link Partner is not 10BASE-T full duplex capable	RO	0
5.5	10BASE-T	1 = Link Partner is 10BASE-T capable 0 = Link Partner is not 10BASE-T capable	RO	0
5.4:0	Selector Field S<4:0>	<00001> = IEEE 802.3 <00010> = IEEE 802.9 ISLAN-16T <00000> = Reserved for future Auto-Negotiation development <11111> = Reserved for future Auto-Negotiation development Unspecified or reserved combinations shall not be transmitted	RO	00000

1. RO = Read Only

Table 64. Auto-Negotiation Expansion (Address 6)

Bit	Name	Description	Type [1]	Default
6.15:6	Reserved	Ignore on read	RO	0
6.5	Base Page	This bit indicates the status of the Auto-Negotiation variable, base page. It flags synchronization with the Auto-Negotiation state diagram allowing detection of interrupted links. This bit is only used if Register bit 16.1 (Alternate NP feature) is set. 1 = base_page = true 0 = base_page = false	RO/ LH	0
6.4	Parallel Detection Fault	1 = Parallel detection fault has occurred. 0 = Parallel detection fault has not occurred.	RO/ LH	0
6.3	Link Partner Next Page Able	1 = Link partner is next page able 0 = Link partner is not next page able	RO	0
6.2	Next Page Able	1 = Local device is next page able 0 = Local device is not next page able	RO	1
6.1	Page Received	Indicates that a new page has been received and the received code word has been loaded into Register 5 or Register 8 as specified in clause 28 of 802.3. 1 = Three identical and consecutive link code words have been received from link partner 0 = Three identical and consecutive link code words have not been received from link partner	RO LH	0
6.0	Link Partner A/ N Able	1 = Link partner is auto-negotiation able 0 = Link partner is not auto-negotiation able	RO	0

1. RO = Read Only, LH = Latching High cleared when read

Table 65. Auto-Negotiation Next Page Transmit Register (Address 7)

Bit	Name	Description	Type [1]	Default
7.15	Next Page (NP)	1 = Additional next pages follow 0 = Last page	R/W	0
7.14	Reserved	Write as 0, ignore on read	RO	0
7.13	Message Page (MP)	1 = Message page 0 = Unformatted page	R/W	1
7.12	Acknowledge 2 (ACK2)	1 = Complies with message 0 = Cannot comply with message	R/W	0
7.11	Toggle (T)	1 = Previous value of the transmitted Link Code Word equalled logic zero 0 = Previous value of the transmitted Link Code Word equalled logic one	R/W	0
7.10:0	Message/ Unformatted Code Field	MP = 1: Code interpreted as “message page” MP = 0: Code interpreted as “unformatted page”	R/W	00000000001

1. R/W = Read Write, RO = Read Only

Table 66. Auto-Negotiation Link Partner Next Page Receive Register (Address 8)

Bit	Name	Description	Type [1]	Default
8.15	Next Page (NP)	1 = Link Partner has additional next pages to send 0 = Link Partner has no additional next pages to send	RO	0
8.14	Acknowledge (ACK)	1 = Link Partner has received Link Code Word from the LXT9785/9785E 0 = Link Partner has not received Link Code Word from the LXT9785/9785E	RO	0
8.13	Message Page (MP)	1 = Page sent by the Link Partner is a Message Page 0 = Page sent by the Link Partner is an Unformatted Page	RO	0
8.12	Acknowledge 2 (ACK2)	1 = Link Partner complies with the message 0 = Link Partner cannot comply with the message	RO	0
8.11	Toggle (T)	1 = Previous value of the transmitted Link Code Word equalled logic zero 0 = Previous value of the transmitted Link Code Word equalled logic one	RO	0
8.10:0	Message/ Unformatted Code Field	MP = 1: Code interpreted as “message page” MP = 0: Code interpreted as “unformatted page”	RO	00000000000

1. RO = Read Only

Table 67. Port Configuration Register (Address 16, Hex 10)

Bit	Name	Description	Type [1]	Default
16.15	Reserved	Write as 0, ignore on read	R/W	0
16.14	Link Disable	1 = Force Link pass. Sets appropriate registers and LEDs to Pass. 0 = Normal operation	R/W	0
16.13	Transmit Disable	1 = Disable Twisted-Pair transmitter 0 = Normal Operation	R/W	0
16.12	Bypass Scramble (100BASE-TX)	1 = Bypass Scrambler and Descrambler 0 = Normal Operation	R/W	0
16.11	Bypass 4B5B (100BASE-TX)	1 = Bypass 4B5B encoder and decoder 0 = Normal Operation	R/W	0
16.10	Jabber (10BASE-T)	1 = Disable Jabber 0 = Normal operation	R/W	0
16.9	SQE (10BASE-T)	This bit is ignored by the LXT9785/9785E 1 = Enable Heart Beat 0 = Disable Heart Beat	R/W	0
16.8	TP Loopback (10BASE-T)	1 = Disable TP loopback during half duplex operation 0 = Normal Operation	R/W	1
16.7	Reserved	Write as one. Ignore on read.	R/W	1
16.6	Reserved	Write as zero. Ignore on read.	R/W	0
16.5	PRE_EN	Preamble Enable. Preamble enable function is applicable to 10BASE-T only. 0 = Set RX_DV high coincident with SFD 1 = Set RX_DV high and RxData = preamble when CRS is asserted.	R/W	0
16.4	Reserved	Write as zero. Ignore on read.	R/W	0
16.3	Reserved	Write as zero. Ignore on read.	R/W	0
16.2	Far End Fault Transmission Enable	1 = Enable Far End Fault Transmission 0 = Disable Far End Fault Transmission	R/W	1
16.1	Reserved	Write as zero. Ignore on read.	R/W	0
16.0	Fiber Select	1 = Select fiber mode for this port 0 = Select TP mode for this port	R/W	LSHR[2,3]

1. R/W = Read/Write
2. LSHR = Default value is derived from a single device input pin state or a group of device input pin states as the pin(s) are latched at startup or hardware reset.
3. The default value of Register bit 16.0 is determined by the G_FX/TP pin. ___ If G_FX/TP is tied Low, the default value of Register bit 16.0 = 0. If G_FX/TP is not tied Low, the default value of Register bit 16.0 = 1.

Table 68. Quick Status Register (Address 17, Hex 11)

Bit	Name	Description	Type [1]	Default
17.15	Reserved	Always 0	RO	0
17.14	10/100 Mode	1 = The LXT9785/9785E is operating in 100BASE-TX mode. 0 = The LXT9785/9785E is not operating 100BASE-TX mode.	RO	0
17.13	Transmit Status	1 = The LXT9785/9785E is transmitting a packet 0 = The LXT9785/9785E is not transmitting a packet	RO LH	0
17.12	Receive Status	1 = The LXT9785/9785E is receiving a packet 0 = The LXT9785/9785E is not receiving a packet	RO LH	0
17.11	Collision Status	1 = Collision is occurring 0 = No collision	RO LH	0
17.10	Link	1 = Link is up 0 = Link is down	RO	0
17.9	Duplex Mode	1 = Full duplex 0 = Half duplex	RO	0
17.8	Auto-Negotiation	1 = The LXT9785/9785E is in Auto-Negotiation Mode 0 = The LXT9785/9785E is in manual mode	RO	0
17.7	Auto-Negotiation Complete	1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed This bit is only valid when auto-negotiate is enabled, and is equivalent to Register bit 1.5.	RO	0
17.6	FIFO Error	1 = FIFO error has occurred (Overflow or Underflow) 0 = No FIFO error has occurred	RO LH	0
17.5	Polarity	1 = Polarity is reversed 0 = Polarity is not reversed	RO	0
17.4	Pause	1 = The LXT9785/9785E is Pause capable 0 = The LXT9785/9785E is Not Pause capable	RO	0
17.3	Error	1 = Error Occurred (Remote Fault, RxERCntFUL, FIFO error, Jabber, Parallel Detect Fault) 0 = No error occurred	RO LH	0
17.2	Reserved	Reserved	RO	0
17.1	Reserved	Ignore	RO	0
17.0	Reserved	Always 0	RO	0

1. RO = Read Only, LH = Latching High cleared when read.

Table 69. Interrupt Enable Register (Address 18, Hex 12)

Bit	Name	Description	Type [1]	Default
18.15:9	Reserved	Write as 0, ignore on read	R/W	0
18.8	CNTRMSK	Mask for Counter Full 1 = Enable event to cause interrupt 0 = Do not allow event to cause interrupt	R/W	0
18.7	ANMSK	Mask for Auto-Negotiate Complete 1 = Enable event to cause interrupt 0 = Do not allow event to cause interrupt	R/W	0
18.6	SPEEDMSK	Mask for Speed Interrupt 1 = Enable event to cause interrupt 0 = Do not allow event to cause interrupt	R/W	0
18.5	DUPLEXMSK	Mask for Duplex Interrupt 1 = Enable event to cause interrupt 0 = Do not allow event to cause interrupt	R/W	0
18.4	LINKMSK	Mask for Link Status Interrupt 1 = Enable event to cause interrupt 0 = Do not allow event to cause interrupt	R/W	0
18.3	ISOLMSK	Mask for Isolate Interrupt 1 = Enable event to cause interrupt 0 = Do not allow event to cause interrupt	R/W	0
18.2	Reserved	Write as 0, ignore on read	R/W	0
18.1	INTEN	1 = Enable interrupts on this port 0 = Disable interrupts on this port	R/W	0
18.0	TINT	1 = Test Force interrupt on $\overline{\text{MDINT}}$ 0 = Normal operation	R/W	0

1. R/W = Read/Write

Table 70. Interrupt Status Register (Address 19, Hex 13)

Bit	Name	Description	Type [1]	Default
19.15:9	Reserved	Ignore on read	RO	0
19.8	RxERCntFUL	RxER Counter Full Status 1 = One of the internal counters has reached its maximum value 0 = The internal counters have not reached maximum values	RO/SC	0
19.7	ANDONE	Auto-Negotiation Status 1= Auto-Negotiation has completed 0= Auto-Negotiation has not completed	RO/SC	N/A
19.6	SPEEDCHG	Speed Change Status 1 = A Speed Change has occurred since last reading this register 0 = A Speed Change has not occurred since last reading this register	RO/SC	0
19.5	DUPLEXCHG	Duplex Change Status 1 = A Duplex Change has occurred since last reading this register 0 = A Duplex Change has not occurred since last reading this register	RO/SC	0
19.4	LINKCHG	Link Status Change Status 1 = A Link Change has occurred since last reading this register 0 = A Link Change has not occurred since last reading this register	RO/SC	0
19.3	Isolate	MII Isolate Change Status 1 = An Isolate change has occurred since last reading this register 0 = An Isolate change has not occurred since last reading this register	RO/SC	0
19.2	$\overline{\text{MDINT}}$	1 = RMII/SMII/SS-SMII interrupt pending 0 = No RMII/SMII/SS-SMII interrupt pending	RO/SC	0
19.1	Reserved	Ignore on read	RO/SC	0
19.0	Reserved	Ignore on read	RO	0

1. R/W = Read/Write, RO = Read Only, SC = Self Clearing when read

Table 71. LED Configuration Register (Address 20, Hex 14)

Bit	Name	Description	Type [1]	Default
20.15:12	LED1 Programming bits	0000 = Display Speed Status (Continuous, Default) 0001 = Display Transmit Status (Stretched) 0010 = Display Receive Status (Stretched) 0011 = Display Collision Status (Stretched) 0100 = Display Link Status (Continuous) 0101 = Display Duplex Status (Continuous) 0110 = Display Isolate Status (Continuous) 0111 = Display Receive or Transmit Activity (Stretched) 1000 = Test mode- turn LED on (Continuous) 1001 = Test mode- turn LED off (Continuous) 1010 = Test mode- blink LED fast (Continuous) 1011 = Test mode- blink LED slow (Continuous) 1100 = Display Link and Receive Status combined [2] (Stretched)[3] 1101 = Display Link and Activity Status combined [2] (Stretched)[3] 1110 = Display Duplex and Collision Status combined [4] (Stretched)[3] 1111 = Display Link and RxER Status combined [2] (Blink)	R/W	0000
20.11:8	LED2 Programming bits	0000 = Display Speed Status 0001 = Display Transmit Status 0010 = Display Receive Status 0011 = Display Collision Status 0100 = Display Link Status 0101 = Display Duplex Status 0110 = Display Isolate Status 0111 = Display Receive or Transmit Activity 1000 = Test mode- turn LED on 1001 = Test mode- turn LED off 1010 = Test mode- blink LED fast 1011 = Test mode- blink LED slow 1100 = Display Link and Receive Status combined [2] (Stretched)[3] 1101 = Display Link and Activity Status combined [2] (Default)(Stretched)[3] 1110 = Display Duplex and Collision Status combined [4] (Stretched)[3] 1111 = Display Link and RxER Status combined [2] (Blink)	R/W	1101

1. R/W = Read/Write, RO = Read Only, LH = Latching High.
2. Link status is the primary LED driver. The LED is asserted (solid ON) when the link is up. The secondary LED driver (Receive, Activity, or Error) causes the LED to change state (blink).
3. Combined event LED settings are not affected by Pulse Stretch Register bit 20.1. These display settings are stretched regardless of the value of 20.1.
4. Duplex status is the primary LED driver. The LED is asserted (solid ON) when the link is full duplex. Collision status is the secondary LED driver. The LED changes state (blinks) when a collision occurs.

Table 71. LED Configuration Register (Address 20, Hex 14) (Continued)

Bit	Name	Description	Type [1]	Default
20.7:4	LED3 Programming bits	0000 = Display Speed Status 0001 = Display Transmit Status 0010 = Display Receive Status 0011 = Display Collision Status 0100 = Display Link Status 0101 = Display Duplex Status 0110 = Display Isolate Status 0111 = Display Receive or Transmit Activity 1000 = Test mode- turn LED on 1001 = Test mode- turn LED off 1010 = Test mode- blink LED fast 1011 = Test mode- blink LED slow 1100 = Display Link and Receive Status combined [2] (Stretched)[3] 1101 = Display Link and Activity Status combined [2] (Stretched)[3] 1110 = Display Duplex and Collision Status combined [4] (Default) (Blink)[3] 1111 = Display Link and RxER Status combined [2] (Blink)	R/W	1110
20.3:2	LEDFREQ	00 = Stretch LED events to 30 ms 01 = Stretch LED events to 60 ms 10 = Stretch LED events to 100 ms 11 = Reserved	R/W	00
20.1	PULSE-STRETCH	1 = Enable pulse stretching of all LEDs 0 = Disable pulse stretching of all LEDs [2]	R/W	1
20.0	Reserved	Reserved	R/W	0

1. R/W = Read/Write, RO = Read Only, LH = Latching High.
2. Link status is the primary LED driver. The LED is asserted (solid ON) when the link is up. The secondary LED driver (Receive, Activity, or Error) causes the LED to change state (blink).
3. Combined event LED settings are not affected by Pulse Stretch Register bit 20.1. These display settings are stretched regardless of the value of 20.1.
4. Duplex status is the primary LED driver. The LED is asserted (solid ON) when the link is full duplex. Collision status is the secondary LED driver. The LED changes state (blinks) when a collision occurs.

Table 72. Receive Error Count Register (Address 21)

Bit	Name	Description	Type [1]	Default
21.15:0	Receive Error Count	A 16-bit counter value indicating the number of times a receive packet with errors occurred. Only one event gets counted per packet. When maximum count is reached, the 16-bit counter remains full until cleared. Refer to the discussion of “Out-of-Band Signalling” on page 74 for details.	RO/ SC	0

1. RO = Read Only
   S/C = Self Clearing when read

Table 73. RMII Out-of-Band Signalling Register (Address 25)

Bit	Name	Description	Type [1]	Default
25.15:7	Reserved	Reserved	R/W	0
25.6:4	BIT1	These three bits select which status information is available on the RxData(1) bit of the RMII bus. 000 = Link 001 = Speed 010 = Duplex 011 = Auto-negotiation complete 100 = Polarity reversed 101 = Jabber detected 110 = Interrupt pending 111 = Isolate	R/W	000
25.3:1	BIT0	These three bits select which status information is available on the RxData(0) bit of the RMII bus. 000 = Link 001 = Speed 010 = Duplex 011 = Auto-negotiation complete 100 = Polarity reversed 101 = Jabber detected 110 = Interrupt pending 111 = Isolate	R/W	000
25.0	PROGRMII	1 = Enable programmable RMII Out-of-Band signalling. When enabled, bits 6:1 specify which status bits are available on the RMII RxData data bus. 0 = Disable Out-of-Band signalling.	R/W	0

1. R/W = Read/Write
   RO = Read Only

Table 74. Trim Enable Register (Address 27)

27.15:12	Reserved	Write as 0, ignore on read	RO	0
27.11:10	Per-Port Rise Time Control	00 = 3.3ns 01 = 3.6ns 10 = 3.9ns 11 = 4.2ns	R/W	LSHR[1,2]
27.9	AMDIX_EN	0 = Disable auto MDIX 1 = Enable auto MDIX	R/W	LSHR[1,3]
27.8	MDIX	Manual MDI/MDIX selection: (This bit is ignored when Register bit 27.9 = 1) 0 = MDI, transmit on pair A and receive on pair B 1 = MDIX transmit on pair B and receive on pair A	R/W	LSHR[1,4]
27.7	Analog Loop back	1 = Enable analog loop back (transmits on twisted-pair) 0 = Disable analog loop back	R/W	0
27.6	Dis_EN	DTE Discovery Process Enable 1 = Enable DTE discovery process 0 = Disable DTE discovery process	R/W	0
27.5	Loop back Speed Up Enable	1 = enable automatic loop back detection speed up 0 = disable automatic loop back detection speed up	R/W	0
27.4	Power_EN	Power Enable (Requires Auto-Negotiation Enable Register bit 0.12 = 1) 1 = Potential Remote-Power DTE discovered; indication to turn on power over the cable. 0 = Remote-Power DTE not discovered; process may not be complete.	RO	0
27.3	SLP_Det	Standard Link Partner Detected 1 = Standard link partner discovered; indication not to turn on power over the cable. 0 = Standard link partner not discovered; process may not be complete.	R/W SC	0
27.2	LFIT Expired	Link Fail Inhibit Timer expiration indicator. Valid only when SLP_Det = 1. 1 = Link Fail Inhibit Timer expired with a standard link partner detected since last register read or link establishment 0 = Timer has not expired or standard link partner not discovered	R/W SC	0
27.1:0	Reserved	Write as 0, ignore on read	RO	0

1. LSHR = Default value is derived from a single device input pin state or a group of device input pin states as the pin(s) are latched at startup or hardware reset.
2. Default values for Register bits 27.11:10 are determined by the TxSLEW pins.
3. Default value for Register bit 27.9 is determined by the AMDIX_EN pin.
4. Default value for Register bit 27.8 is determined by the MDIX pin.
5. SC = Self Clearing when read; RO = Read Only; R/W = Read/Write.

Table 76. Register Bit Map

Reg Title	Bit Fields																Addr
	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	
Control Register (Address 0)																	
Control	Reset	Loopback	Speed Select	A/N Enable	Power Down	Isolate	Re-start A/N	Duplex Mode	COL Test	Speed Select	Reserved						0
Status Register (Address 1)																	
Status	100Base-T4	100Base-X Full Duplex	100Base-X Half Duplex	10 Mbps Full Duplex	10 Mbps Half Duplex	100Base-T2 Full Duplex	100Base-T2 Half Duplex	Extended Status	Reserved	MF Preamble Suppress	A/N Complete	Remote Fault	A/N Ability	Link Status	Jabber Detect	Extended Capability	1
PHY ID Registers (Address 2 and 3)																	
PHY ID 1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	2
PHY ID2	PHY ID No						MFR Model No						MFR Rev No			Model Variant	3
Auto-Negotiation Advertisement Register (Address 4)																	
A/N Advertise	Next Page	Reserved	Remote Fault	Reserved	Asymm Pause	Pause	100Base-T4	100Base-TX Full Duplex	100Base-TX	10Base-T Full Duplex	10Base-T	IEEE Selector Field					4
Auto-Negotiation Link Partner Base Page Ability Register (Address 5)																	
A/N Link Ability	Next Page	Ack	Remote Fault	Reserved	Asymm Pause	Pause	100Base-T4	100Base-TX Full Duplex	100Base-TX	10Base-T Full Duplex	10Base-T	IEEE Selector Field					5
Auto-Negotiation Expansion Register (Address 6)																	
A/N Expansion	Reserved										Base Page	Parallel Detect Fault	Link Partner Next Page Able	Next Page Able	Page Received	Link Partner A/N Able	6
Auto-Negotiation Next Page Transmit Register (Address 7)																	
A/N Next Page Txmit	Next Page	Reserved	Message Page	Ack 2	Toggle	Message / Unformatted Code Field											7
Auto-Negotiation Link Partner Next Page Ability Register (Address 8)																	
A/N Link Next Page	Next Page	Ack	Message Page	Ack 2	Toggle	Message / Unformatted Code Field											8

Table 76. Register Bit Map (Continued)

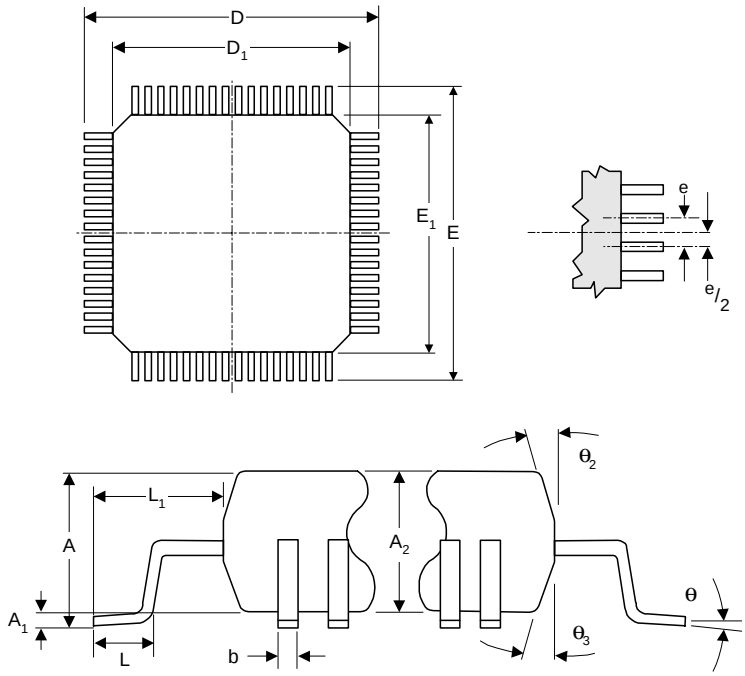
Reg Title	Bit Fields																Addr
	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	
Port Configuration Register (Address 16)																	
Port Config	Reserved	Link Disable	Txmit Disable	Bypass Scrambler (100BASE-TX)	Bypass 4B/5B (100BASE-TX)	Jabber (10BASE-T)	SQE (10BASE-T)	TP Loopback (10BASE-T)	Reserved	Reserved	PRE_EN	Reserved	Reserved	Far End Fault Enable	Reserved	Fiber Select	16
Quick Status Register (Address 17)																	
Quick Status	Reserved	10/100 Mode	Transmit Status	Receiver Status	Collision Status	Link	Duplex Mode	Auto-Neg	Auto-Neg Complete	FIFO Error	Polarity	Pause	Error	Reserved	Reserved	Reserved	17
Interrupt Enable Register (Address 18)																	
Interrupt Enable	Reserved							Counter Mask	Auto-Neg Mask	Speed Mask	Duplex Mask	Link Mask	Isolate Mask	Reserved	Interrupt Enable	Test Interrupt	18
Interrupt Status Register (Address 19)																	
Interrupt Status	Reserved							RxER Counter Full	Auto-Neg Done	Speed Change	Duplex Change	Link Change	Isolate Change	MD Interrupt	Reserved	Reserved	19
LED Configuration Register (Address 20)																	
LED Config	LED1				LED2				LED3				LED Freq		Pulse Stretch	Reserved	20
Receive Error Count Register (Address 21)																	
Rcv Error Count	Receive Error Count																21
False Carrier Counter Register (Address 22)																	
Reserved	Reserved																22
Programmable RMII Out-of-Band Signalling Register (Register 25)																	
RMII OOB Signalling	Reserved									Bit 1			Bit 0			Program RMII	25
Trim Enable Register (Address 27)																	
Trim Enable	Reserved				Per Port Rise Time Control		AMDIX_EN	MDIX	Analog Loop Back	Dis_EN	Loop Back Speed Up Enable	Power_EN	SLP_Det	LFIT Expired	Reserved		27

6.0 Package Specifications

Figure 63. LXT9785/9785E 208-Pin PQFP Plastic Package Specification

208-Pin Plastic Quad Flat Package

- Part Number LXT9785HC, LXT9785EHC
- Commercial Temperature Range (0°C to 70°C)



Dim	Millimeters	
	Min	Max
A	-	4.10
A1	0.25	-
A2	3.20	3.60
b	0.17	0.27
D	30.30	30.90
D_1	27.70	28.30
E	30.30	30.90
E_1	27.70	28.30
e	.50 BASIC	
L	0.50	0.75
L_1	1.30 REF	
q	0°	7°
θ_2	5°	16°
θ_3	5°	16°

Figure 64. LXT9785/9785E 241-Ball PBGA Package Specs - Top/Side View(LXT9785BC/ LXT9785EBC)

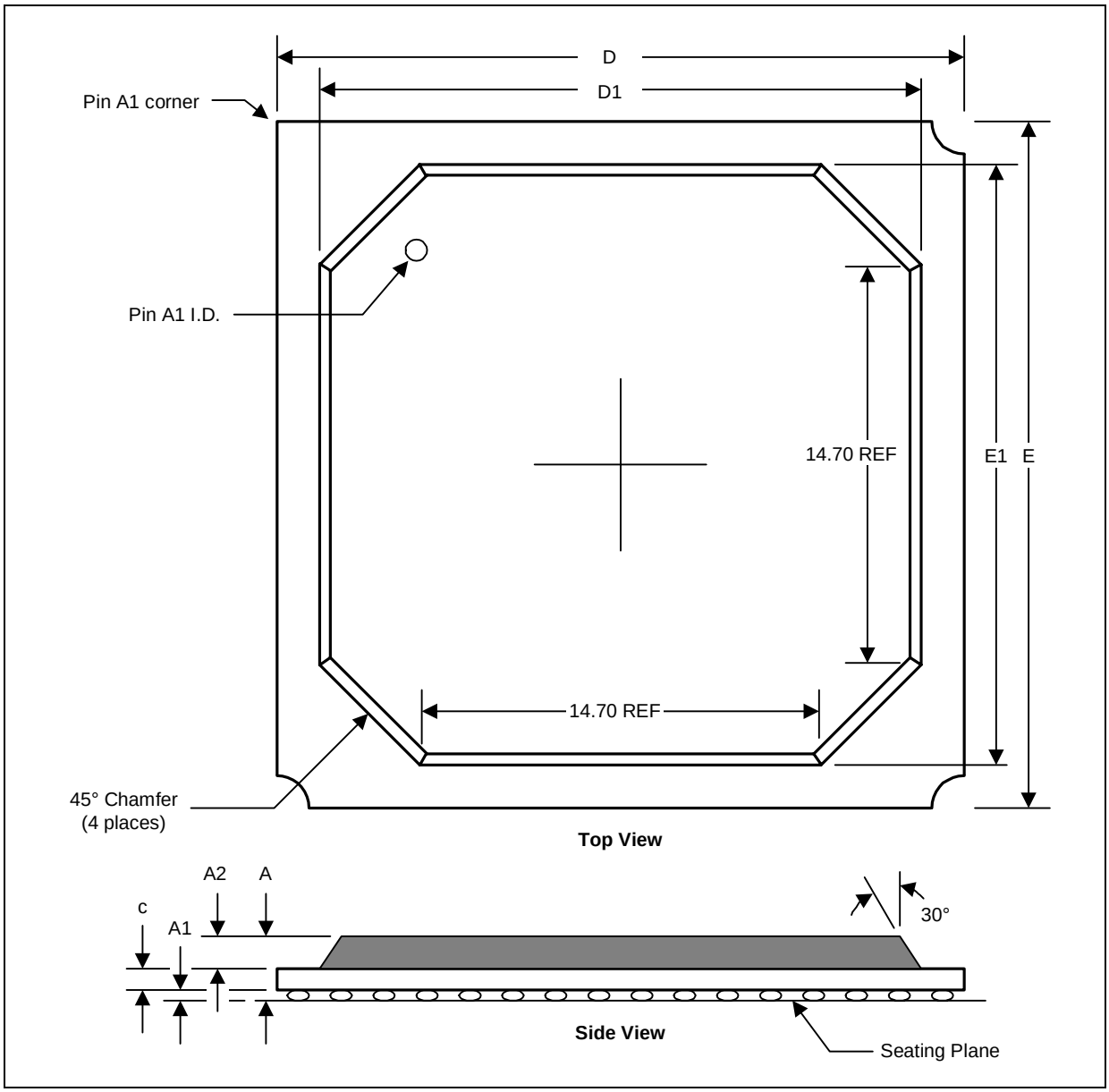


Figure 65. LXT9785/9785E 241-Ball PBGA Package Specs - Bottom View (LXT9785BC/ LXT9785EBC)

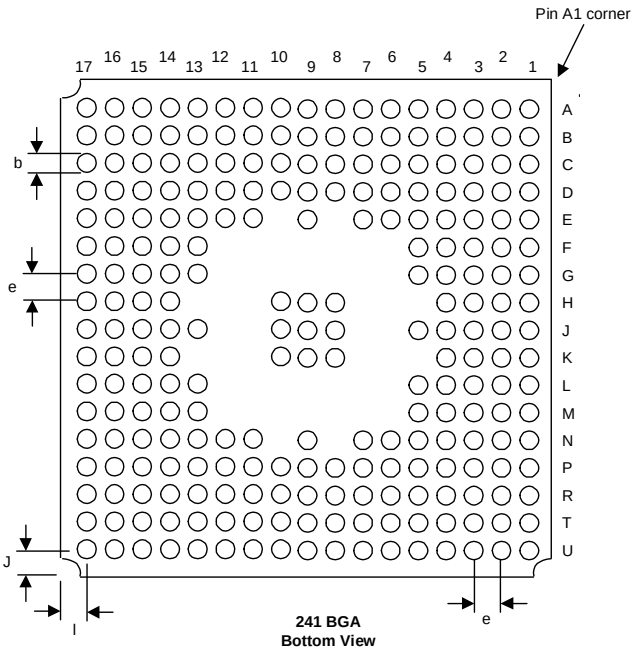


Table 77. LXT9785/9785E 241-Ball PBGA Package Dimensions

Symbol	Min	Nominal	Max	Units	Note
A	2.14	2.33	2.51	mm	
A1	0.50	0.60	0.70	mm	
A2	1.12	1.17	1.22	mm	
D	22.90	23.00	24.00	mm	
D1	19.30	10.50	19.70	mm	
E	22.90	23.00	24.00	mm	
E1	19.30	19.50	19.70	mm	
e	1.27 (solder ball pitch)			mm	
I	1.34 REF.			mm	
J	1.34 REF.			mm	
M	17 x 17 Matrix			mm	
b^2	0.60	0.75	0.90	mm	
c	0.52	0.56	0.60	mm	
e		1.27		mm	

1. All dimensions and tolerances conform to ANSI Y14.5-1982.
2. Dimension is measured at maximum solder ball diameter parallel to primary datum (-C-).
3. Primary datum (-C-) and seating plane are defined by the spherical crowns of the solder balls.