SONY

CXA1310AQ

Single Chip Processing for CCD Monochrome Camera

Description

The CXA1310AQ is designed to perform the basic signal processing in CCD monochrome cameras with a single chip. This bipolar IC is most suitable for compact usage and low power consumption.

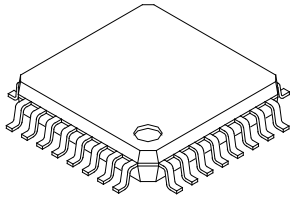
Features

- Processing from CCD output to 75Ω video output with a single chip
- Wide variable AGC (4 to 32dB Typ.)
- Built-in operational amplifier for AGC loop
- 75Ω line capacitance minimized using sag compensation function
- Variable white clip level realize wide dynamic range (140 IRE)

Application

CCD monochrome camera

32 pin QFP (Plastic)



Structure

Bipolar silicon monolithic IC

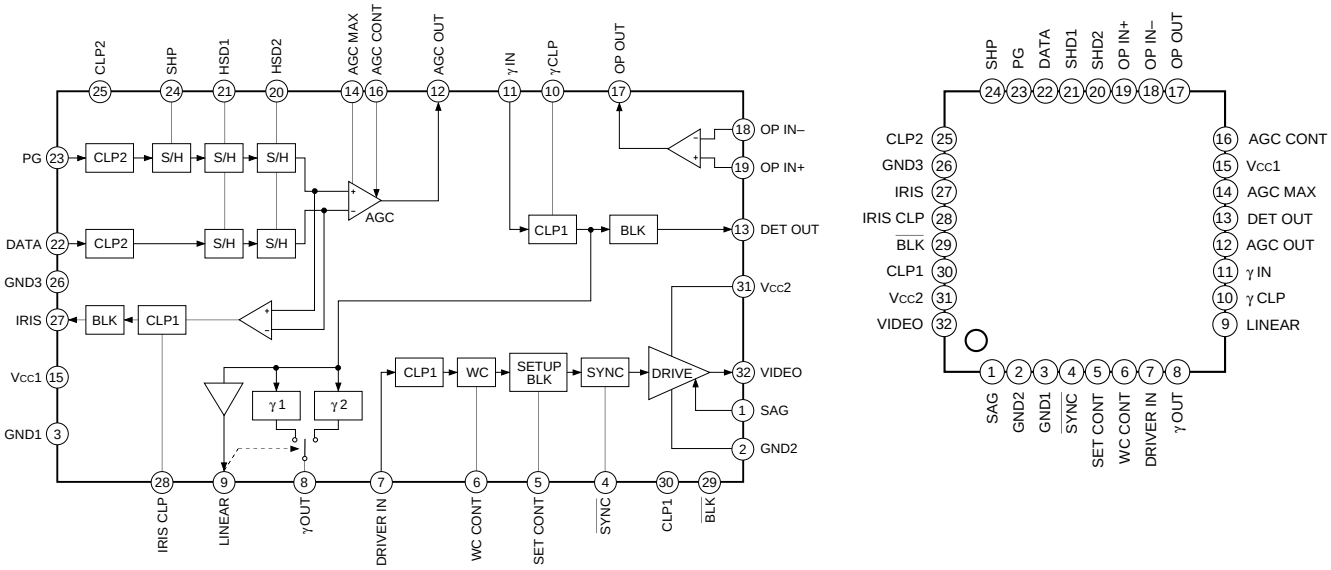
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	7	V
• Storage temperature	Tstg	–65 to +150	°C
• Operating temperature	Topr	–20 to +75	°C
• Allowable power dissipation	P_D	500	mW

Operating Conditions

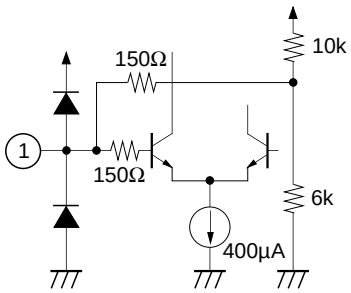
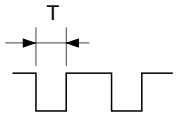
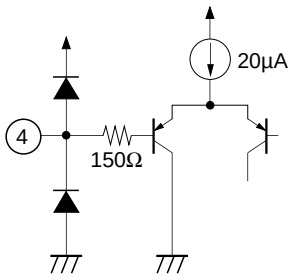
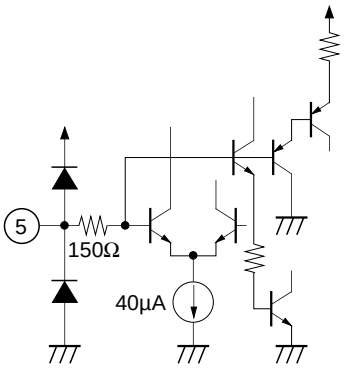
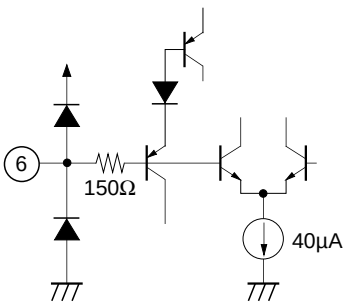
Supply voltage	V_{CC}	4.75 to 5.25	V

Block Diagram and Pin Configuration

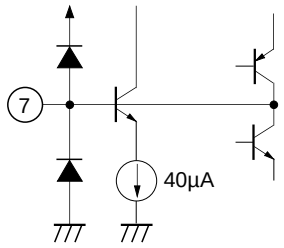
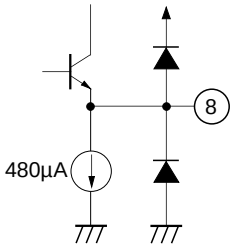
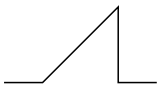
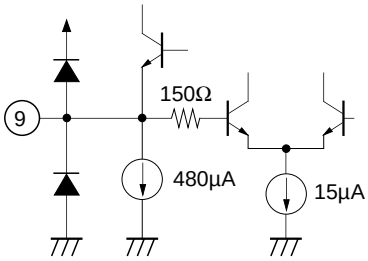
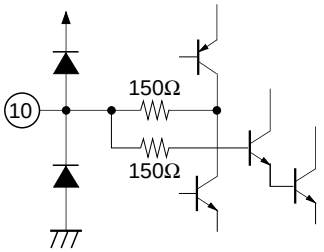
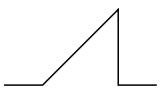
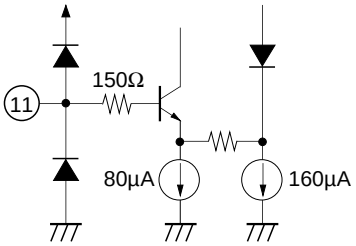


E89Z21A78-PS

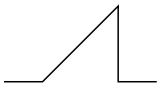
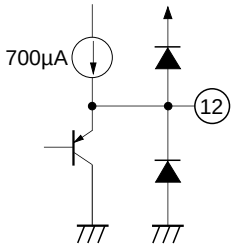
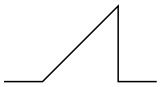
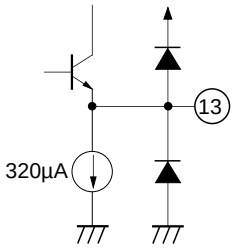
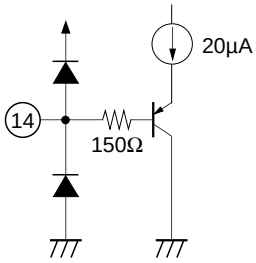
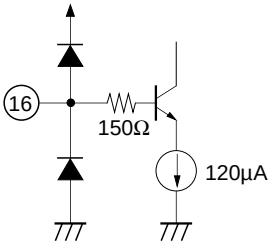
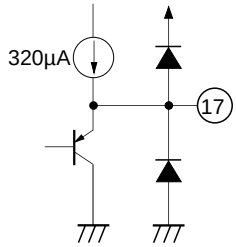
Pin Description

No.	Symbol	I/O signal	Equivalent circuit	Description
1	SAG	Inputs VIDEO OUT through capacitor		Input pin of sag compensation signal
2	GND2	GND*		GND for driver and IRIS
3	GND1	GND*		GND for other than driver, sample hold and IRIS
4	$\overline{\text{SYNC}}$	 High: 4.5V and above* Low: 0.5V and below T: 5µs		Sync pulse input pin (active at Low)
5	SET CONT			Set-up level adjusting pin
		GND*		Turns to preset mode 1
		2 to 3.5V*		Control mode
		V_{CC}*		Turns to preset mode 2
6	WC CONT			White clip level adjusting pin
		GND*		Preset mode
		2 to 3.5V*		Control mode

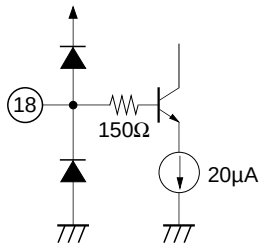
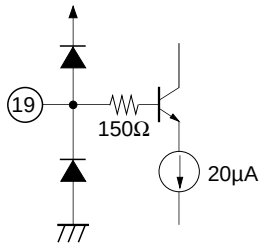
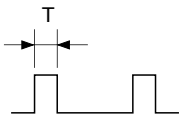
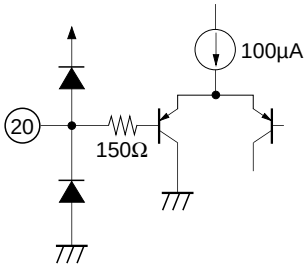
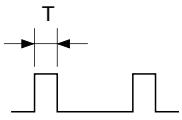
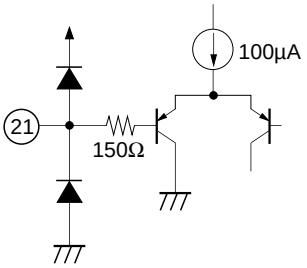
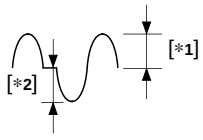
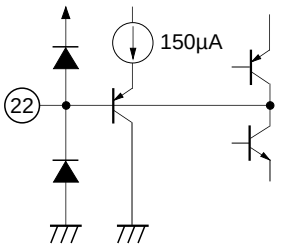
* External applied voltage

No.	Symbol	I/O signal	Equivalent circuit	Description
7	DRIVER IN	Input γ OUT through capacitor or LINEAR		Input pin to driver
8	γ OUT	 DC 2V		Gamma correction signal output pin. Outputs γ 1 when Pin 9 is at OPEN Outputs γ 2 when Pin 9 is turnedto 5V
9	LINEAR	 DC 1.8V		Linear signal (γ-OFF signal) output pin
		V_{CC}*		Pin 8 output signal turns to γ 2 output
10	γ CLP			Capacitor connecting pin for gamma input clamp
11	γ IN	 Input DC permissible range DC2 to 3V*		Input pin of the gamma correction circuit

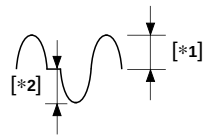
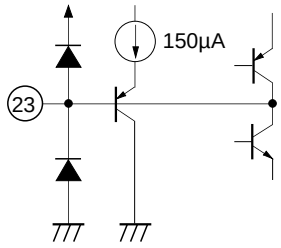
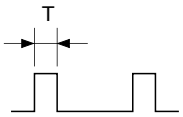
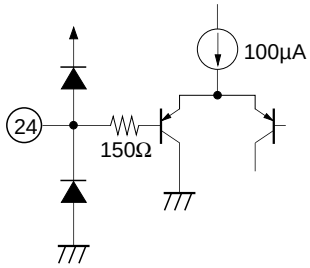
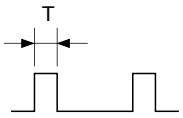
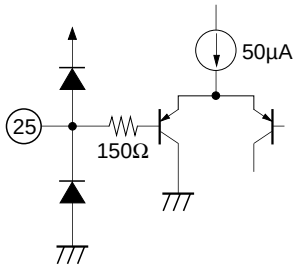
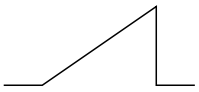
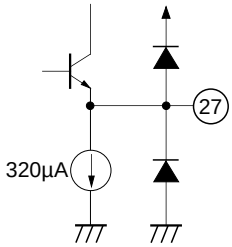
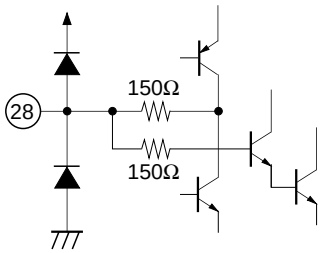
* External applied voltage

No.	Symbol	I/O signal	Equivalent circuit	Description
12	AGC OUT	 Vp-p MAX 1300mV Vp-p TYP 500mV DC 2.55V		Output pin of signal passed through AGC
13	DET OUT	 MAX 1500mV TYP 500mV DC 2V		Output pin of AGC detection signal
14	AGC MAX	DC*		Maximum gain setting pin of AGC amplifier
15	Vcc1	5V*		Power supply for other than driver and IRIS
16	AGC CONT	DC*		Gain control pin of AGC amplifier
17	OP OUT			Output pin of the operational amplifier

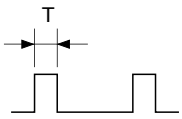
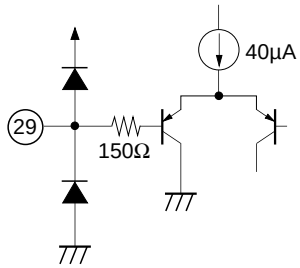
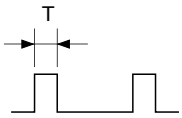
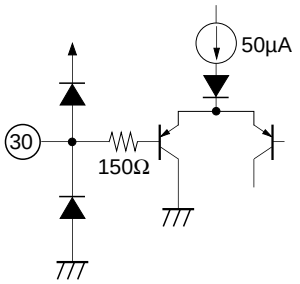
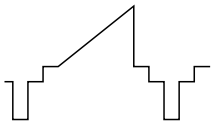
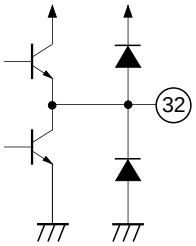
* External applied voltage

No.	Symbol	I/O signal	Equivalent circuit	Description
18	OP IN–			Inverted input pin of the operational amplifier
19	OP IN+			Non inverted input pin of the operational amplifier (AGC detection signal input pin)
20	SHD2	 High: 4.5V and above* Low: 0.5V and below T: 15ns and above		Input pin of the sample / hold pulse (active at High)
21	SHD1	 High: 4.5V and above* Low: 0.5V and below T: 15ns and above		Input pin of the sample / hold pulse (active at High)
22	DATA	 [*1] MAX 800mV [*2] MAX 800mV		CCD signal input pin

* External applied voltage

No.	Symbol	I/O signal	Equivalent circuit	Description
23	PG	 [*1] MAX 800mV [*2] MAX 800mV		CCD single input pin
24	SHP	 High: 4.5V and above* Low: 0.5V and below T: 15ns		Input pin of the sample / hold pulse (active at High)
25	CLP2	 High: 4.5V and above* Low: 0.5V and below T: 2µs		CLP2 pulse input pin (active at High)
26	GND3	GND*		Sample / hold GND
27	IRIS	 DC 1.3V		Output pin of the IRIS control signal
28	IRIS CLP			Capacitor connecting pin for IRIS output clamp

* External applied voltage

No.	Symbol	I/O signal	Equivalent circuit	Description
29	$\overline{BLK}$	 High: 4.5V and above* Low: 0.5V and below T: 11µs		BLK pulse input pin (active at Low)
30	CLP1	 High: 4.5V and above* Low: 0.5V and below T: 2µs		CLP1 pulse input pin (active at High)
31	$V_{CC}2$	5V*		Driver and IRIS power supply
32	VIDEO	 BLK level 1.5V		VIDEO signal output pin

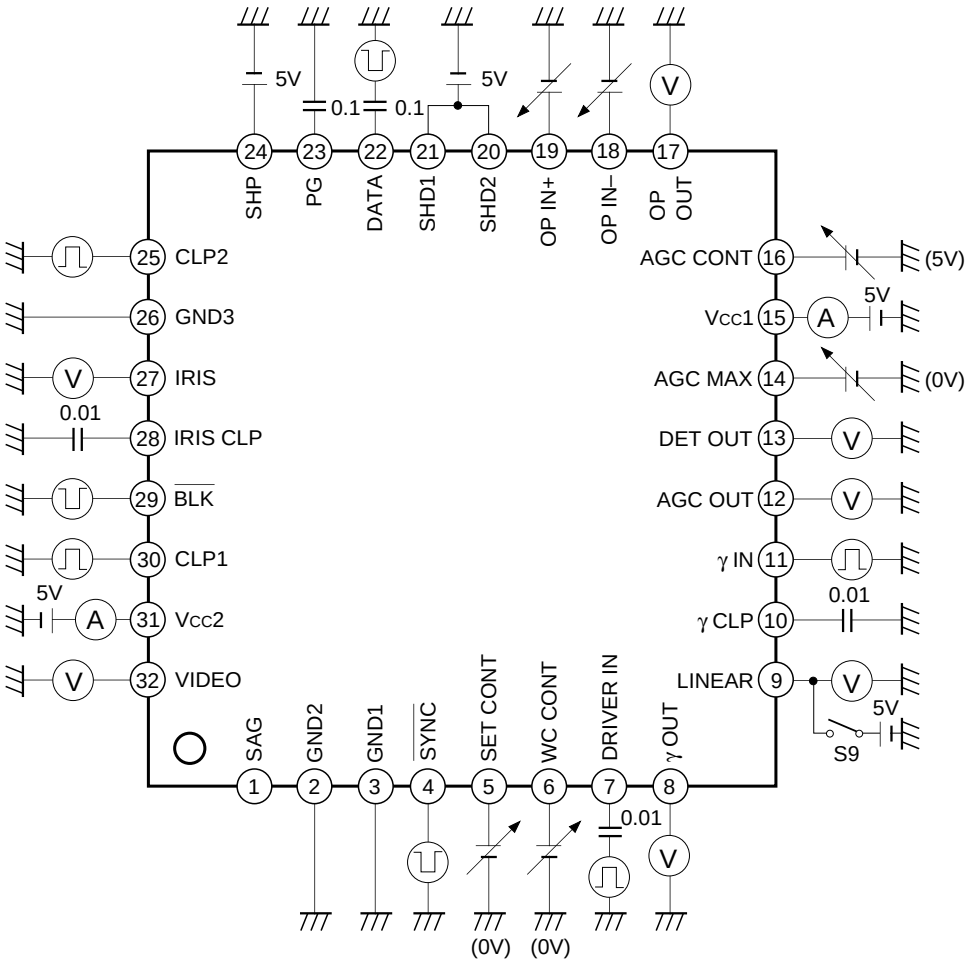
* External applied voltage

Electrical Characteristics (Ta = 25°C, Vcc = 5V, See Electrical Characteristics Test Circuit)

No.	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
1	Current consumption	Icc	Current value of Vcc1 and Vcc2 AGC CONT = 1.5V	30	45	60	mA
2	Min. value of AGC MAX	MAX	GAIN between DATA input and AGC OUT DATA input = 100mV AGC MAX = 4V, AGC CONT = 1.5V	—	18	20	dB
3	Min. value of AGC CONT	AG1	GAIN between DATA input and AGC OUT DATA input = 500mV, AGC CONT = 5V	—	4	6	dB
4	Max. value of AGC CONT	AG2	GAIN between DATA input and AGC OUT DATA input = 30mV, AGC CONT = 1.5V	30	32	—	dB
5	AGC CONT 10dB	AG3	GAIN between DATA input and AGC OUT DATA input = 320mV, AGC CONT = 3.55V	8	10	12	dB
6	AGC OUT DC	ADC	DC output level of AGC OUT	2.25	2.55	2.85	V
7	γ 1 output level	γ 1	Test value of γ 1 output level γ IN input = 500mV	530	630	730	mV
8	γ 2 output level	γ 2	Test value of γ 2 output level γ IN input = 500mV, S9 ON	580	680	780	mV
9	LINEAR AMP GAIN	LG	GAIN between γ IN input and LINEAR γ IN input = 500mV	1.6	2.6	3.6	dB
10	DET OUT DC	DDC	DC output level of DET OUT	1.8	2.0	2.2	V
11	IRIS AMP GAIN	IG	GAIN between DATA input and IRIS DATA input = 300mV	8	10	12	dB
12	IRIS OUT DC	IDC	DC output level of IRIS	1.1	1.3	1.5	V
13	DRIVER GAIN	DG	GAIN between DRIVER IN and VIDEO DRIVER IN = 700mV	5.7	6.0	6.3	dB
14	SYNC level	SY	SYNC level/DG* of VIDEO output	270	293	316	mV
15	SETUP 1	SE1	SETUP level of preset mode 1 SETUP level/DG* of VIDEO output	–15	0	15	mV
16	SETUP 2	SE2	SETUP level of preset mode 2 SETUP level/DG* of VIDEO output	0	20	40	mV
17	Min. value of SET CONT	SE3	SETUP level/DG* of VIDEO output SET CONT = 2V	—	–3	15	mV
18	Max. value of SET CONT	SE4	SETUP level/DG* of VIDEO output SET CONT = 3.3V	80	130	—	mV
19	W-CLIP level	WC1	W-CLIP level /DG* of VIDEO output DRIVER IN = 1500mV, WC CONT = GND	780	820	860	mV
20	Min. value of WC CONT	WC2	W-CLIP level /DG* of VIDEO output DRIVER IN = 1500mV, WC CONT = 2.2V	—	300	600	mV
21	Max. value of WC CONT	WC3	W-CLIP level /DG* of VIDEO output DRIVER IN = 1500mV, WC CONT = 3.3V	1000	1300	—	mV
22	OP AMP output D range Low level	OPL	DC output level of OP OUT OP IN+ = 2.5V, OP IN– = 4V	—	0.8	1.2	V
23	OP AMP output D range High level	OPH	DC output level of OP OUT OP IN+ = 4V, OP IN– = 2.5V	4.5	4.8	—	V

* Characteristics value at DRIVER GAIN item

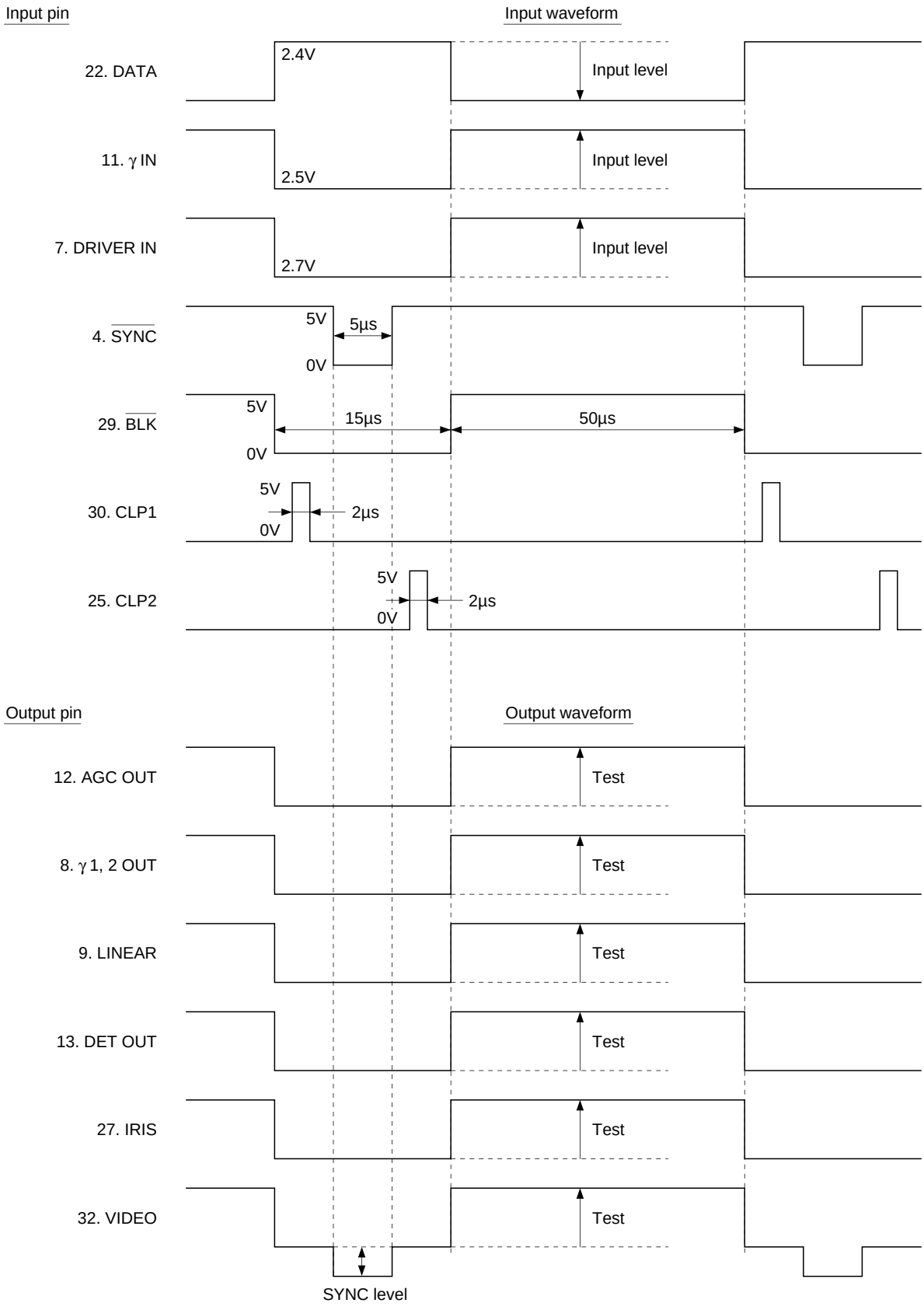
Electrical Characteristics Test Circuit



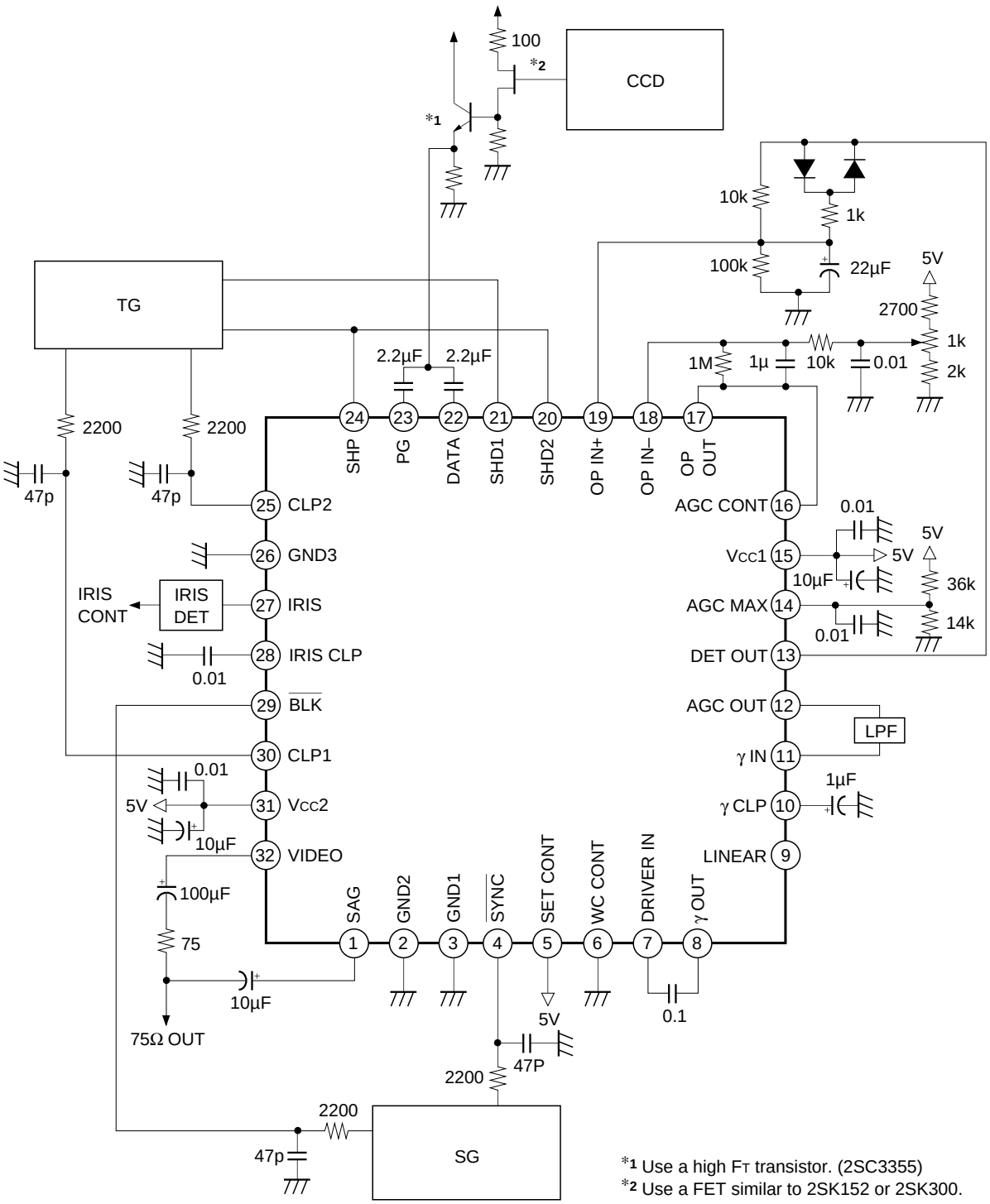
Notes)

1. µF is the capacitance unit of the capacitor.
2. For Pins 5, 6, 14 and 16, apply voltage in brackets unless otherwise specified in the conditions column of the Electrical Characteristics.
3. Ⓥ indicates a test pin. (Test AC, DC voltage)
4. For Pins 7, 11 and 22, the input signal level is at 0mV, unless otherwise specified in the conditions column of the Electrical Characteristics.

Test Circuit I/O Waveform Diagram



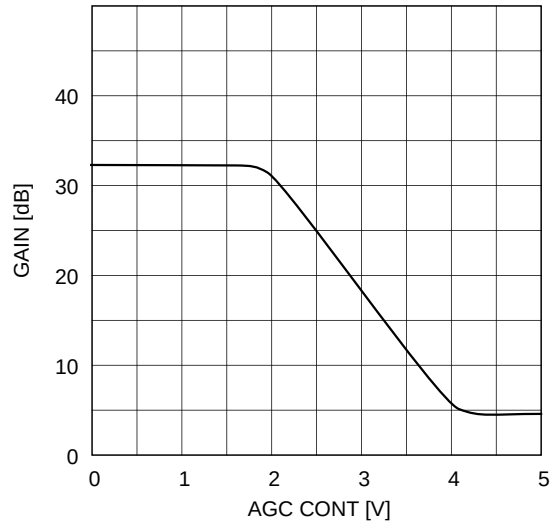
Application Circuit



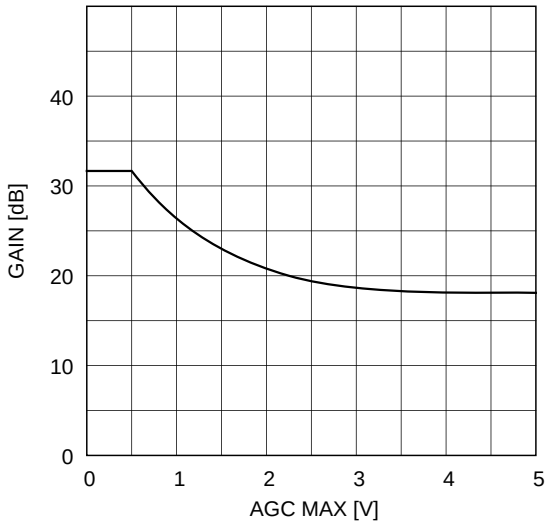
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics (Vcc = 5V, Ta = 25°C)

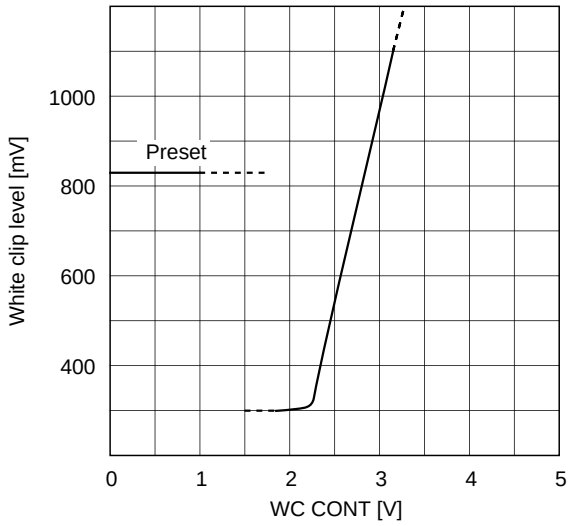
AGC control characteristics



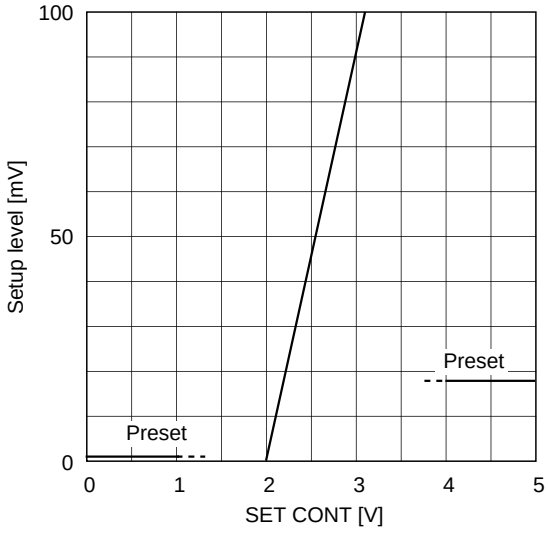
AGC MAX control characteristics



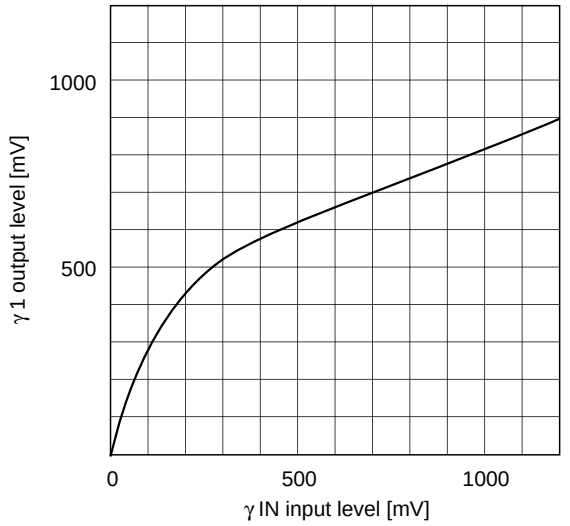
White clip control characteristics



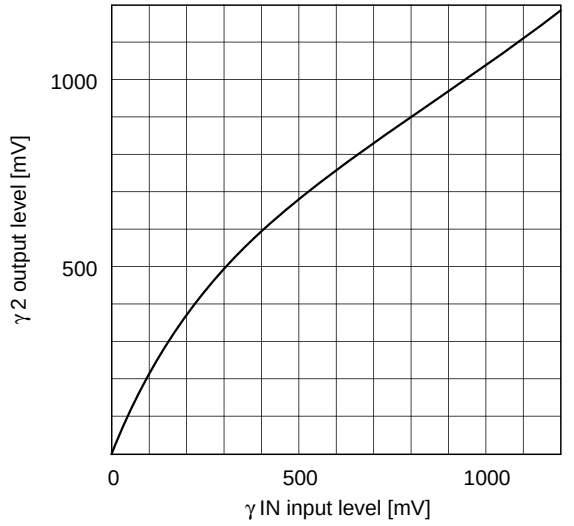
Setup control characteristics



γ 1 I/O characteristics

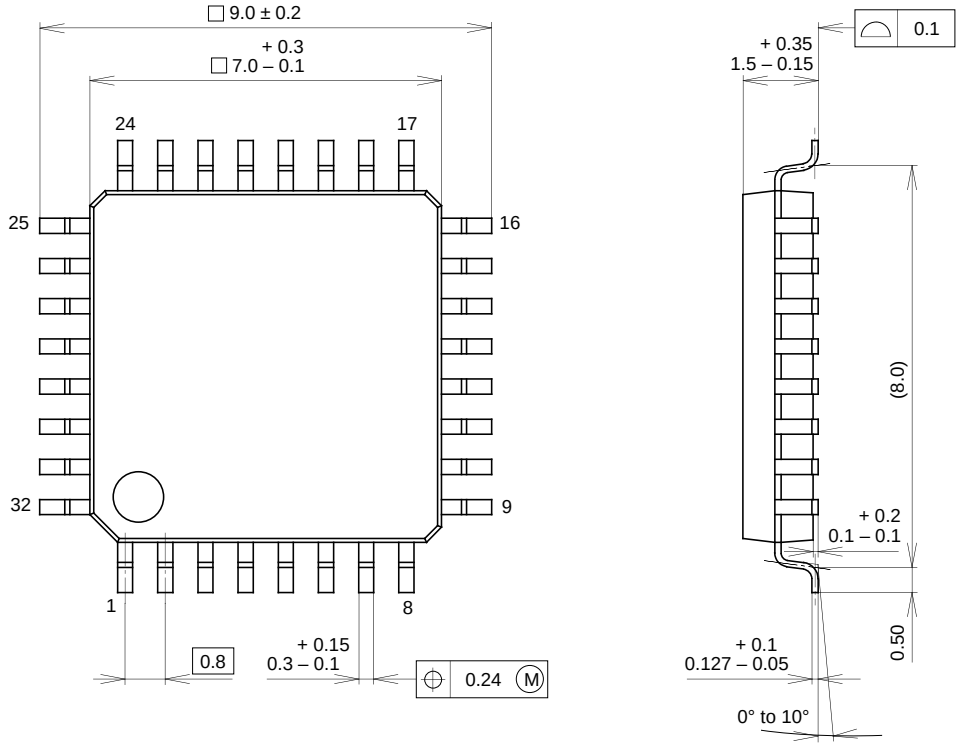


γ 2 I/O characteristics



Package Outline Unit: mm

32PIN QFP (PLASTIC)



SONY CODE	QFP-32P-L01
EIAJ CODE	QFP032-P-0707
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.2g