MCM6287

64K x 1 Bit Static Random Access Memory

P PACKAGE
PLASTIC
CASE 736A

J PACKAGE
300 MIL SOJ
CASE 810A

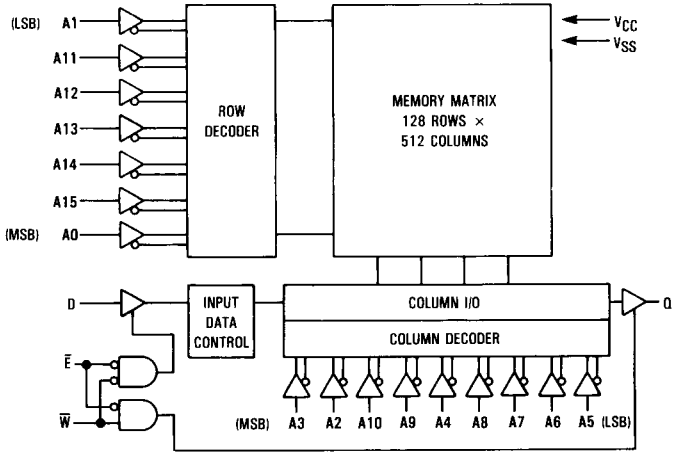
The MCM6287 is a 65,536 bit static random access memory organized as 65,536 words of 1 bit, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This device also incorporates internal power down circuitry that will reduce active current for less than 100% duty cycle applications. These features provide reduced system power requirements without degrading access time performance.

The MCM6287 is available in a 300 mil, 22 lead plastic DIP and a 24 lead, 300 mil, surface-mount SOJ package. Both feature JEDEC standard pinout.

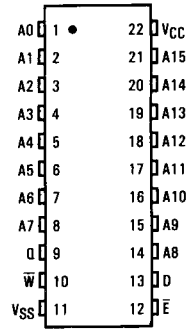
- Single 5 V ±10% Power Supply
- Fast Access Time: 25/35 ns
- Equal Address and Chip Enable Access Time
- Low Power Operation: 120/110 mA Maximum, Active AC
- High Board Density SOJ Available
- Three State Data Output
- Fully TTL Compatible

BLOCK DIAGRAM

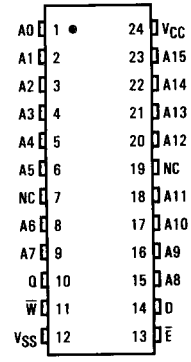


PIN ASSIGNMENT

DUAL-IN-LINE



SMALL OUTLINE



PIN NAMES	
A0-A15	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No Connection

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TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	ISB1, ISB2	High-Z	–
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature — Plastic Ceramic	T_{stg}	−55 to +125 −65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	–	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	–	±1.0	μA
AC Supply Current (I_{out} = 0 mA) MCM6287-25: t_{AVAV} = 25 ns	I_{CCA}	–	120	mA
AC Supply Current (I_{out} = 0 mA) MCM6287-35: t_{AVAV} = 35 ns	I_{CCA}	–	110	
TTL Standby Current ($\overline{E}$ = V_{IH}, No Restrictions on Other Inputs)	I_{SB1}	–	20	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} −0.2 V, No Restrictions on Other Inputs)	I_{SB2}	–	15	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	–	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)	V_{OH}	2.4	–	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance All Inputs Except $\overline{E}$	C_{in}	4	6	pF
Input Capacitance $\overline{E}$		5	7	
Output Capacitance	C_{out}	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

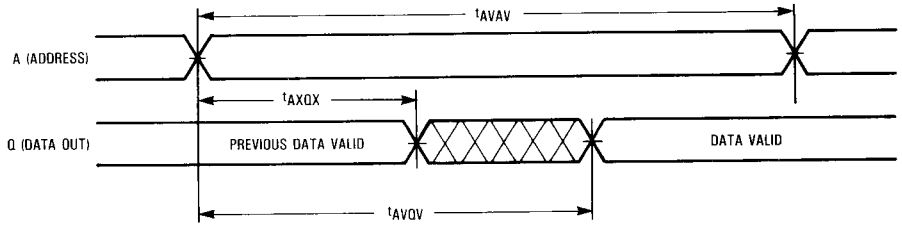
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

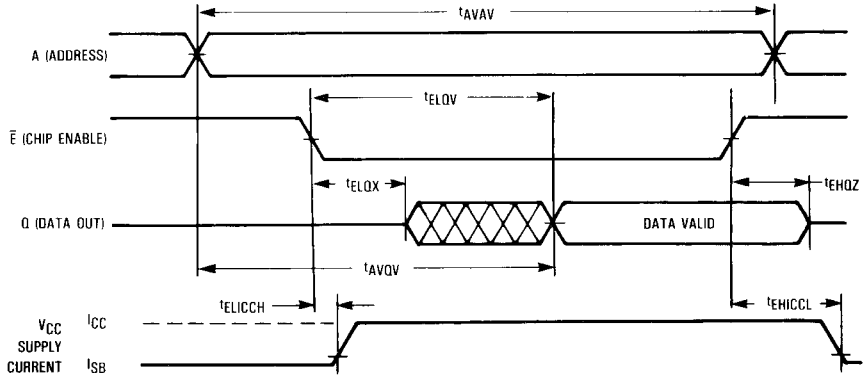
Parameter	Symbol		MCM6287-25		MCM6287-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	25	–	35	–	ns	2
Address Access Time	t_{AVQV}	t_{AA}	–	25	–	35	ns*	
Enable Access Time	t_{ELQV}	t_{ACS}	–	25	–	35	ns	3
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	5	–	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	5	–	5	–	ns	4,5,6
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	15	0	15	ns	4,5,6
Power Up Time	t_{ELICCH}	t_{PU}	0	–	0	–	ns	
Power Down Time	t_{EHICCL}	t_{PD}	–	25	–	30	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max, is less than t_{ELQX} min, both for a given device and from device to device.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E} = V_{IL}$).

READ CYCLE 1 (See Note 7 Above)



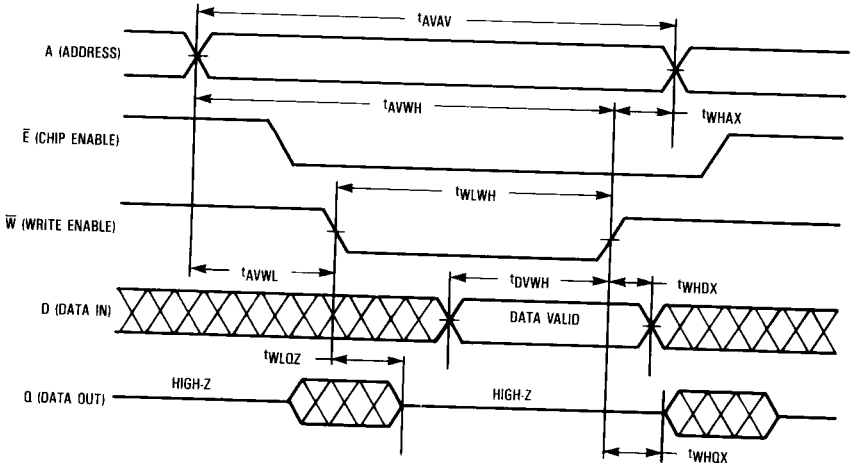
READ CYCLE 2 (See Note 3 Above)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)

Parameter	Symbol		MCM6287-25		MCM6287-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	–	35	–	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	–	25	–	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	20	–	20	–	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	15	–	15	–	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	15	0	15	ns	3,4
Write High to Output Active	t_{WHQX}	t_{OW}	5	–	5	–	ns	3,4
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. Parameter is sampled and not 100% tested.



AC TEST LOADS

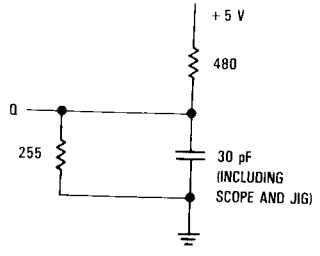


Figure 1A

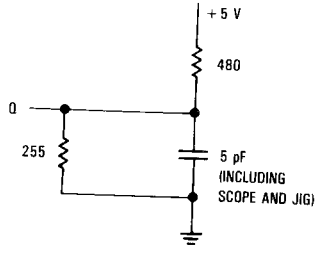


Figure 1B

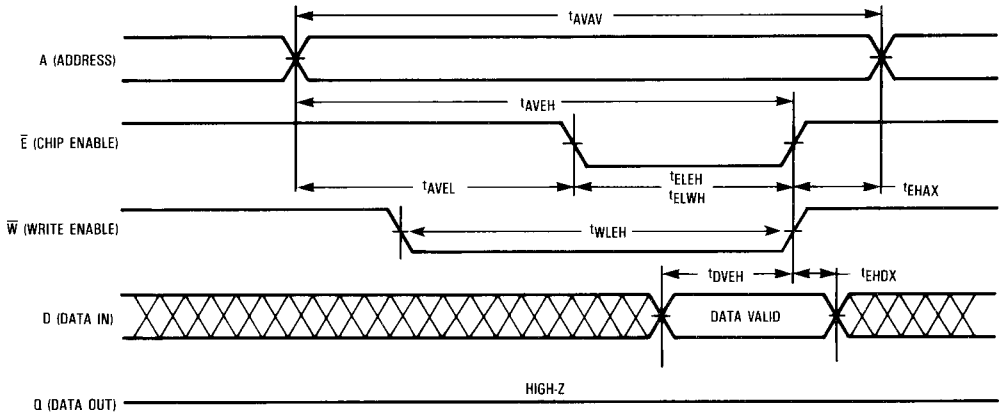
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)

Parameter	Symbol		MCM6287-25		MCM6287-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	–	35	–	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	–	0	–	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	20	–	25	–	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	20	–	25	–	ns	3,4
Enable to End of Write	t_{ELWH}	t_{CW}	20	–	25	–	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	20	–	20	–	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	15	–	15	–	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	–	0	–	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	–	0	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



TYPICAL CHARACTERISTICS

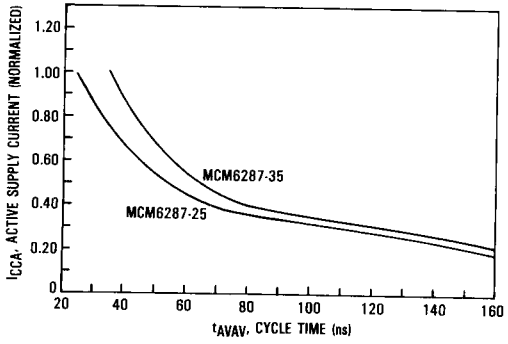


Figure 2. Relative Power versus Cycle Time

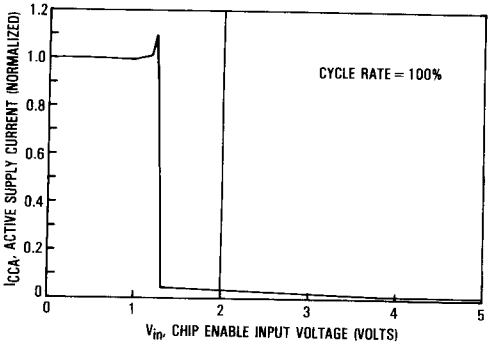


Figure 3. Active Supply Current versus Chip Enable Input Voltage

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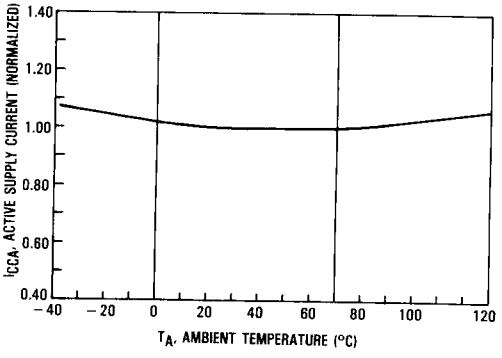


Figure 4. Active Supply Current versus Temperature

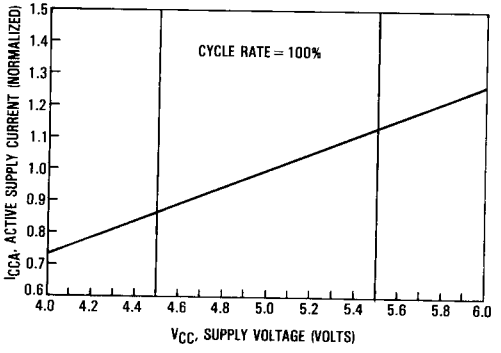


Figure 5. Active Supply Current versus Supply Voltage

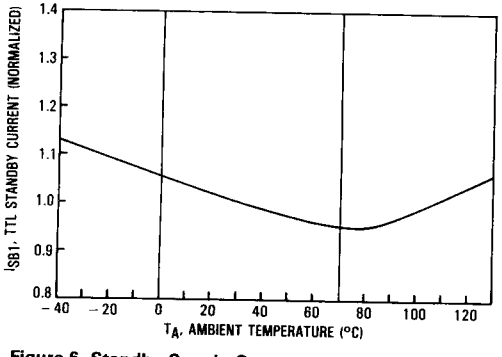


Figure 6. Standby Supply Current versus Temperature

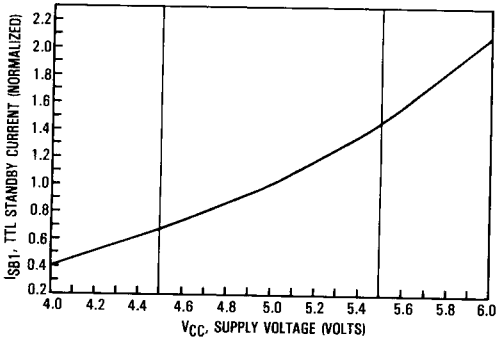


Figure 7. Standby Supply Current versus Supply Voltage

TYPICAL CHARACTERISTICS (Continued)

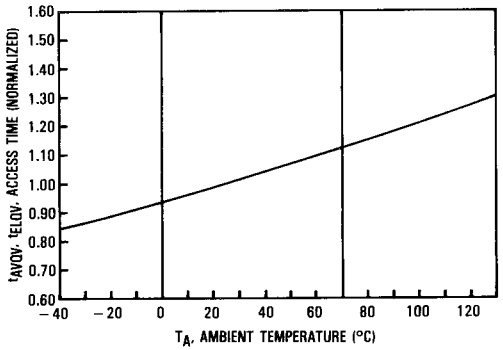


Figure 8. Address and Enable Access Times versus Temperature

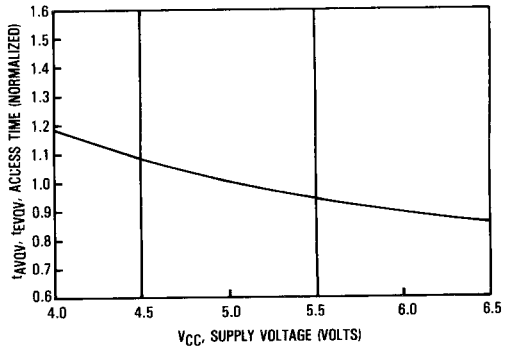


Figure 9. Address and Enable Access Times versus Supply Voltage

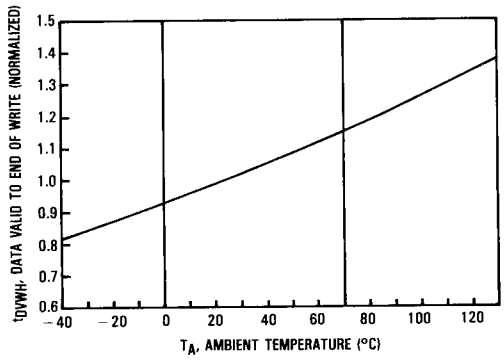


Figure 10. Data Setup Time versus Temperature

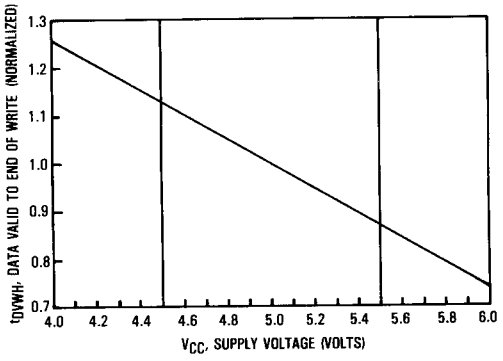


Figure 11. Data Setup Time versus Supply Voltage

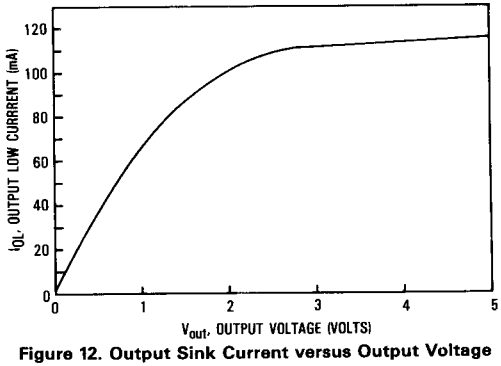


Figure 12. Output Sink Current versus Output Voltage

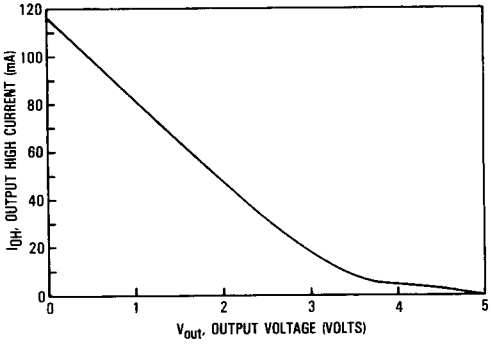
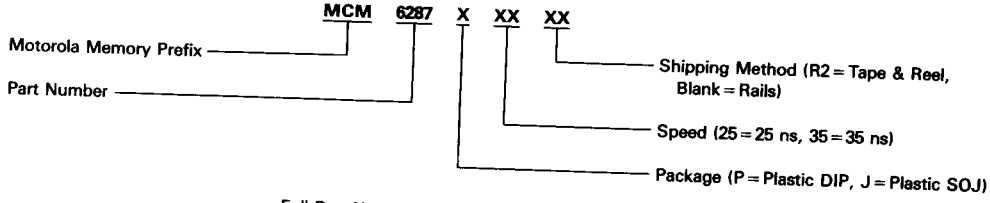


Figure 13. Output Source Current versus Output Voltage

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM6287P25, MCM6287J25, MCM6287J25R2, MCM6287P35, MCM6287J35, MCM6287J35R2

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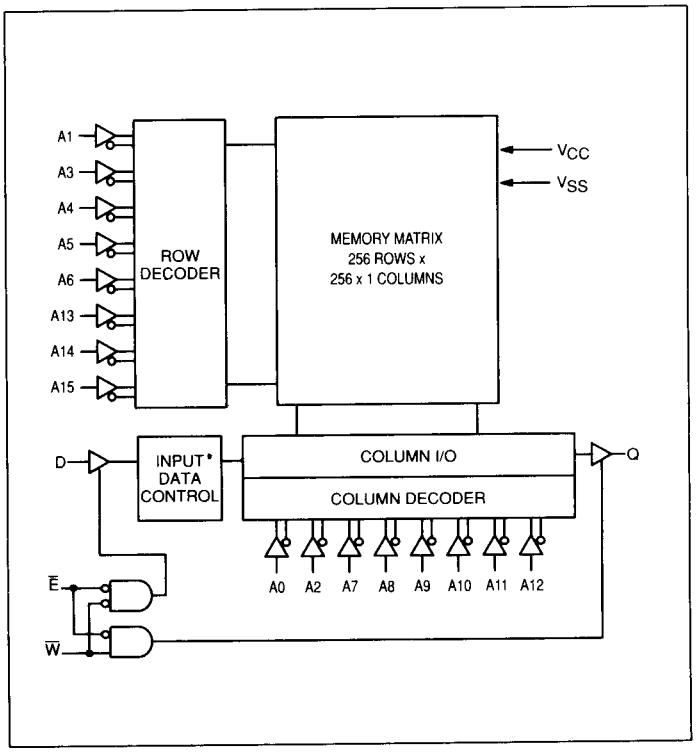
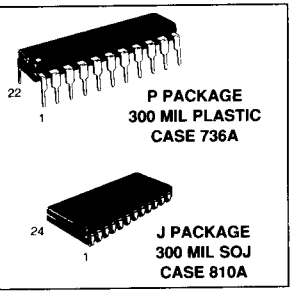
64K x 1 Bit Fast Static RAM

MCM6287-12, -15, -20
See QuickRAM, Page 7-122

MCM6287C-8, -10
See QuickRAM II, Page 7-142





DUAL-IN-LINE

A0	1	22	VCC
A1	2	21	A15
A2	3	20	A14
A3	4	19	A13
A4	5	18	A12
A5	6	17	A11
A6	7	16	A10
A7	8	15	A9
Q	9	14	A8
W	10	13	D
VSS	11	12	E

SOJ

A0	1	24	VCC
A1	2	23	A15
A2	3	22	A14
A3	4	21	A13
A4	5	20	A12
A5	6	19	NC
NC	7	18	A11
A6	8	17	A10
A7	9	16	A9
Q	10	15	A8
W	11	14	D
VSS	12	13	E

PIN NAMES

A0-A15	Address Input	Q	Data Output
E	Chip Enable	VCC	+5 V Power Supply
W	Write Enable	VSS	Ground
D	Data Input	NC	No Connection

MCM6287 TRUTH TABLE (X = don't care)

E	W	Mode	VCC Current	Output	Cycle
H	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

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Advance Information
QuickRAM™
Fast Static RAM Family

The QuickRAM Family of fast static RAMs is fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The product family includes devices with four different densities: 294,912 bits, 262,144 bits, 73,728 bits, and 65,536 bits.

These devices meet JEDEC standards for functionality and pinout, and are available in plastic dual-in-line and plastic small-outline J-leaded packages.

- Single 5 V ±10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 12, 15, 17, 20, and 25 ns
- Equal Address and Chip Enable Access Times
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems — on MCM6205/06, MCM6209, MCM6264/65, and MCM6290
- Low Power Operation: 120–160 mA Maximum AC
- Fully TTL Compatible — Three State Output
- Separate Data Input and Output on MCM6207 and MCM6287

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256K

256K x 1
MCM6207-15, -20, -25

64K x 4
MCM6208-15, -20, -25

64K x 4 with OE
MCM6209-15, -20, -25

32K x 8
MCM6206-17, -20, -25

32K x 9
MCM6205-17, -20, -25

64K

64K x 1
MCM6287-12, -15, -20

16K x 4
MCM6288-12, -15

16K x 4 with OE
MCM6290-12, -15

8K x 8
MCM6264-15, -20

8K x 9
MCM6265-15, -20, -25

CONTENTS

DEVICE NUMERICAL INDEX

Part Number	Access Times (ns)	Organization	Page
MCM6205-17, -20, -25	17, 20, 25	32K x 9	14
MCM6206-17, -20, -25	17, 20, 25	32K x 8	12
MCM6207-15, -20, -25	15, 20, 25	256K x 1	8
MCM6208-15, -20, -25	15, 20, 25	64K x 4	10
MCM6209-15, -20, -25	15, 20, 25	64K x 4 OE	10
MCM6264-15, -20	15, 20	8K x 8	13
MCM6265-15, -20, -25	15, 20, 25	8K x 9	15
MCM6287-12, -15, -20	12, 15, 20	64K x 1	9
MCM6288-12, -15	12, 15	16K x 4	11
MCM6290-12, -15	12, 15	16K x 4 OE	11

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to +7	V
Voltage on Any Pin, Except V_{CC}, Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±30	mA
Power Dissipation	P_D	1	W
Temperature Under Bias	T_{bias}	– 10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature-Plastic	T_{stg}	– 55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the OPERATING CONDITIONS. Exposure to voltages higher than the operating voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

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DC OPERATING CONDITIONS AND CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Parameter	Conditions	Symbol	Min	Max	Unit
Supply Voltage	Operating Voltage Range	V_{CC}	4.5	5.5	V
Input High Voltage		V_{IH}	2.2	V_{CC}+0.3*	V
Input Low Voltage		V_{IL}	–0.5**	0.8	V
Input Leakage Current	$0 V \le V_{in} \le V_{CC}$	$I_{lkg(I)}$	—	±1	µA
Output Leakage Current	Output(s) Disabled, $0 V \le V_{out} \le V_{CC}$	$I_{lkg(O)}$	—	±1	µA
Output High Voltage	I_{OH} = –4 mA	V_{OH}	2.4	—	V
Output Low Voltage	I_{OL} = 8 mA	V_{OL}	—	0.4	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)

**V_{IL} (min) = –0.5 V dc, V_{IL} (min) = –2 V ac (pulse width ≤ 20 ns)

POWER SUPPLY CURRENTS (AC Operating Conditions Unless Otherwise Noted)

Density	Config.	Device	Parameter	Symbol	-12	-15	-17	-20	-25	Unit
64K	16K x 4	MCM6288/90	AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	150	140	—	—	—	mA
	64K x 1	MCM6287			150	140	—	130	—	
	8K x 8	MCM6264			—	140	—	130	—	
	8K x 9	MCM6265			—	140	—	130	120	
	All	All	AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, f = f_{max})	I_{SB1}	45	40	—	35	30	mA
	All	All	CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E} \geq V_{CC} - 0.2$ V* $V_{in} \leq V_{SS}$ +0.2 V, or $\geq V_{CC}$ −0.2 V)	I_{SB2}	20	20	—	20	20	mA
256K	64K x 4	MCM6208/09	AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	—	155	—	145	135	mA
	256K x 1	MCM6207			—	150	—	140	130	
	32K x 8	MCM6206			—	—	155	150	140	
	32K x 9	MCM6205			—	—	160	155	145	
	All	All	AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, f = f_{max})	I_{SB1}	—	50	45	45	40	mA
	All	All	CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E} \geq V_{CC} - 0.2$ V* $V_{in} \leq V_{SS}$ +0.2 V, or $\geq V_{CC}$ −0.2 V)	I_{SB2}	—	20	20	20	20	mA

*For devices with multiple chip enables of opposite polarity, $\overline{E1} \geq V_{CC} - 0.2$ V or E2 $\leq V_{SS} + 0.2$ V

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Address and Data Input Capacitance	C_{in}		pF
MCM6287 (64K x 1), MCM6288/90 (16K x 4)		6	
MCM6264 (8K x 8), MCM6265 (8K x 9)		6	
MCM6207 (256K x 1), MCM6208/09 (64K x 4)		6	
MCM6205 (32K x 9), MCM6206 (32K x 8)		6	
Control Pin Input Capacitance ($\overline{E}$,* $\overline{G}$, $\overline{W}$)	C_{in}		pF
MCM6287 (64K x 1), MCM6288/90 (16K x 4)		6	
MCM6264 (8K x 8), MCM6265 (8K x 9)		6	
MCM6207 (256K x 1), MCM6208/09 (64K x 4)		6	
MCM6205 (32K x 9), MCM6206 (32K x 8)		8	
Output Capacitance	C_{out}		pF
MCM6287 (64K x 1), MCM6288/90 (16K x 4)		7	
MCM6264 (8K x 8), MCM6265 (8K x 9)		7	
MCM6207 (256K x 1), MCM6208/09 (64K x 4)		8	
MCM6205 (32K x 9), MCM6206 (32K x 8)		8	

*For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

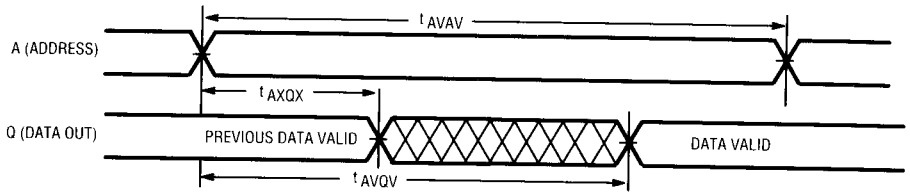
READ CYCLE (See Notes 1 and 2)

Product Family	Configuration	-12	-15	-17	-20	-25	Density
MCM6288 and MCM6290	16K x 4	√	√	—	EXISTING MOTOROLA PRODUCTS		64K
MCM6287	64K x 1	√	√	—	√		
MCM6264	8K x 8	FUTURE MOTOROLA PRODUCTS	√	—	√		
MCM6265	8K x 9		√	—	√	√	
MCM6208 and MCM6209	64K x 4		√	—	√	√	256K
MCM6207	256K x 1		√	—	√	√	
MCM6206	32K x 8			√	√	√	
MCM6205	32K x 9			√	√	√	

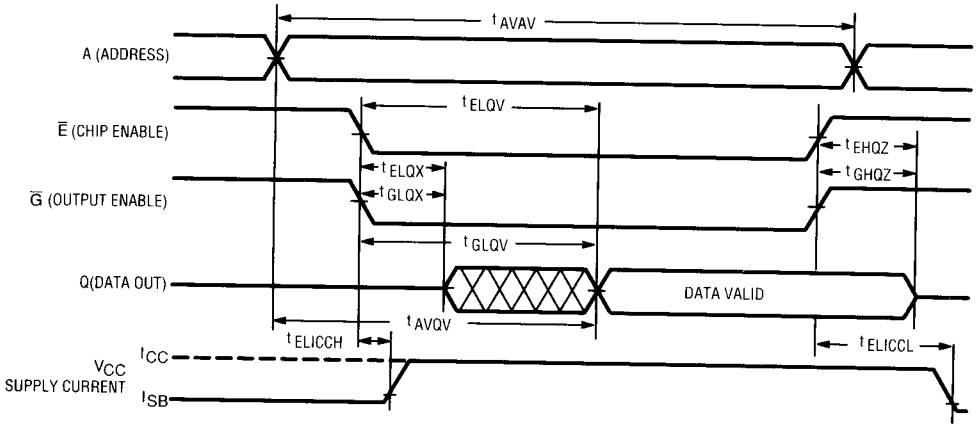
Parameter	Symbol Std	Symbol Alt	-12 Min	-12 Max	-15 Min	-15 Max	-17 Min	-17 Max	-20 Min	-20 Max	-25 Min	-25 Max	Unit	Notes
Read Cycle Time	t_{AVAV}	t_{RC}	12	—	15	—	17	—	20	—	25	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	12	—	15	—	17	—	20	—	25	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	12	—	15	—	17	—	20	—	25	ns	4
Output Enable Access Time	t_{GLQV}	t_{OE}	—	6	—	8	—	9	—	10	—	12	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	4	—	4	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	4	—	4	—	4	—	ns	5,6,7
Output Enable Low to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	0	—	ns	5,6,7
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	6	0	8	0	8	0	9	0	10	ns	5,6,7
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	6	0	7	0	8	0	8	0	10	ns	5,6,7
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	12	—	15	—	17	—	20	—	25	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected. $\overline{E} \le V_{IL}$ and $\overline{G} \le V_{IL}$.

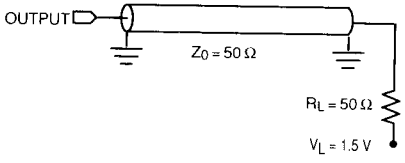
READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Notes 2 and 4)



AC TEST LOADS



See Output Load Conditions, page 18.

Figure 1A

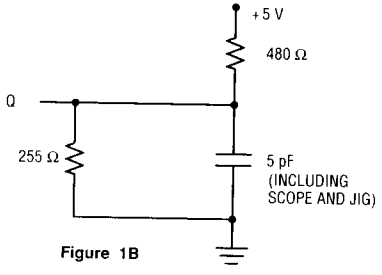
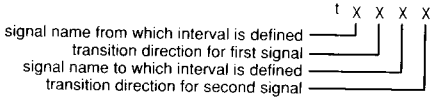


Figure 1B

TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are:
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device output will be valid no later than that time.

WRITE CYCLES

Product Family	Configuration	-12	-15	-17	-20	-25	Density
MCM6288 and MCM6290	16K x 4	√	√	—	EXISTING MOTOROLA PRODUCTS		64K
MCM6287	64K x 1	√	√	—	√		
MCM6264	8K x 8	FUTURE MOTOROLA PRODUCTS	√	—	√		
MCM6265	8K x 9		√	—	√	√	
MCM6208 and MCM6209	64K x 4		√	—	√	√	256K
MCM6207	256K x 1		√	—	√	√	
MCM6206	32K x 8			√	√	√	
MCM6205	32K x 9			√	√	√	

WRITE CYCLE 1 ($\overline{W}$ Controlled) (See Notes 1, 2, and 3)

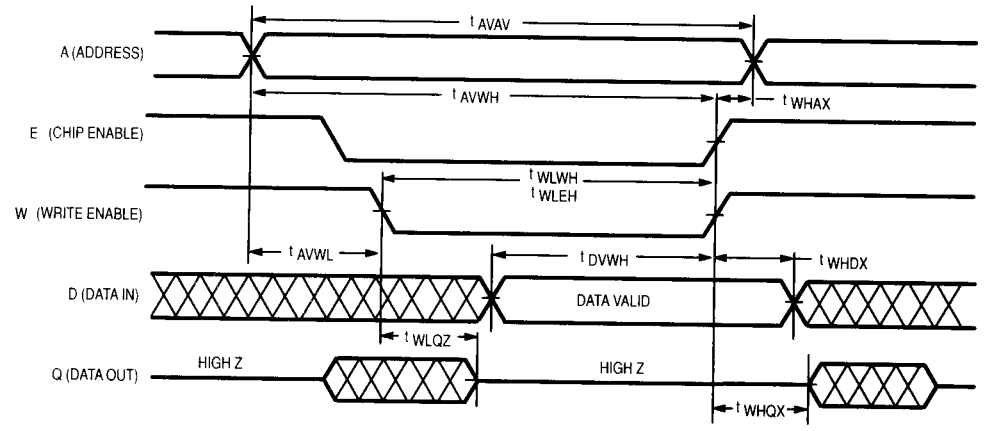
Parameter	Symbol Std	Symbol Alt	-12 Min	-12 Max	-15 Min	-15 Max	-17 Min	-17 Max	-20 Min	-20 Max	-25 Min	-25 Max	Unit	Notes
Write Cycle Time	t_{AVAV}	t_{WC}	12	—	15	—	17	—	20	—	25	—	ns	4
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	10	—	12	—	14	—	15	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	10	—	12	—	14	—	15	—	20	—	ns	
Write Pulse Width, $\overline{G}$ High (Output Enable devices)	t_{WLWH}, t_{WLEH}	t_{WP}	8	—	10	—	11	—	12	—	15	—	ns	5
Data Valid to End of Write	t_{DVWH}	t_{DW}	6	—	7	—	8	—	8	—	10	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	6	0	7	0	8	0	8	0	10	ns	6,7,8
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	4	—	4	—	4	—	ns	6,7,8
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

WRITE CYCLE 2 ($\overline{E}$ Controlled) (See Notes 1, 2, and 3)

Parameter	Symbol Std	Symbol Alt	-12 Min	-12 Max	-15 Min	-15 Max	-17 Min	-17 Max	-20 Min	-20 Max	-25 Min	-25 Max	Unit	Notes
Write Cycle Time	t_{AVAV}	t_{WC}	12	—	15	—	17	—	20	—	25	—	ns	4
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	10	—	12	—	14	—	15	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	t_{CW}	8	—	10	—	11	—	12	—	15	—	ns	9,10
Data Valid to End of Write	t_{DVEH}	t_{DW}	6	—	7	—	8	—	8	—	10	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

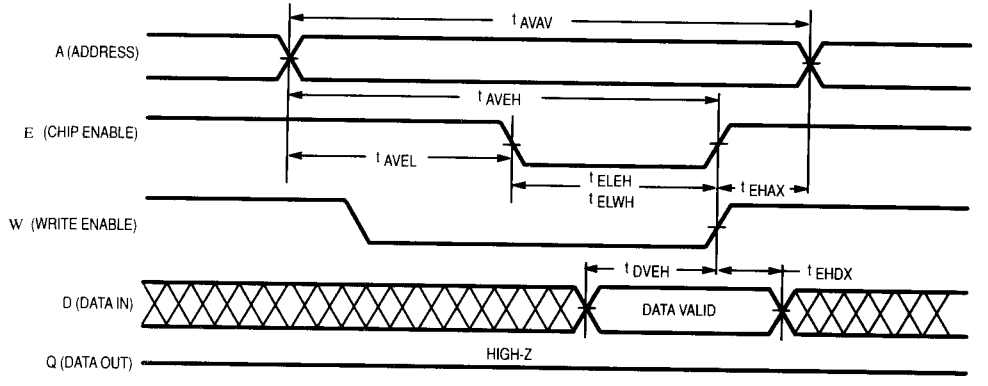
NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For devices with multiple chip enables, $\overline{E}1$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. For Output Enable devices, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. For Output Enable devices, if $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
6. At any given voltage and temperature, t_{WLQG} max < t_{WHQX} min, both for a given device and from device to device.
7. Transition is measured 500 mV from steady-state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.
9. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
10. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 1 (See Note 2)



7

WRITE CYCLE 2 (See Note 2)



Product Preview

QuickRAM™ II
Fast Static RAM Family

The QuickRAM Family of fast static RAMs is fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The product family includes devices with four different densities: 294,912 bits, 262,144 bits, 73,728 bits, and 65,536 bits.

These devices meet JEDEC standards for functionality and pinout, and are available in plastic dual-in-line and plastic small-outline J-leaded packages.

- Single 5 V ±10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 8, 10, 12, and 15 ns
- Equal Address and Chip Enable Access Times
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems — on MCM6205/06, MCM6209, MCM6264/65, and MCM6290
- Low Power Operation: 150–180 mA Maximum AC
- Fully TTL Compatible — Three State Output
- Separate Data Input and Output on MCM6207 and MCM6287

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256K

256K x 1
MCM6207C-10, -12

64K x 4
MCM6208C-10, -12

64K x 4 with OE
MCM6209C-10, -12

32K x 8
MCM6206C-12, -15

32K x 9
MCM6205C-12, -15

64K

64K x 1
MCM6287C-8, -10

16K x 4
MCM6288C-8, -10

16K x 4 with OE
MCM6290C-8, -10

8K x 8
MCM6264C-10, -12

8K x 9
MCM6265C-10, -12

CONTENTS

DEVICE NUMERICAL INDEX (See Note)

Part Number	Access Times (ns)	Organization	Page
MCM6205C-12, -15	12, 15	32K x 9	14
MCM6206C-12, -15	12, 15	32K x 8	12
MCM6207C-10, -12	10, 12	256K x 1	8
MCM6208C-10, -12	10, 12	64K x 4	10
MCM6209C-10, -12	10, 12	64K x 4 OE	10
MCM6264C-10, -12	10, 12	8K x 8	13
MCM6265C-10, -12	10, 12	8K x 9	15
MCM6287C-8, -10	8, 10	64K x 1	9
MCM6288C-8, -10	8, 10	16K x 4	11
MCM6290C-8, -10	8, 10	16K x 4 OE	11

NOTE: Device Specifications for the faster access times are included to assist future system designs. Contact a Motorola Sales Representative for scheduled availability.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to +7	V
Voltage on Any Pin, Except V_{CC}, Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±30	mA
Power Dissipation	P_D	1	W
Temperature Under Bias	T_{bias}	– 10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature-Plastic	T_{stg}	– 55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the OPERATING CONDITIONS. Exposure to voltages higher than the operating voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

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DC OPERATING CONDITIONS AND CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Parameter	Conditions	Symbol	Min	Max	Unit
Supply Voltage	Operating Voltage Range	V_{CC}	4.5	5.5	V
Input High Voltage		V_{IH}	2.2	V_{CC}+0.3*	V
Input Low Voltage		V_{IL}	–0.5**	0.8	V
Input Leakage Current	0 V ≤ V_{in} ≤ V_{CC}	$I_{lkg(I)}$	—	±1	µA
Output Leakage Current	Output(s) Disabled, 0 V ≤ V_{out} ≤ V_{CC}	$I_{lkg(O)}$	—	±1	µA
Output High Voltage	I_{OH} = –4 mA	V_{OH}	2.4	—	V
Output Low Voltage	I_{OL} = 8 mA	V_{OL}	—	0.4	V

**V_{IL} (min) = –0.5 V dc, V_{IL} (min) = –2 V ac (pulse width ≤ 20 ns)

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)

POWER SUPPLY CURRENTS (AC Operating Conditions Unless Otherwise Noted)

Density	Config.	Device	Parameter	Symbol	-8	-10	-12	-15	Unit
64K	16K x 4	MCM6288C/90C	AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	180	170	—	—	mA
	64K x 1	MCM6287C			170	160	—	—	
	8K x 8	MCM6264C			—	170	150	—	
	8K x 9	MCM6265C			—	170	150	—	
	All	All	AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, f = f_{max})	I_{SB1}	55	50	45	40	mA
	All	All	CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E} \geq V_{CC} - 0.2$ V* $V_{in} \leq V_{SS}$ +0.2 V, or $\geq V_{CC}$ −0.2 V)	I_{SB2}	20	20	20	20	mA
256K	64K x 4	MCM6208C/09C	AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	—	175	165	—	mA
	256K x 1	MCM6207C			—	170	160	—	
	32K x 8	MCM6206C			—	—	175	165	
	32K x 9	MCM6205C			—	—	180	170	
	All	All	AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, f = f_{max})	I_{SB1}	—	60	55	50	mA
	All	All	CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E} \geq V_{CC} - 0.2$ V* $V_{in} \leq V_{SS}$ +0.2 V, or $\geq V_{CC}$ −0.2 V)	I_{SB2}	—	20	20	20	mA

*For devices with multiple chip enables of opposite polarity, $\overline{E1} \geq V_{CC} - 0.2$ V or E2 ≤ V_{SS} + 0.2 V

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Address and Data Input Capacitance	C_{in}		pF
MCM6287C (64K x 1), MCM6288C/90C (16K x 4)		6	
MCM6264C (8K x 8), MCM6265C (8K x 9)		6	
MCM6207C (256K x 1), MCM6208C/09C (64K x 4)		6	
MCM6205C (32K x 9), MCM6206C (32K x 8)		6	
Control Pin Input Capacitance ($\overline{E}$,* $\overline{G}$, $\overline{W}$)	C_{in}		pF
MCM6287C (64K x 1), MCM6288C/90C (16K x 4)		6	
MCM6264C (8K x 8), MCM6265C (8K x 9)		6	
MCM6207C (256K x 1), MCM6208C/09C (64K x 4)		6	
MCM6205C (32K x 9), MCM6206C (32K x 8)		8	
Output Capacitance	C_{out}		pF
MCM6287C (64K x 1), MCM6288C/90C (16K x 4)		7	
MCM6264C (8K x 8), MCM6265C (8K x 9)		7	
MCM6207C (256K x 1), MCM6208C/09C (64K x 4)		8	
MCM6205C (32K x 9), MCM6206C (32K x 8)		8	

*For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

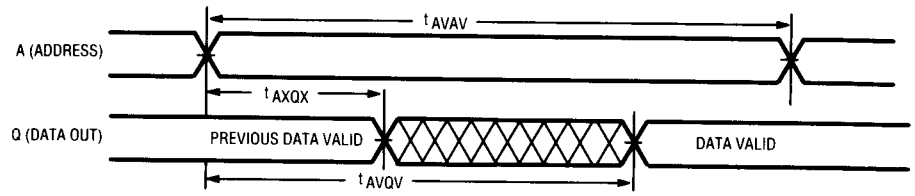
READ CYCLE (See Notes 1 and 2)

Product Family	Configuration	-8	-10	-12	-15	Density
MCM6288C and MCM6290C	16K x 4	√	√	EXISTING MOTOROLA PRODUCTS		64K
MCM6287C	64K x 1	√	√			
MCM6264C	8K x 8	FUTURE MOTOROLA PRODUCTS	√			
MCM6265C	8K x 9		√			
MCM6208C and MCM6209C	64K x 4		√			256K
MCM6207C	256K x 1		√			
MCM6206C	32K x 8			√	√	
MCM6205C	32K x 9			√	√	

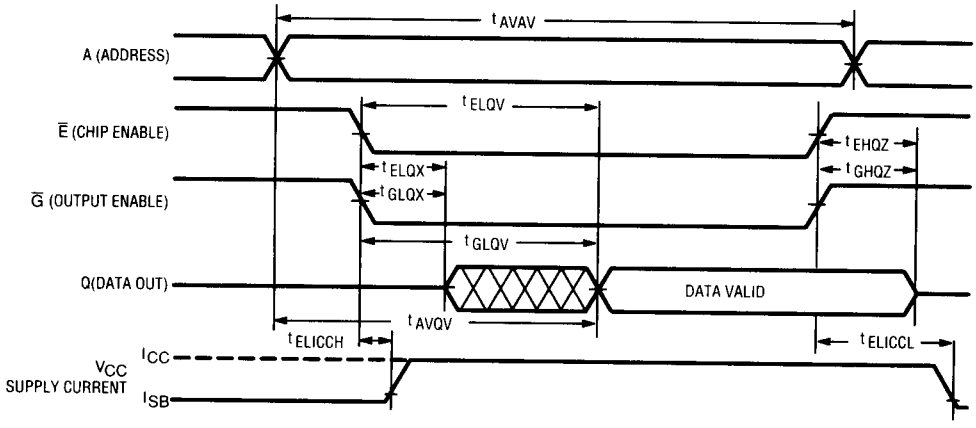
Parameter	Symbol		-8		-10		-12		-15		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	8	—	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	8	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	8	—	10	—	12	—	15	ns	4
Output Enable Access Time	t_{GLQV}	t_{OE}	—	4	—	5	—	6	—	8	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	4	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	4	—	4	—	ns	5,6,7
Output Enable Low to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	ns	5,6,7
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	4	0	5	0	6	0	8	ns	5,6,7
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	4	0	5	0	6	0	7	ns	5,6,7
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	8	—	10	—	12	—	15	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected. $\overline{E} \leq V_{IL}$ and $\overline{G} \leq V_{IL}$.

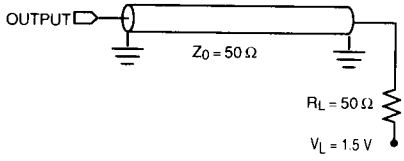
READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Notes 2 and 4)



AC TEST LOADS



See Output Load Conditions, page 18.

Figure 1A

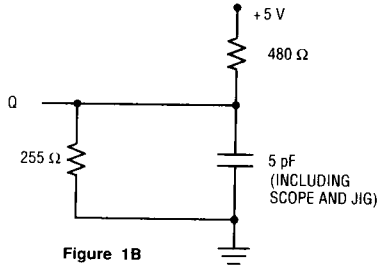
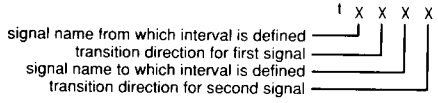


Figure 1B

TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are:
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device output will be valid no later than that time.

WRITE CYCLES

Product Family	Configuration	-8	-10	-12	-15	Density
MCM6288C and MCM6290C	16K x 4	√	√	EXISTING MOTOROLA PRODUCTS		64K
MCM6287C	64K x 1	√	√			
MCM6264C	8K x 8	FUTURE MOTOROLA PRODUCTS	√	√		
MCM6265C	8K x 9		√	√		
MCM6208C and MCM6209C	64K x 4		√	√		256K
MCM6207C	256K x 1		√	√		
MCM6206C	32K x 8			√	√	
MCM6205C	32K x 9			√	√	

WRITE CYCLE 1 ($\overline{W}$ Controlled) (See Notes 1, 2, and 3)

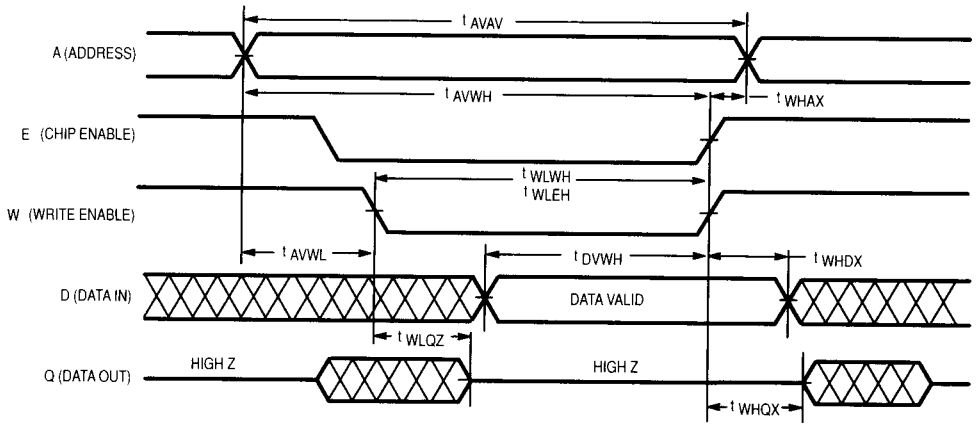
Parameter	Symbol Std	Symbol Alt	-8 Min	-8 Max	-10 Min	-10 Max	-12 Min	-12 Max	-15 Min	-15 Max	Unit	Notes
Write Cycle Time	t_{AVAV}	t_{WC}	8	—	10	—	12	—	15	—	ns	4
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	8	—	9	—	10	—	12	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	8	—	9	—	10	—	12	—	ns	
Write Pulse Width, $\overline{G}$ High (Output Enable devices)	t_{WLWH}, t_{WLEH}	t_{WP}	6	—	7	—	8	—	10	—	ns	5
Data Valid to End of Write	t_{DVWH}	t_{DW}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	4	0	5	0	6	0	7	ns	6,7,8
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	4	—	4	—	ns	6,7,8
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	

WRITE CYCLE 2 ($\overline{E}$ Controlled) (See Notes 1, 2, and 3)

Parameter	Symbol Std	Symbol Alt	-8 Min	-8 Max	-10 Min	-10 Max	-12 Min	-12 Max	-15 Min	-15 Max	Unit	Notes
Write Cycle Time	t_{AVAV}	t_{WC}	8	—	10	—	12	—	15	—	ns	4
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	8	—	9	—	10	—	12	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	t_{CW}	6	—	7	—	8	—	10	—	ns	9,10
Data Valid to End of Write	t_{DVEH}	t_{DW}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	

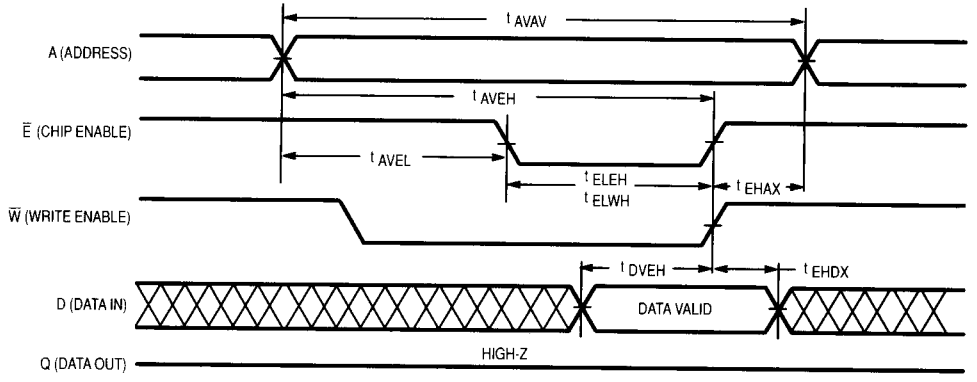
NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. For Output Enable devices, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. For Output Enable devices, if $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
6. At any given voltage and temperature, t_{WLQG} max < t_{WHQX} min, both for a given device and from device to device.
7. Transition is measured 500 mV from steady-state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.
9. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
10. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 1 (See Note 2)



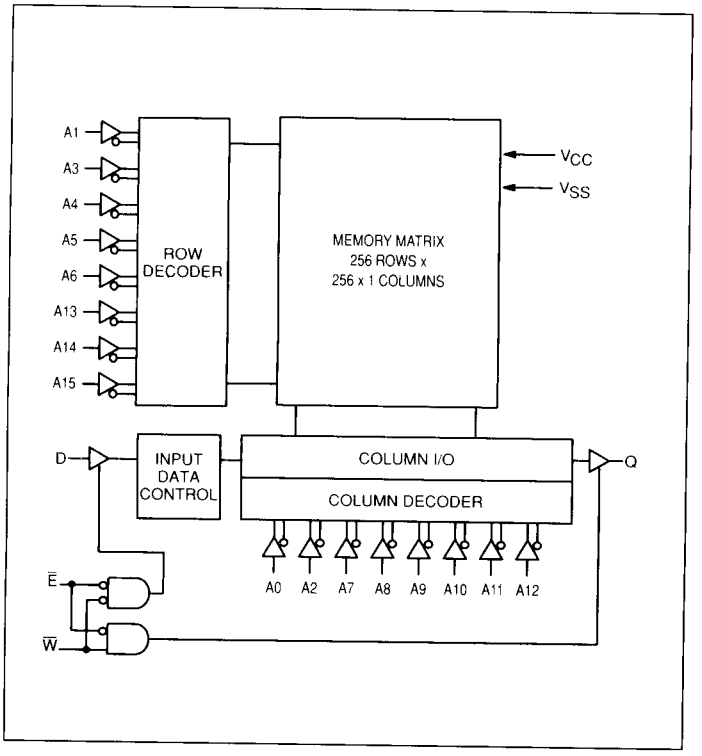
7

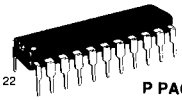
WRITE CYCLE 2 (See Note 2)



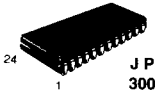
64K x 1 Bit Fast Static RAM

MCM6287C



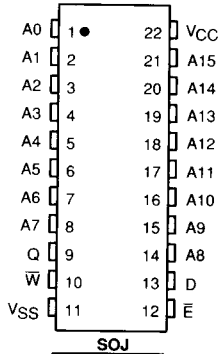


P PACKAGE
300 MIL PLASTIC
CASE 736A

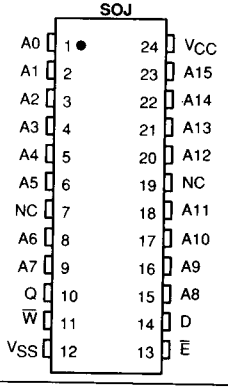


J PACKAGE
300 MIL SOJ
CASE 810A

DUAL-IN-LINE



SOJ



PIN NAMES			
A0-A15	Address Input	Q	Data Output
$\overline{E}$	Chip Enable	V_{CC}	+5 V Power Supply
$\overline{W}$	Write Enable	V_{SS}	Ground
D	Data Input	NC	No Connection

MCM6287C TRUTH TABLE (X = don't care)

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

ORDERING INFORMATION (Order by Full Part Number)

MCM 6287 C X XX XX

- MCM — Motorola Memory Prefix
- 6287 — Part Number
- C — Revision
- X — Package (P = 300 mil Plastic DIP, J = 300 mil SOJ)
- XX — Speed (10 = 10 ns)
- XX — Shipping Method (R2 = Tape & Reel, Blank = Rails)

Full Part Numbers—MCM6287CP10 MCM6287CJ10 MCM6287CJ10R2