August 1992
Edition 2.0A

FUJITSU

DATA SHEET

MB814260A-70/-80/-10

CMOS 256K x 16 Bits Fast Page Mode Dynamic RAM

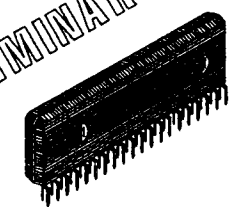
The Fujitsu MB814260A is a fully decoded CMOS Dynamic RAM (DRAM) that contains 4,194,304 memory cells accessible in 16- or 8-bit increments. The MB814260A features a fast page mode of operation whereby high-speed access of up to 512 x 16 bits of data can be selected in the same row. The MB814260A DRAM is ideally suited for memory applications where very low power dissipation and high bandwidth are basic requirements of the design such as embedded control buffers, portable computers, and video imaging equipment.

The MB814260A is fabricated using silicon gate CMOS and Fujitsu's advanced four-layer polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes.

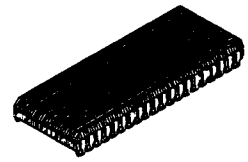
Parameter		MB814260A-70	MB814260A-80	MB814260A-10
$\overline{RAS}$ Access Time		70 ns max.	80 ns max.	100 ns max.
$\overline{CAS}$ Access Time		20 ns max.	20 ns max.	25 ns max.
Address Access Time		35 ns max.	40 ns max.	45 ns max.
Random Cycle Time		125 ns min.	140 ns min.	170 ns min.
Fast Page Mode Cycle Time		45 ns min.	50 ns min.	55 ns min.
Low Power Dissipation	Operating Current	853 mW max.	770 mW max.	633 mW max.
	Standby Current	11 mW max. (TTL level)/5.5 mW max. (CMOS level)		

- 262,144 words x 16 bits organization
- Silicon gate, CMOS, 3D-stacked capacitor cell
- All inputs and outputs are TTL compatible
- 512 refresh cycles every 8.2 ms
- 9 rows x 9 columns address scheme
- 1 $\overline{WE}$/2 $\overline{CAS}$
- Early write or $\overline{OE}$ controlled write capability
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or hidden refresh
- Fast page mode, Read-Modify-Write capability
- On-chip substrate bias generator for high performance

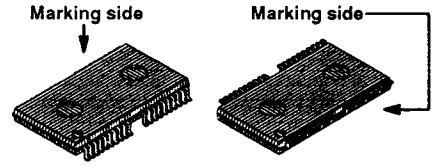
PRELIMINARY



Plastic ZIP
(ZIP-40P-M01)



Plastic SOJ
(LCC-40P-M01)



Plastic TSOP-II

(normal bend leads)
(FPT-44P-M07)

(reverse bend leads)
(FPT-44P-M08)

Package and Ordering Information

- 40-pin plastic (475 mil) ZIP, order as MB814260A-xxPZ
- 40-pin plastic (400 mil) SOJ, order as MB814260A-xxPJ
- 44-pin plastic (400 mil) TSOP-II with normal bend leads, order as MB814260A-xxPFTN
- 44-pin plastic (400 mil) TSOP-II with reverse bend leads, order as MB814260A-xxPFTR

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

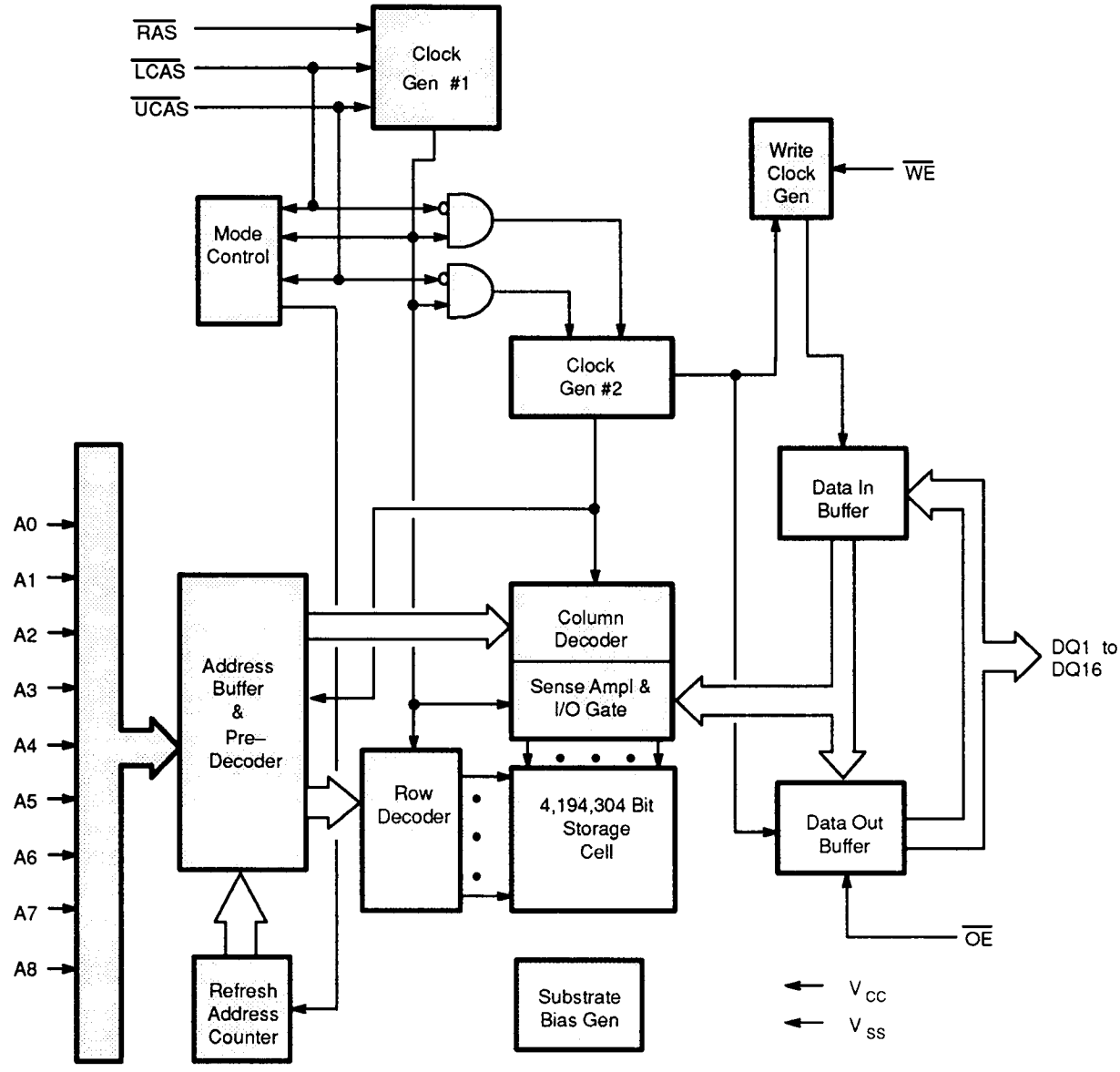
Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Voltage at any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Power dissipation	PD	1.0	W
Short circuit output current	—	50	mA
Storage temperature	T_{STG}	−55 to +125	°C

— Note —

Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 – MB814260A DYNAMIC RAM – BLOCK DIAGRAM

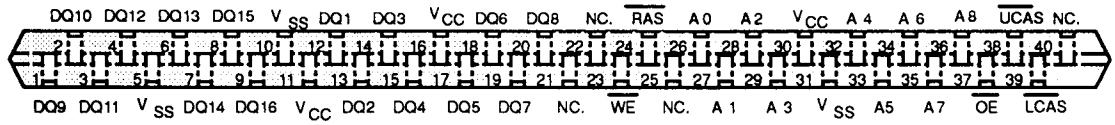


CAPACITANCE (T_A = 25°C, f = 1MHz)

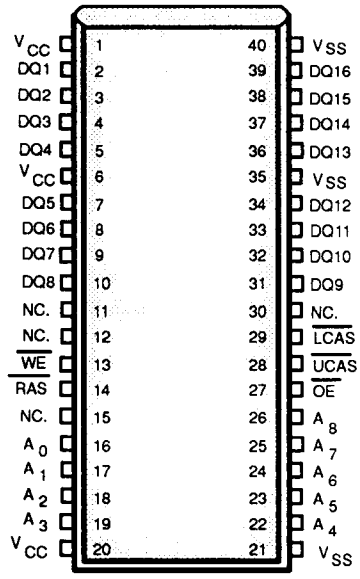
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A8	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}	—	7	pF
Input/Output Capacitance, DQ1 to DQ16	C_{DQ}	—	7	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

40–Pin ZIP:
(TOP VIEW)

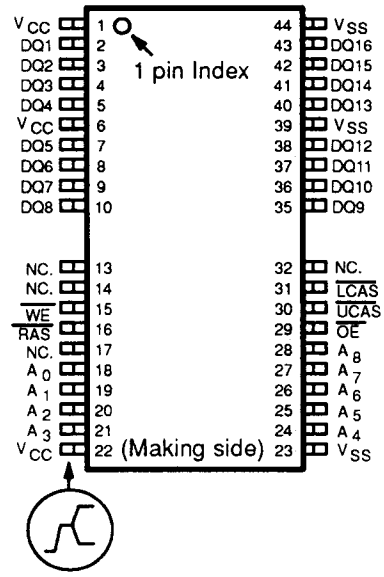


40–Pin SOJ:
(TOP VIEW)

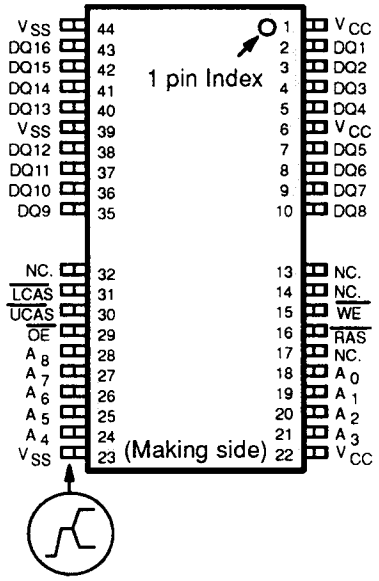


44–Pin FPT:
(TOP VIEW)

<Normal Bend : FPT–44P–M07>



<Reverse Bend : FPT–44P–M08>



Designator	Function
A0 to A8	Address inputs. row : A0 to A8 column : A0 to A8 refresh : A0 to A8
$\overline{RAS}$	Row address strobe.
$\overline{LCAS}$	Lower column address strobe
$\overline{UCAS}$	Upper column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable.
DQ1 to DQ16	Data Input/ Output
VCC	+5 volt power supply.
VSS	Circuit ground.

RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	−2.0	—	0.8	V	
Input Low Voltage, DQ(*)	1	VILD	−1.0	—	0.8	V	

* : Undershoots of up to −2.0 volts with a pulse width not exceeding 20ns are acceptable.

FUNCTIONAL OPERATION

ADDRESS INPUTS

Eighteen input bits are required to decode any sixteen of 4,194,304 cell addresses in the memory matrix. Since only nine address bits are available, the column and row inputs are separately strobed by $\overline{LCAS}$ or $\overline{UCAS}$ and $\overline{RAS}$ as shown in Figure 5. First, nine row address bits are input on pins A0–through–A8 and latched with the row address strobe ($\overline{RAS}$) then, nine column address bits are input and latched with the column address strobe ($\overline{LCAS}$ or $\overline{UCAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{LCAS}$ or $\overline{UCAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Input data is written into memory in either of three basic ways—an early write cycle, an $\overline{OE}$ (delayed) write cycle, and a read–modify–write cycle. The falling edge of $\overline{WE}$ or $\overline{LCAS}$ / $\overline{UCAS}$, whichever is later, serves as the input data–latch strobe. In an early write cycle, the input data of DQ1–DQ8 is strobed by $\overline{LCAS}$ and DQ9–DQ16 is strobed by $\overline{UCAS}$ and the setup/hold times are referenced to each $\overline{LCAS}$ and $\overline{UCAS}$ because $\overline{WE}$ goes Low before $\overline{LCAS}$ / $\overline{UCAS}$. In a delayed write or a read–modify–write cycle, $\overline{WE}$ goes Low after $\overline{LCAS}$ / $\overline{UCAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write–enable signal.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{LCAS}$ (for DQ1–DQ8) $\overline{UCAS}$ (for DQ9–DQ16) when t_{RCD} is greater than t_{RCD} (max).

tAA : from column address input when t_{RAD} is greater than t_{RAD} (max).

tOEA : from the falling edge of $\overline{OE}$ when $\overline{OE}$ is brought Low after t_{RAC} , t_{CAC} , or t_{AA} .

The data remains valid until either $\overline{LCAS}$ / $\overline{UCAS}$ or $\overline{OE}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high–impedance state during the entire cycle.

FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, $\overline{RAS}$ is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 512x16–bits can be accessed. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or ready–modify–write cycles are permitted.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) Notes 3

Paramter	Notes	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit
Output high voltage	1	V_{OH}	I_{OH} = –5 mA	2.4	—	—	V
Output low voltage	1	V_{OL}	I_{OL} = 4.2 mA	—	—	0.4	V
Input leakage current (any input)		$I_{I(L)}$	0V≤ V_{IN} ≤ 5.5V; 4.5V≤ V_{CC} ≤ 5.5V; V_{SS} = 0V; All other pins not under test = 0V	–10	—	10	µA
Output leakage current		$I_{DQ(L)}$	0V≤ V_{OUT} ≤ 5.5V; Data out disabled	–10	—	10	µA
Operating current (Average Power supply current) 2	MB814260A–70	I_{CC1}	$\overline{RAS}$ & $\overline{LCAS}$, $\overline{UCAS}$ cycling; t_{RC} = min	—	—	155	mA
	MB814260A–80					140	
	MB814260A–10					115	
Standby current (Power supply current)	TTL level	I_{CC2}	$\overline{RAS}$ = $\overline{LCAS}$, $\overline{UCAS}$ = V_{IH}	—	—	2.0	mA
	CMOS level		$\overline{RAS}$ = $\overline{LCAS}$, $\overline{UCAS}$ ≥ V_{CC} –0.2V			1.0	
Refresh current #1 (Average power supply current) 2	MB814260A–70	I_{CC3}	$\overline{LCAS}$, $\overline{UCAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min	—	—	155	mA
	MB814260A–80					140	
	MB814260A–10					115	
Fast Page Mode current 2	MB814260A–70	I_{CC4}	$\overline{RAS}$ = VIL, $\overline{LCAS}$, $\overline{UCAS}$ cycling; t_{PC} = min	—	—	80	mA
	MB814260A–80					72	
	MB814260A–10					60	
Refresh current #2 (Average power supply current) 2	MB814260A–70	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	—	155	mA
	MB814260A–80					140	
	MB814260A–10					115	

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB814260A-70		MB814260A-80		MB814260A-10		Unit
				Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	8.2	—	8.2	—	8.2	ms
2	Random Read/Write Cycle Time		t_{RC}	125	—	140	—	170	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	175	—	195	—	230	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	70	—	80	—	100	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	20	—	20	—	25	ns
6	Column Address Access Time	8,9	t_{AA}	—	35	—	40	—	45	ns
7	Output Hold Time		t_{OH}	0	—	0	—	0	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	0	—	0	—	0	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	15	—	20	—	20	ns
10	Transition Time		t_T	2	50	2	50	2	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	45	—	50	—	60	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	70	100000	80	100000	100	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	20	—	20	—	25	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	5	—	5	—	5	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	20	50	20	60	25	75	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	20	—	20	—	25	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	70	—	80	—	100	—	ns
18	$\overline{CAS}$ Precharge Time (Normal)	19	t_{CPN}	10	—	10	—	10	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	10	—	15	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	12	—	15	—	15	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	35	15	40	20	55	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	35	—	40	—	45	—	ns
25	Column Address to $\overline{CAS}$ Lead Time		t_{CAL}	35	—	40	—	45	—	ns
26	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	ns
28	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	ns
29	Write Command Set Up Time	15	t_{WCS}	0	—	0	—	0	—	ns
30	Write Command Hold Time		t_{WCH}	10	—	12	—	15	—	ns
31	$\overline{WE}$ Pulse Width		t_{WP}	10	—	12	—	15	—	ns
32	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	20	—	20	—	25	—	ns
33	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	18	—	20	—	20	—	ns
34	DIN set Up Time		t_{DS}	0	—	0	—	0	—	ns
35	DIN Hold Time		t_{DH}	10	—	12	—	15	—	ns
36	$\overline{RAS}$ to $\overline{WE}$ Delay Time		t_{RWD}	95	—	110	—	130	—	ns
37	$\overline{CAS}$ to $\overline{WE}$ Delay Time		t_{CWD}	45	—	50	—	55	—	ns
38	Column Address to $\overline{WE}$ Delay Time		t_{AWD}	60	—	70	—	75	—	ns
39	$\overline{RAS}$ Precharge time to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	0	—	0	—	0	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB814260A-70		MB814260A-80		MB814260A-10		Unit
				Min	Max	Min	Max	Min	Max	
40	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	ns
41	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CHR}	10	—	12	—	15	—	ns
42	Access Time from $\overline{OE}$	9	t_{OEA}	—	20	—	20	—	25	ns
43	Output Buffer Turn Off Delay from $\overline{OE}$	10	t_{OEZ}	—	15	—	20	—	20	ns
44	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data		t_{OEL}	10	—	10	—	10	—	ns
45	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	16	t_{OEH}	0	—	0	—	0	—	ns
46	$\overline{OE}$ to Data In Delay Time		t_{OED}	15	—	20	—	20	—	ns
47	DIN to $\overline{CAS}$ Delay Time	17	t_{DZC}	0	—	0	—	0	—	ns
48	DIN to $\overline{OE}$ Delay Time	17	t_{DZO}	0	—	0	—	0	—	ns
50	Fast Page Mode $\overline{RAS}$ Pulse width		t_{RASP}	—	200000	—	200000	—	200000	ns
51	Fast Page Mode Read/Write Cycle Time		t_{PC}	45	—	50	—	55	—	ns
52	Fast Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	93	—	105	—	110	—	ns
53	Access Time from $\overline{CAS}$ Precharge	9,18	t_{CPA}	—	40	—	45	—	50	ns
54	Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	10	—	10	—	10	—	ns
55	Fast Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge		t_{RHCP}	40	—	45	—	50	—	ns
56	Fast Page Mode $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time		t_{CPWD}	65	—	75	—	80	—	ns

Notes:

1. Referenced to VSS.
2. Icc depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   Icc depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{UCAS}$= V_{IH}, $\overline{LCAS}$= V_{IH}, V_{IL} > −0.5V.
   I_{CC1}, I_{CC3} and I_{CC5} are specified at three time of address change during $\overline{RAS}$ = V_{IL} and $\overline{UCAS}$= V_{IH}, $\overline{LCAS}$= V_{IH}.
   I_{CC4} is specified at one time of address change during one Page cycle.
3. An Initial pause ($\overline{RAS}$ = $\overline{CAS}$ =VIH) of 200µs is required after power-up followed by any eight $\overline{RAS}$ -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ -before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min) = t_{RAH} (min)+ 2t_T + t_{ASC} (min).
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.
16. Assumes that $t_{WCS} < t_{WCS}$ (min).
17. Either t_{DZC} or t_{DZO} must be satisfied.
18. t_{CPA} is access time from the selection of a new column address (that is caused by changing both $\overline{UCAS}$and $\overline{LCAS}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max).
19. Assuemes that $\overline{CAS}$ -before-$\overline{RAS}$ refresh.

Fig. 2 – t_{RAC} vs. t_{RCD}

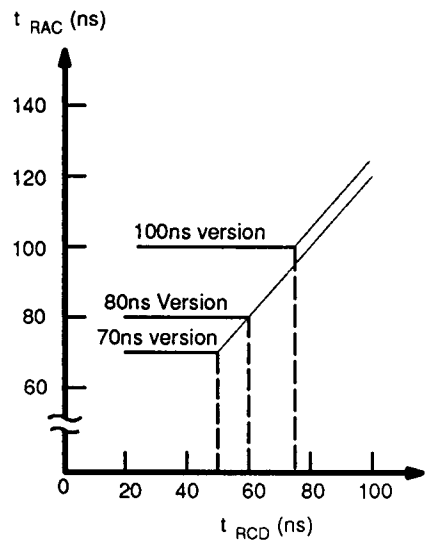


Fig. 3 – t_{RAC} vs. t_{RAD}

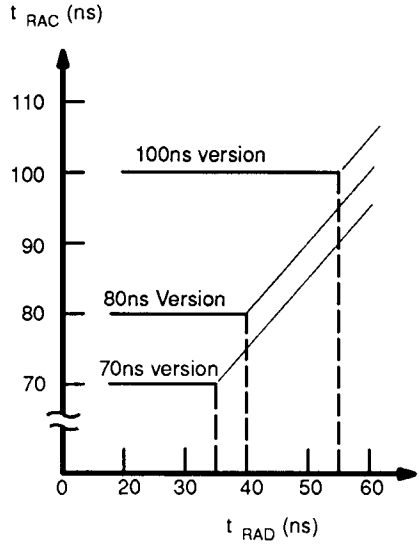
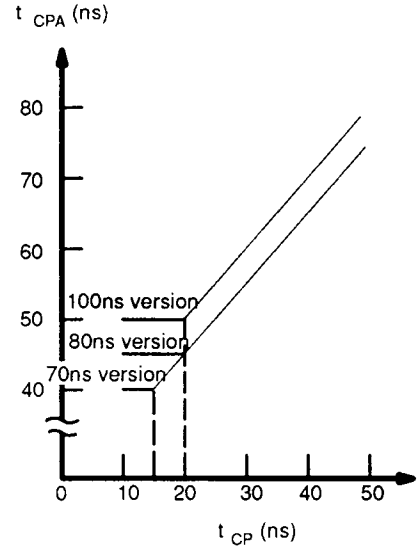


Fig. 4 – t_{CPA} vs. t_{CP}

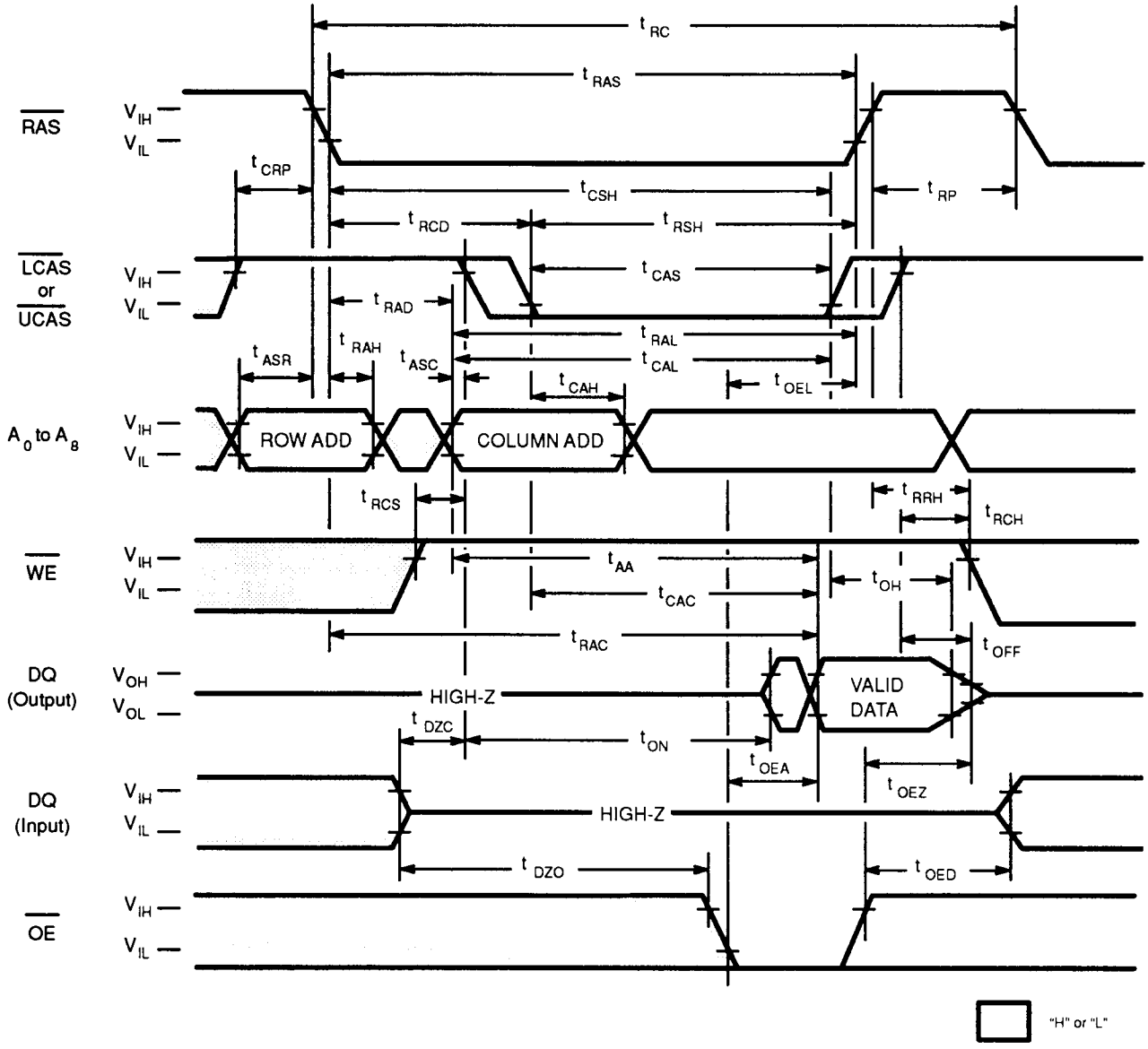


FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input					Address		Input/Output Data				Refresh	Note
								DQ1 to DQ8		DQ9 to DQ16			
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	Row	Column	Input	Output	Input	Output		
Standby	H	H	H	X	X	–	–	–	High–Z	–	High–Z	–	
Read Cycle	L	L H L	H L L	H	L	Valid	Valid	–	Valid High–Z Valid	–	High–Z Valid	Yes. *	tRCS≥ tRCS (min.)
Write Cycle (Early Write)	L	L H L	H L L	L	X	Valid	Valid	Valid – Valid	High–Z	– Valid Valid	Valid High–Z	Yes. *	tWCS≥ tWCS (min.)
Read–Modify–Write Cycle	L	L H L	H L L	H→L	L→H	Valid	Valid	Valid – Valid	Valid High–Z Valid	– Valid Valid	High–Z Valid	Yes. *	
$\overline{RAS}$–only Refresh Cycle	L	H	H	X	X	Valid	–	–	High–Z	–	Valid High–Z	Yes.	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	L	X	X	–	–	–	High–Z	–	High–Z	Yes.	tCSR≥ tCSR (min.)
Hidden Refresh Cycle	H→L	L H L	H L L	H	L	–	–	–	Valid High–Z Valid	–	High–Z Valid	Yes.	Previous data is kept.

X; "H" or "L"
*; It is impossible in Fast Page Mode

Fig. 5 – READ CYCLE



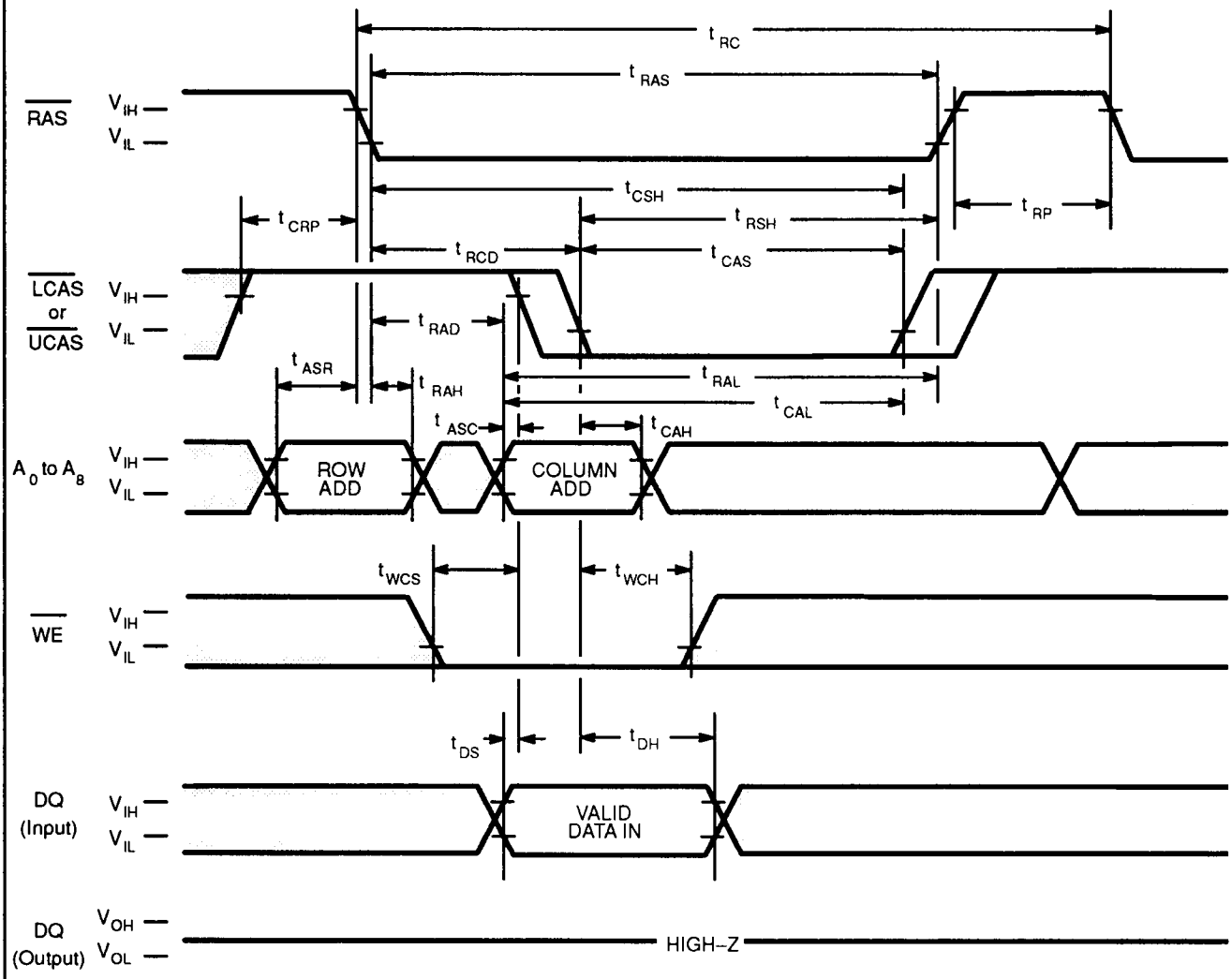
DESCRIPTION

To implement a read operation, a valid address is latched in by the $\overline{RAS}$ and $\overline{LCAS}$ or $\overline{UCAS}$ address strobes and with $\overline{WE}$ set to a High level and $\overline{OE}$ set to a low level, the output is valid once the memory access time has elapsed. $\overline{LCAS}$ controls the input/output data on DQ1–DQ8 pins, $\overline{UCAS}$ controls one on DQ8–DQ16 pins. The access time is determined by $\overline{RAS}$(tRAC), $\overline{LCAS}$/$\overline{UCAS}$ (tCAC), $\overline{OE}$ (tOEA) or column addresses (tAA) under the following conditions:

If tRCD > tRCD (max), access time = tCAC.
If tRAD > tRAD (max), access time = tAA.
If $\overline{OE}$ is brought Low after tRAC, tCAC, or tAA (which ever occurs later), access time = tOEA.

However, if either $\overline{LCAS}$/$\overline{UCAS}$ or $\overline{OE}$ goes High, the output returns to a high–impedance state after tOH is satisfied.

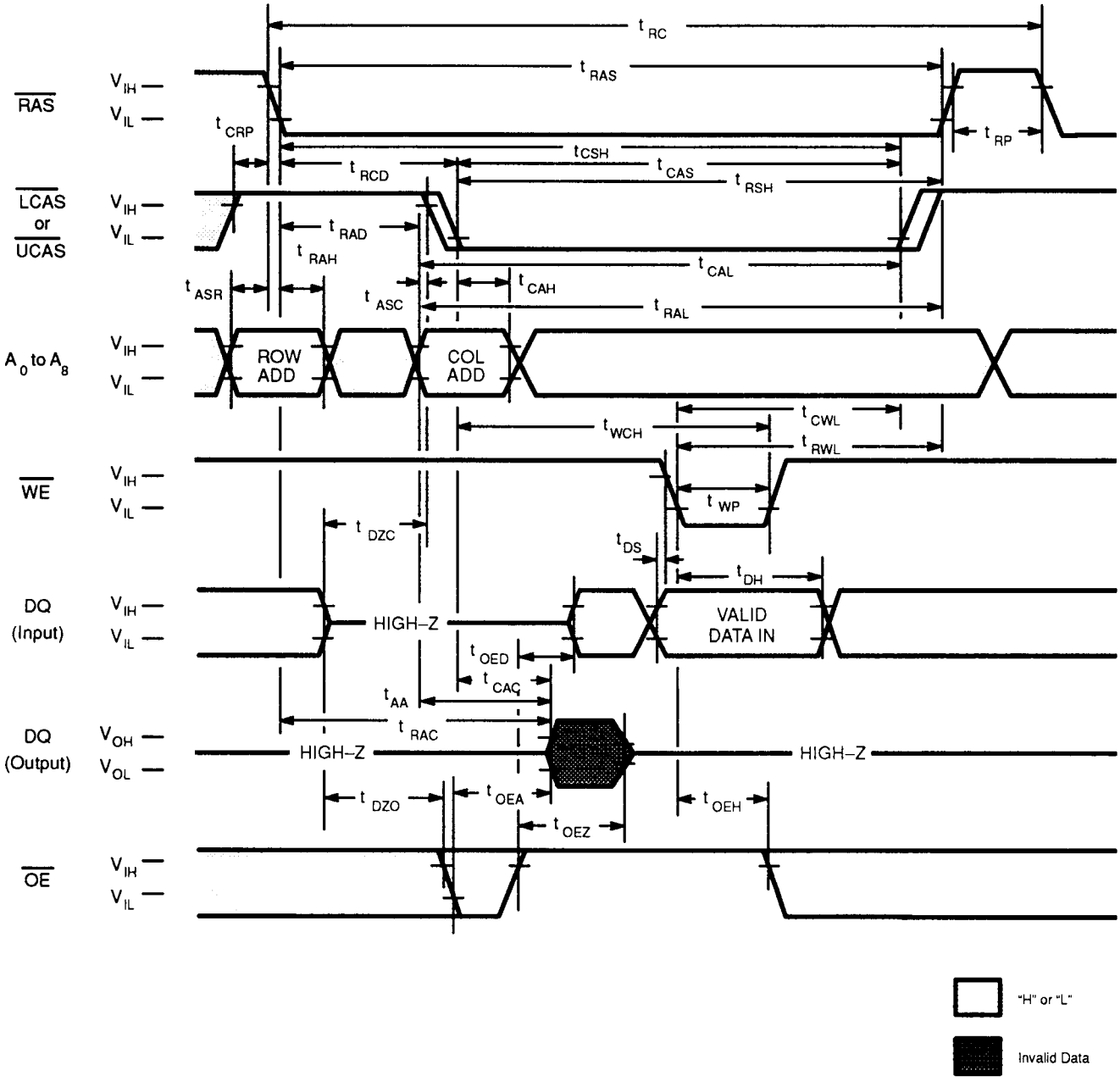
Fig. 6 – EARLY WRITE CYCLE ($\overline{OE}$ = "H" or "L")



DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is a "H" or "L" signal. A write cycle can be implemented in either of three ways – early write, OE $\overline{write}$ (delayed write), or read–modify–write. During all write cycles, timing parameters tRWL, tCWL, tRAL and tCAL must be satisfied. In the early write cycle shown above tWCS satisfied, data on the DQ pins are latched with the falling edge of $\overline{LCAS}$ or $\overline{UCAS}$ and written into memory.

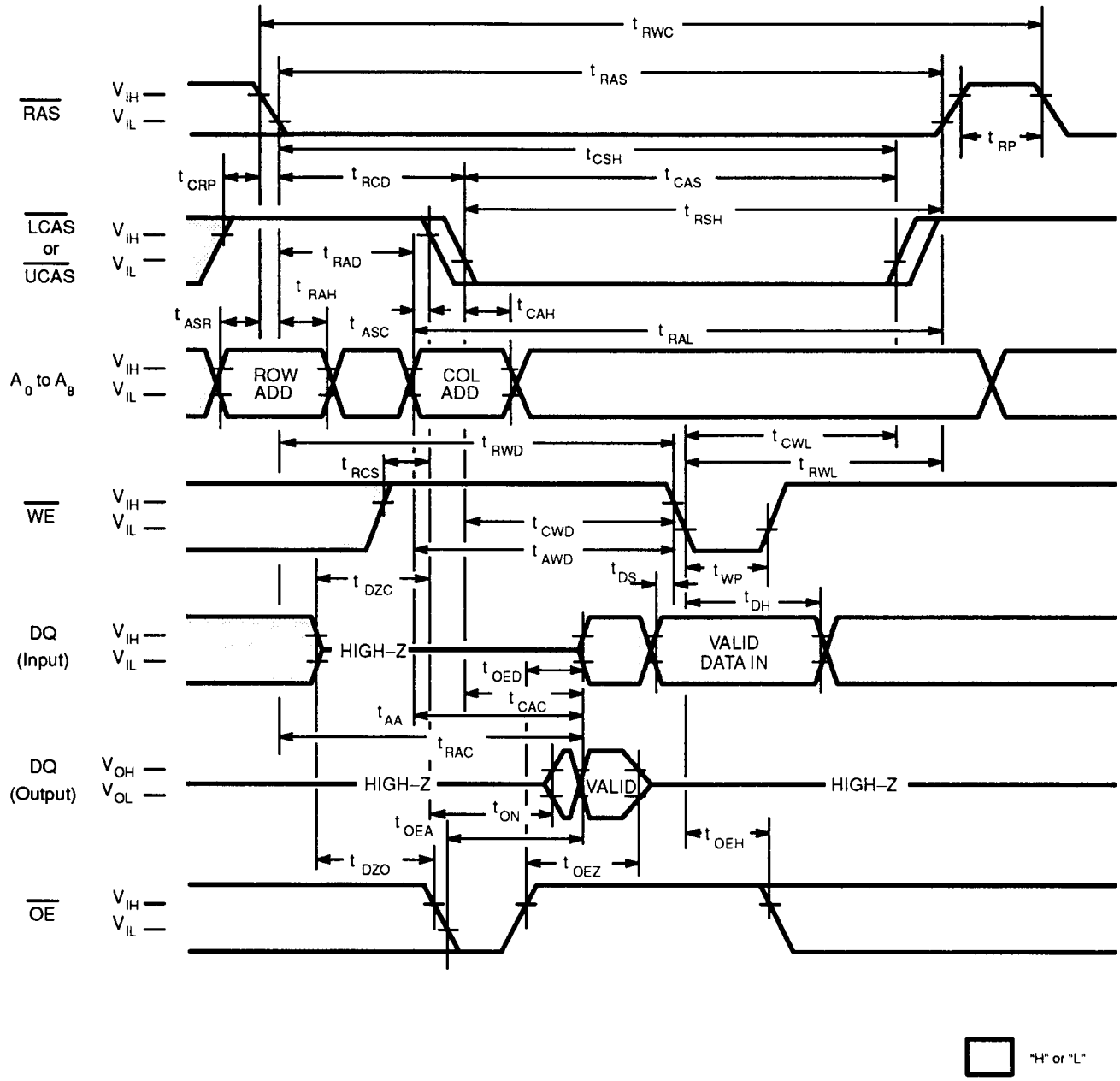
Fig. 7 – $\overline{OE}$ (DELAYED WRITE CYCLE)



DESCRIPTION

In the $\overline{OE}$ (delayed write) cycle, tWCS is not satisfied ; thus, the data on the DQ pins is latched with the falling edge of $\overline{WE}$ and written into memory. The Output Enable ($\overline{OE}$) signal must be changed from Low to High before $\overline{WE}$ goes Low (tOED+ tT + tDS).

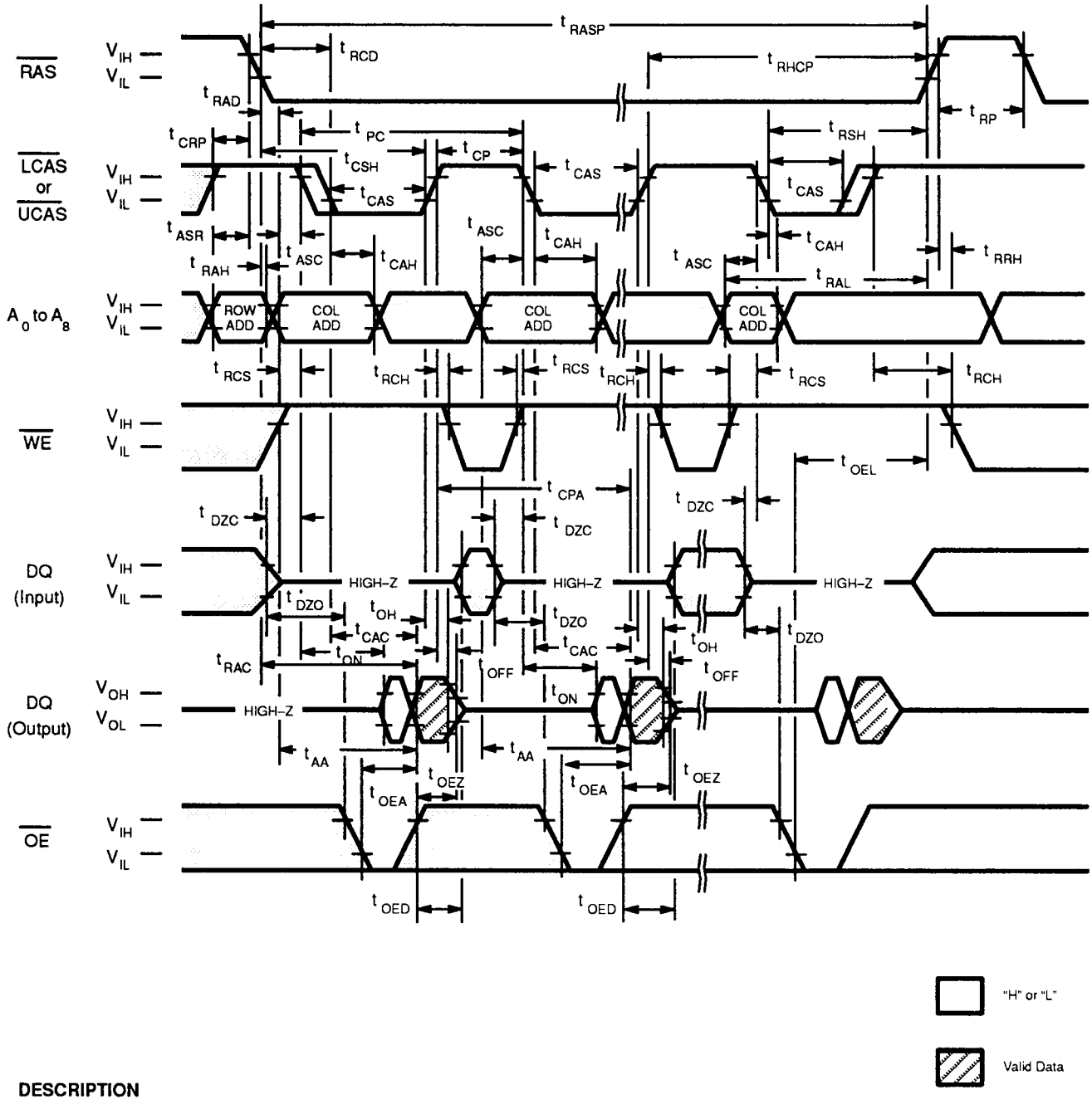
Fig. 8 – READ–MODIFY–WRITE–CYCLE



DESCRIPTION

The read–modify–write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read–modify–write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

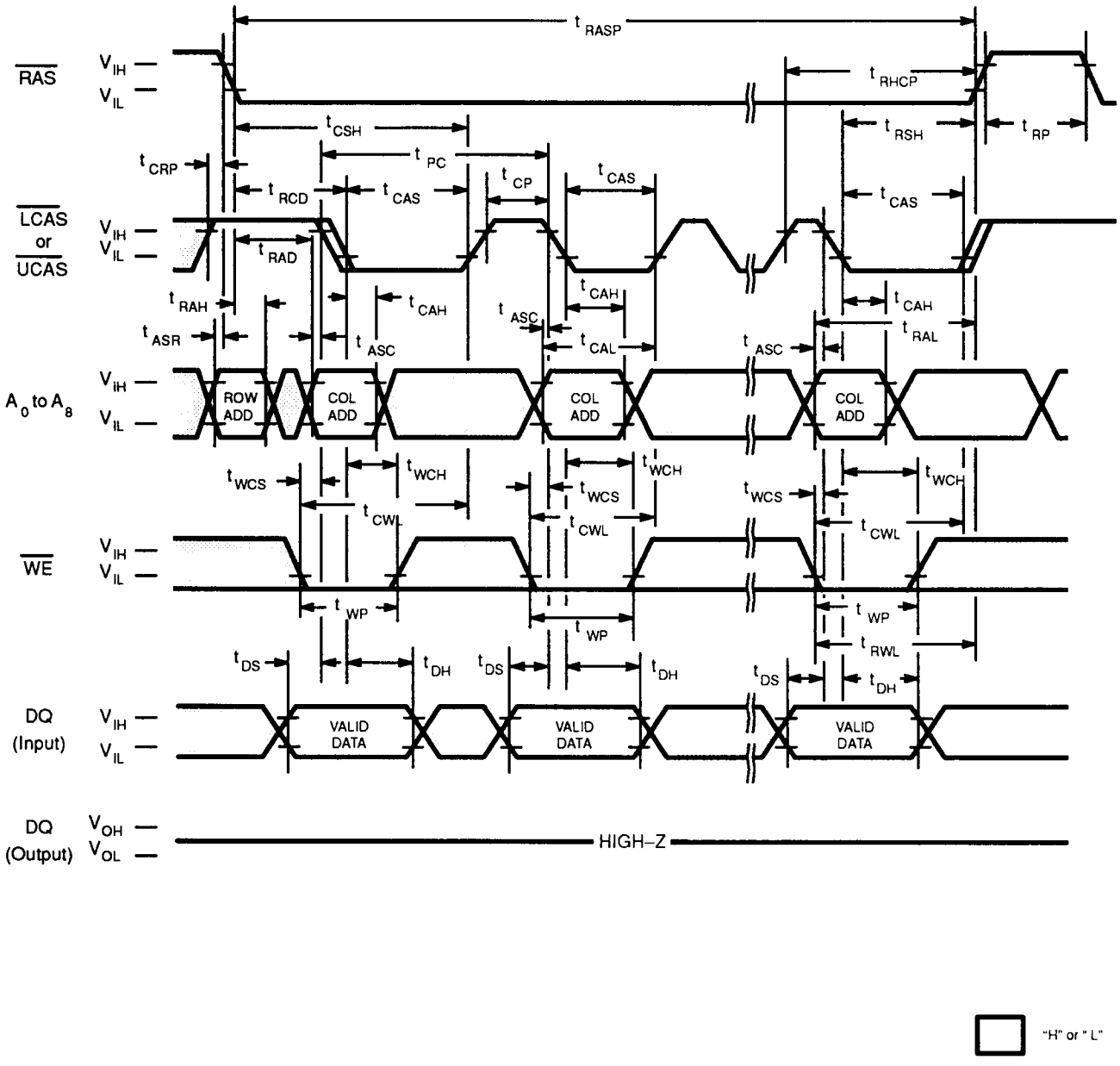
Fig. 9 – FAST PAGE MODE READ CYCLE



DESCRIPTION

The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level and $\overline{WE}$ at a High level during all successive memory cycles in which the row address is latched. The access time is determined by tCAC, tAA, tCPA, or tOEA, whichever one is the latest in occuring.

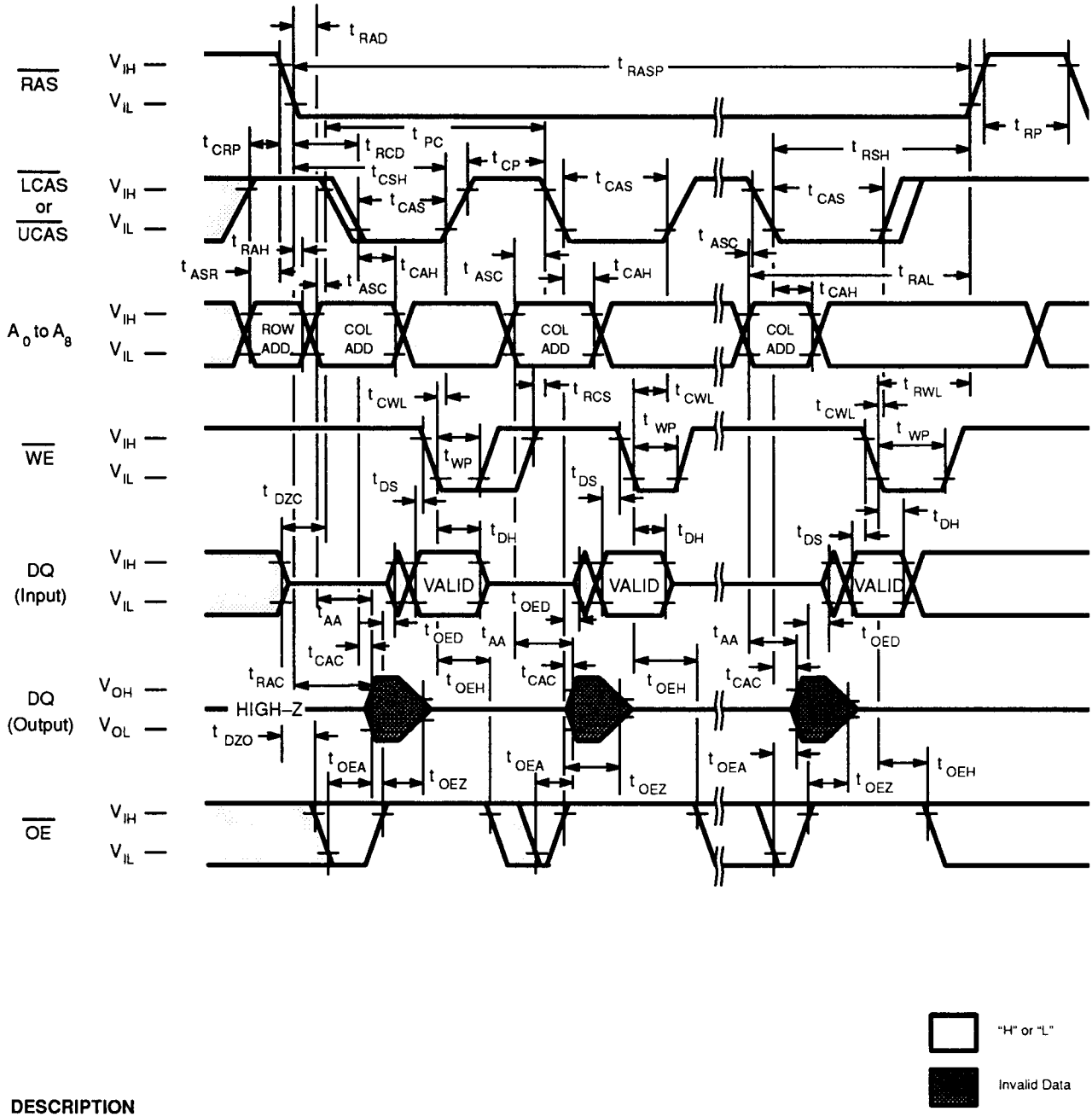
Fig. 10 – FAST PAGE MODE WRITE CYCLE ($\overline{OE}$ = "H" or "L")



DESCRIPTION

The fast page mode write cycle is executed in the same manner as the fast page mode read cycle except the states of $\overline{WE}$ and $\overline{OE}$ are reversed. Data appearing on the DQ1 to DQ8 is latched on the falling edge of $\overline{LCAS}$ and one appearing on the DQ9 to DQ16 is latched on the falling edge of $\overline{UCAS}$ and the data is written into the memory. During the fast page mode write cycle, including the delayed ($\overline{OE}$) write and read–modify–write cycles, tCWL must be satisfied.

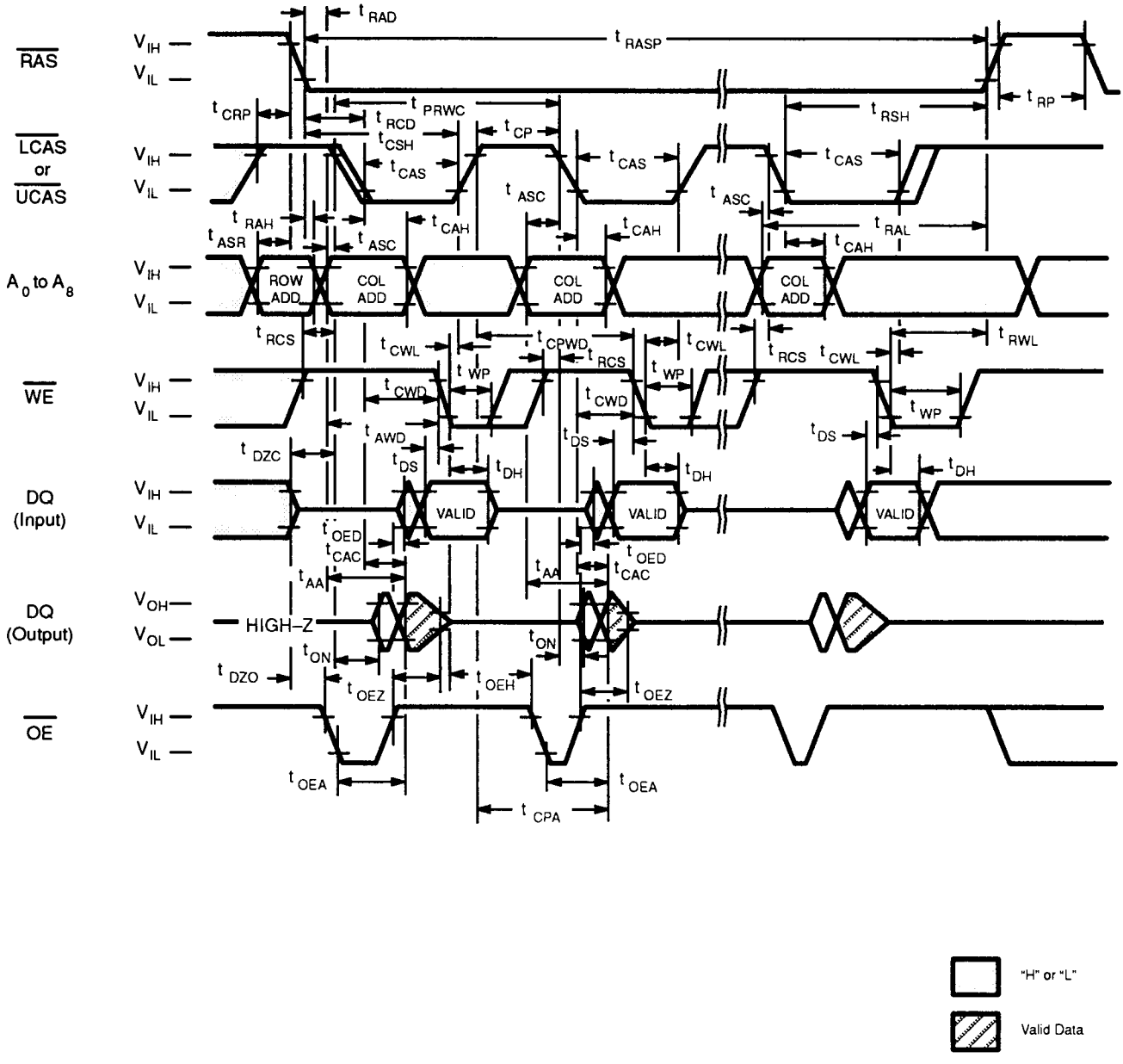
Fig. 11 – FAST PAGE MODE $\overline{OE}$ WRITE CYCLE



DESCRIPTION

The fast page mode $\overline{OE}$ (delayed) write cycle is executed in the same manner as the fast page mode write cycle except for the states of $\overline{WE}$ and $\overline{OE}$. Input data on the DQ pins are latched on the falling edge of $\overline{WE}$ and written into memory. In the fast page mode delayed write cycle, $\overline{OE}$ must be changed from Low to High before $\overline{WE}$ goes Low (tOED + tT + tDS).

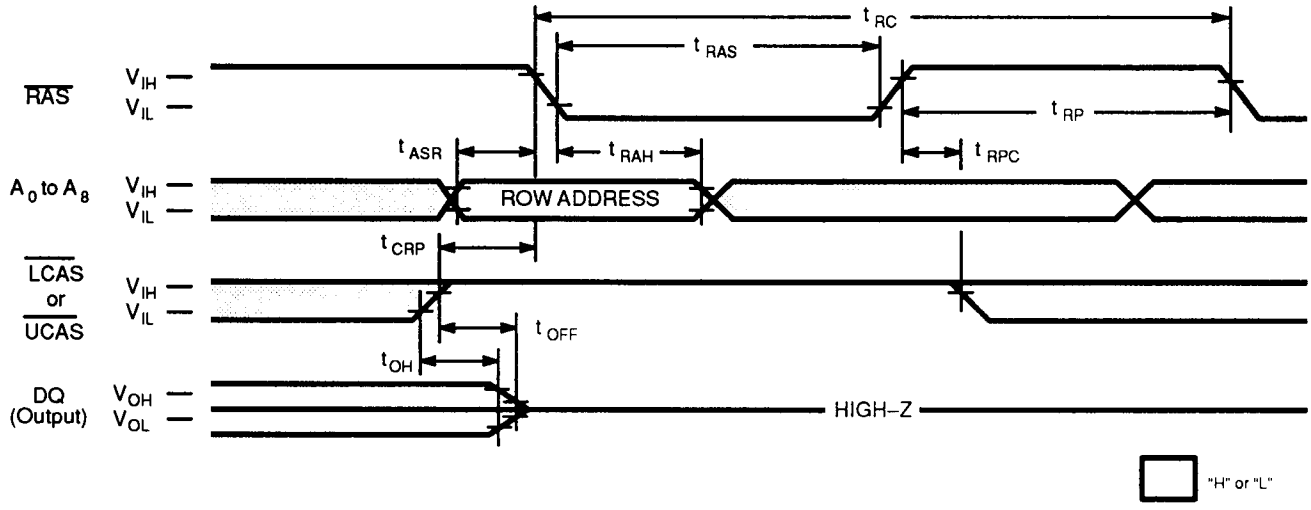
Fig. 12 – FAST PAGE MODE READ–MODIFY–WRITE CYCLE



DESCRIPTION

During fast page mode of operation, the read–modify–write cycle can be executed by switching $\overline{WE}$ from High to Low after input data appears at the DQ pins during a normal cycle.

Fig. 13 – $\overline{RAS}$–ONLY REFRESH ($\overline{WE}$ = $\overline{OE}$ = "H" or "L")

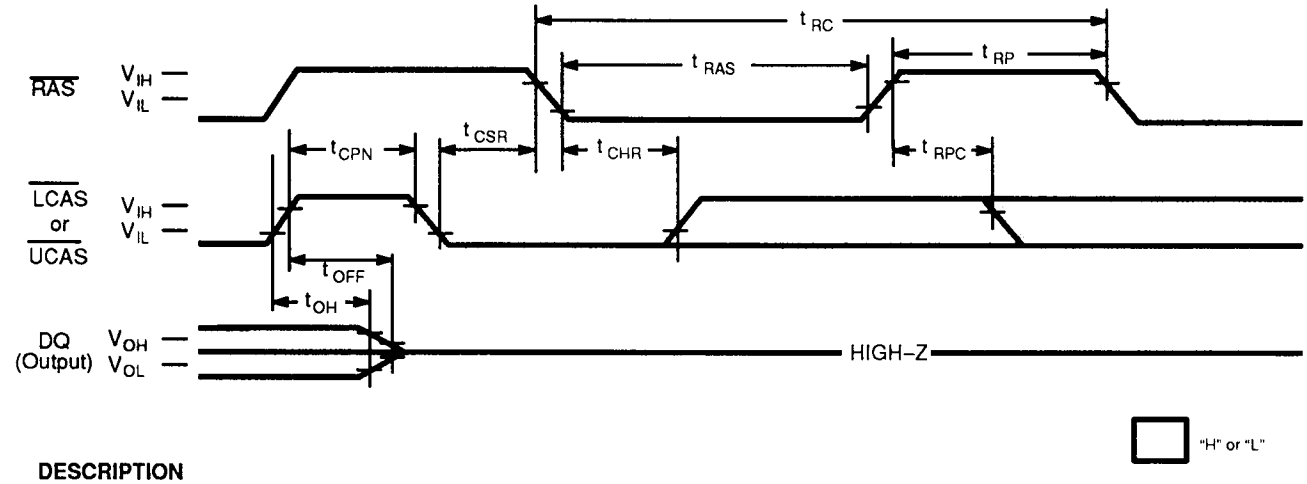


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 512 row addresses every 8.2–milliseconds. Three refresh modes are available: $\overline{RAS}$–only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$–only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{LCAS}$ and $\overline{UCAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, DQ pins are kept in a high-impedance state.

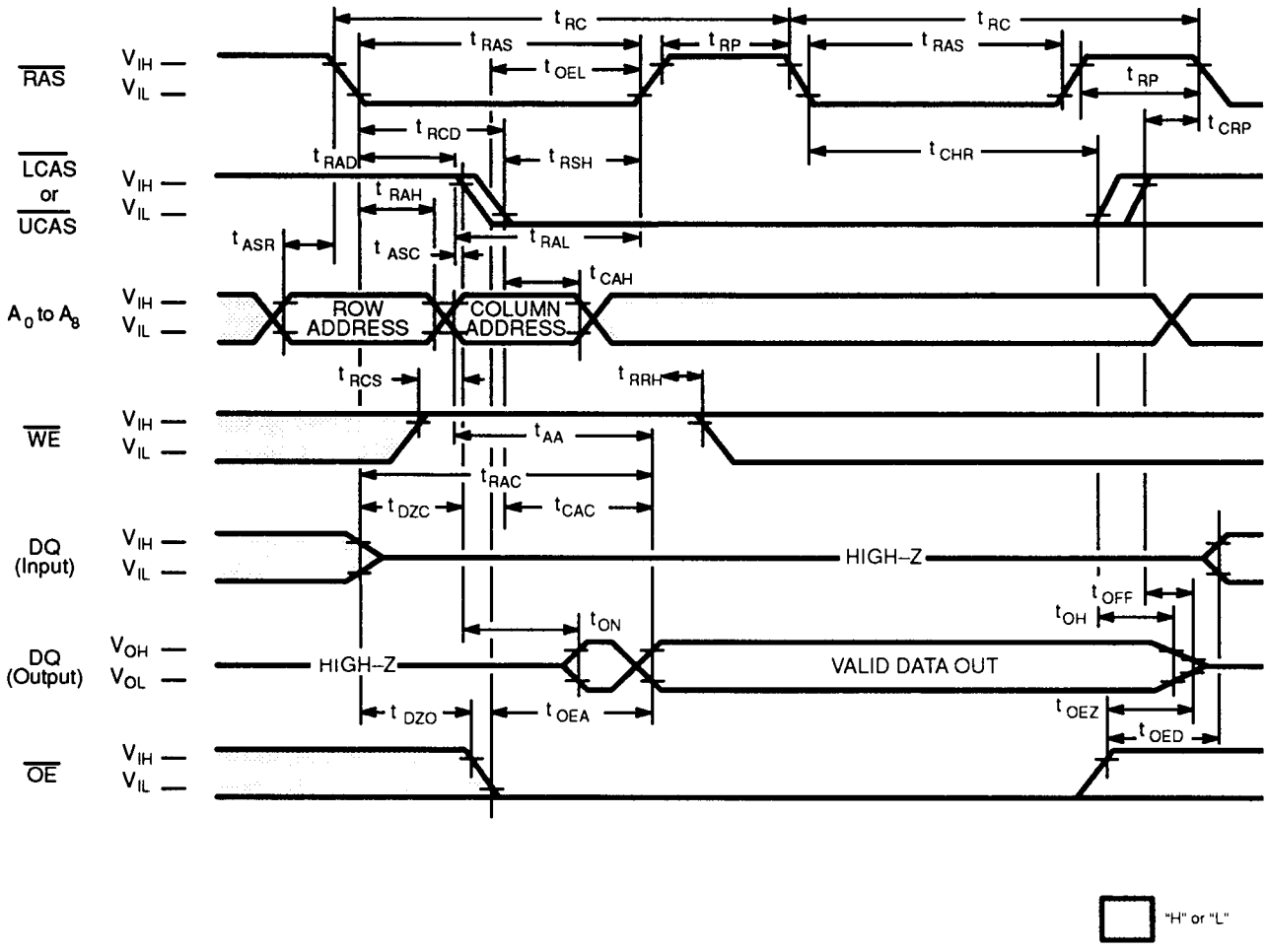
Fig. 14 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH (ADDRESSES = $\overline{WE}$ = $\overline{OE}$ = "H" or "L")



DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{LCAS}$ or $\overline{UCAS}$ is held Low for the specified setup time (t_{CSR}) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

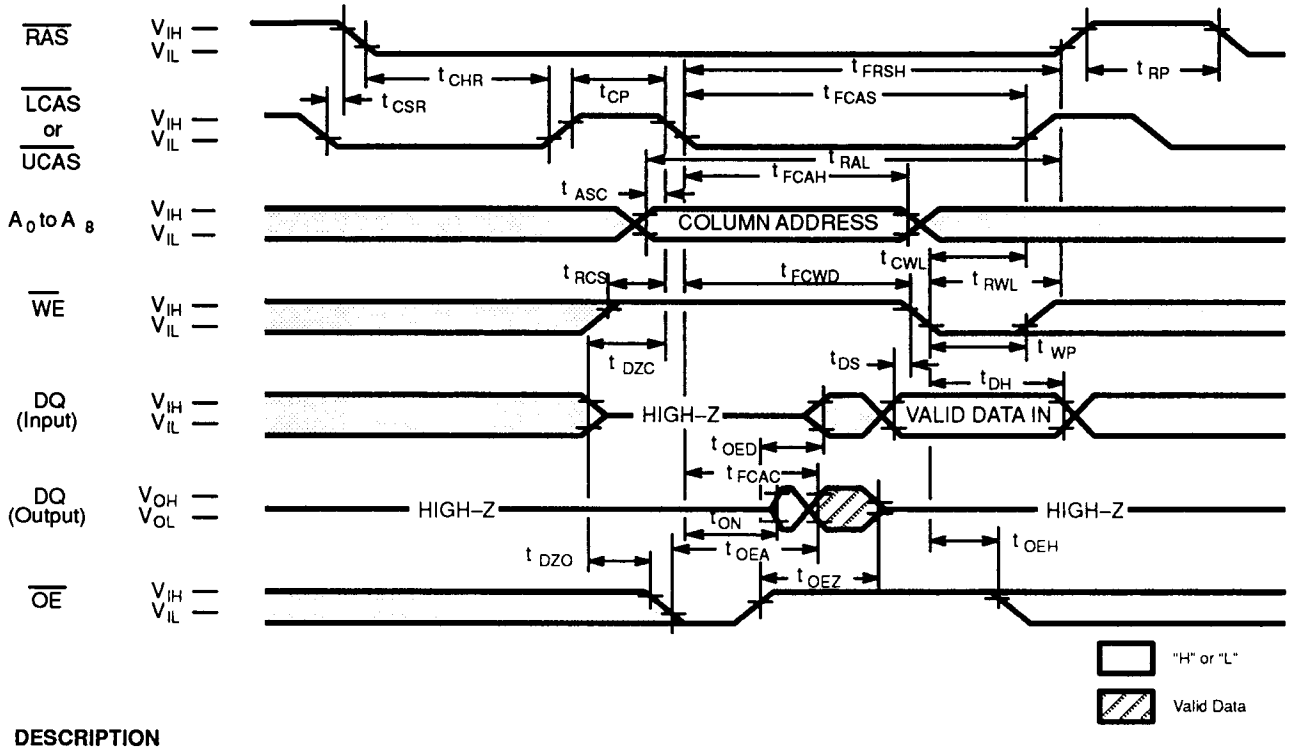
Fig. 15 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ and cycling $\overline{\text{RAS}}$. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability.

Fig. 16 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. After a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, if $\overline{LCAS}$ or $\overline{UCAS}$ makes a transition from High to Low while $\overline{RAS}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A0 through A8 are defined by the on-chip refresh counter.
Column Address: Bits A0 through A8 are defined by latching levels on A0–A8 at the second falling edge of $\overline{LCAS}$ or $\overline{UCAS}$.

The $\overline{CAS}$-before-$\overline{RAS}$ Counter Test procedure is as follows ;

1) Normalize the internal refresh address counter by using 8 $\overline{RAS}$ only refresh cycles.
2) Use the same column address throughout the test.
3) Write "0" to all 512 row addresses at the same column address by using CBR refresh counter test cycles.
4) Read "0" written in procedure 3) by using normal read cycle and check; After reading "0" and check are completed (or simultaneously), write "1" to the same addresses by using normal write cycle (or read–modify–write cycle).
5) Read and check data "1" written in procedure 4) by using CBR refresh counter test cycle for all 512 memory locations.
6) Reverse test data and repeat procedures 3), 4), and 5).

(At recommended operating conditions unless otherwise noted.)

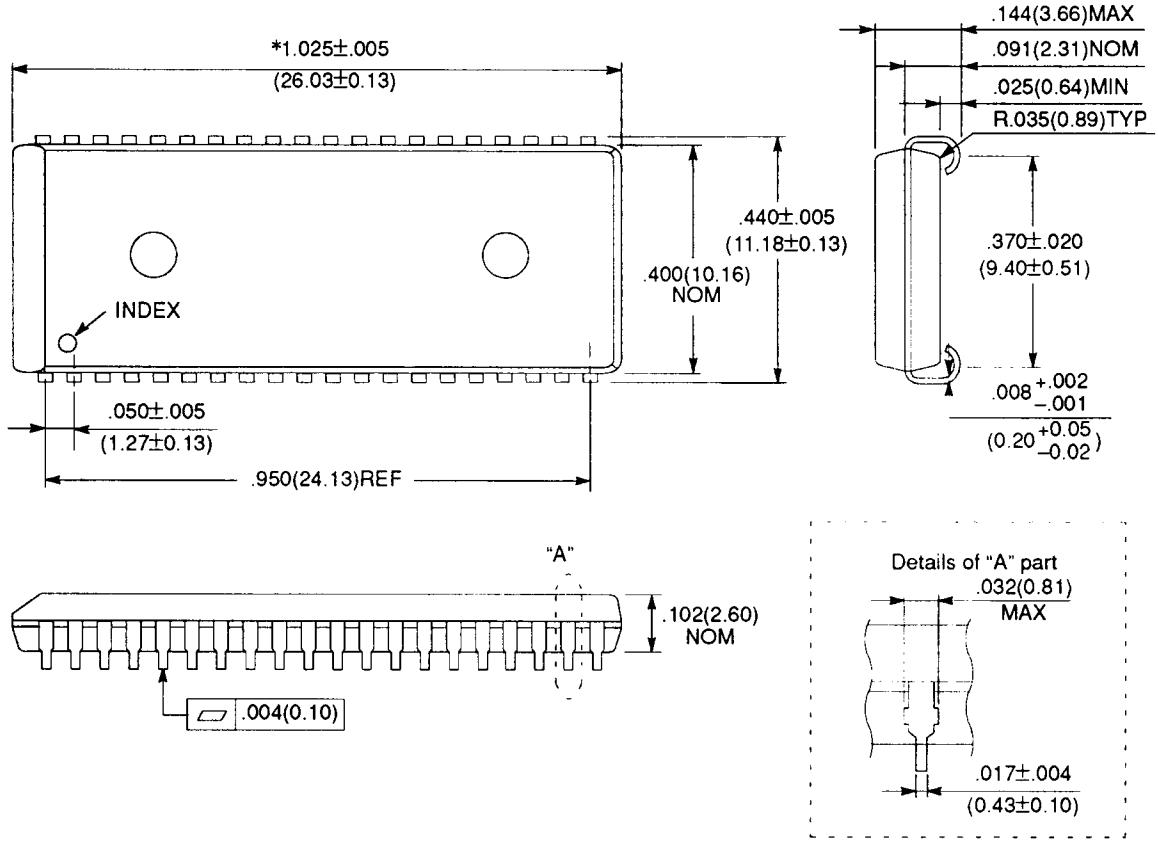
No.	Parameter	Symbol	MB814260A–70		MB814260A–80		MB814260A–10		Unit
			Min	Max	Min	Max	Min	Max	
90	Access Time from $\overline{CAS}$	t_{FCAC}	—	55	—	60	—	70	ns
91	Column Address Hold Time	t_{FCAH}	30	—	35	—	40	—	ns
92	$\overline{CAS}$ to WE Delay Time	t_{FCWD}	80	—	90	—	100	—	ns
93	$\overline{CAS}$ Pulse width	t_{FCAS}	55	—	60	—	70	—	ns
94	$\overline{RAS}$ Hold Time	t_{FRSH}	55	—	60	—	70	—	ns

Note . Assumes that $\overline{CAS}$–before–$\overline{RAS}$ refresh counter test cycle only.

PACKAGE DIMENSIONS

(Suffix : –PJ)

40-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-40P-M01)



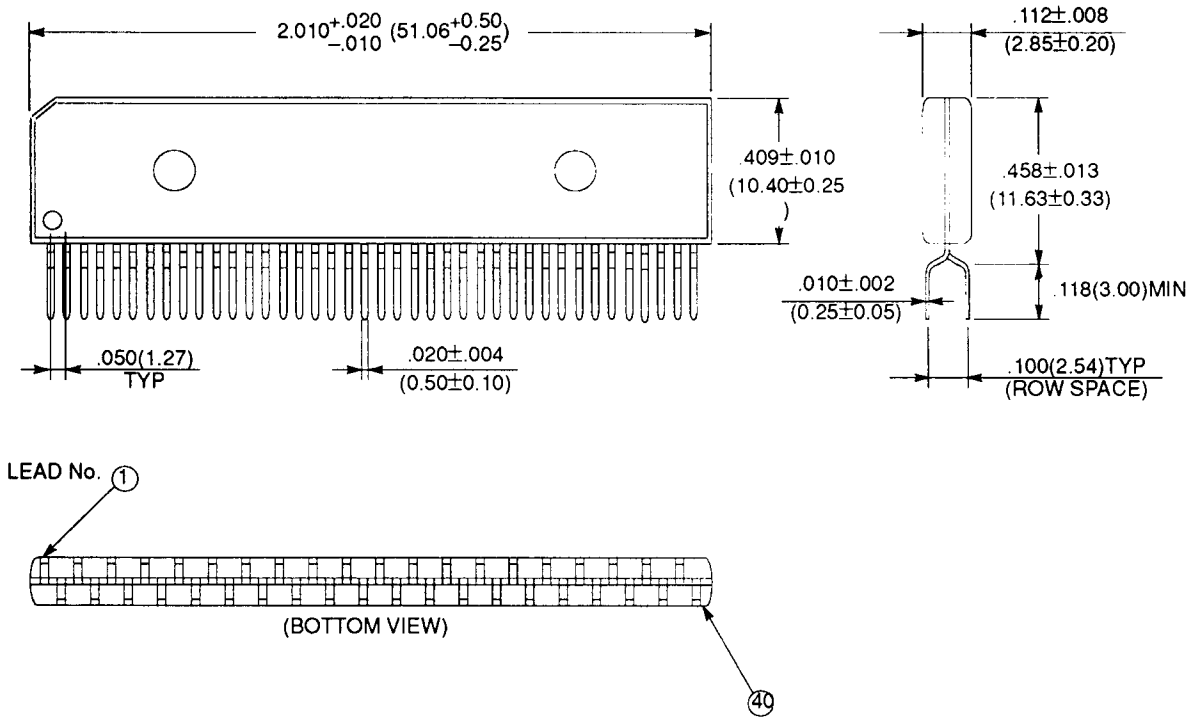
*Resin protrusion. (Each side:.006(0.15)MAX.)

Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –PZ)

40-LEAD ZIG-ZAG IN-LINE PACKAGE
(CASE No.: ZIP-40P-M01)

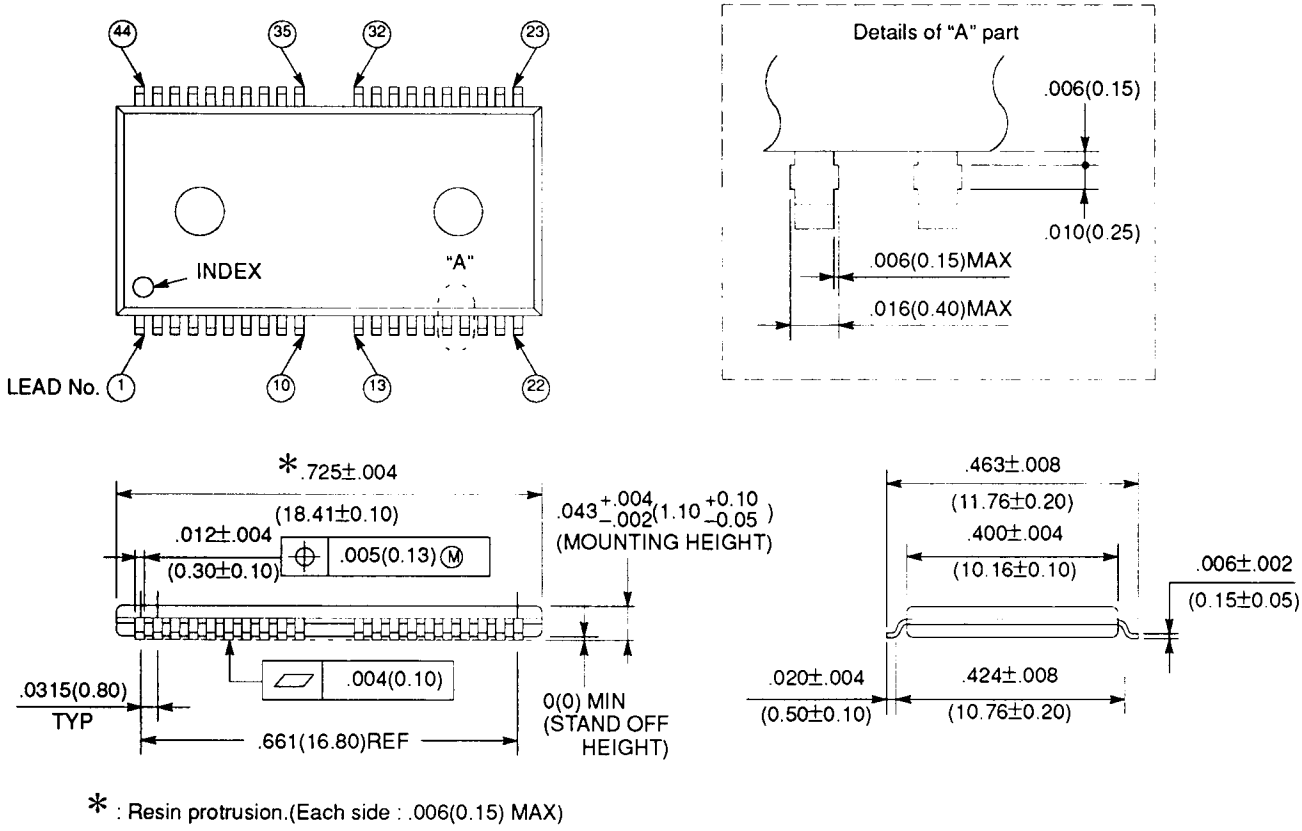


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –PFTN)

44-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-44P-M07)



* : Resin protrusion.(Each side : .006(0.15) MAX)

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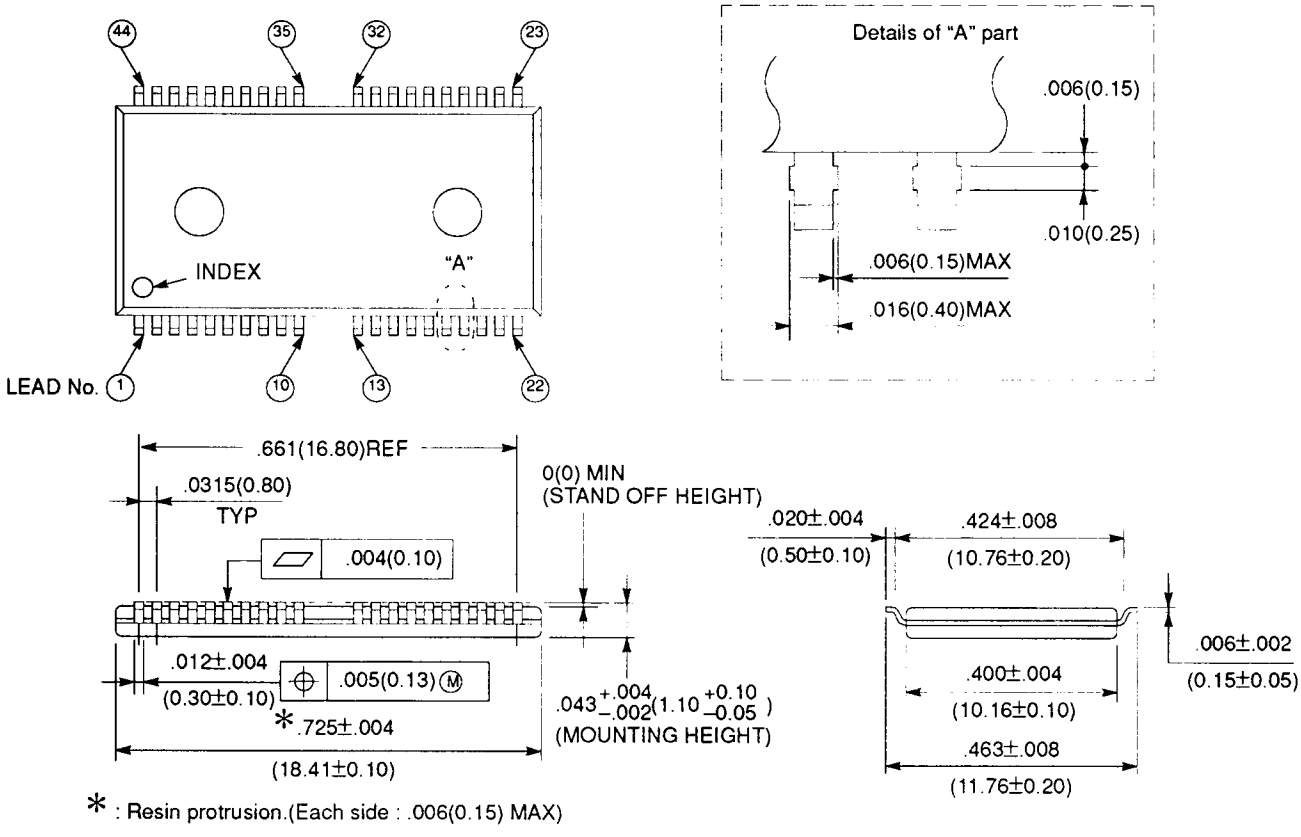
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –PFTR)

44-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-44P-M08)



* : Resin protrusion.(Each side : .006(0.15) MAX)

Dimensions in
inches (millimeters)