82593
CSMA/CD CORE LAN CONTROLLER

- **Supports Industry Standard LANs**
  - **IEEE 10BASE5 (Ethernet*)**
  - **IEEE 10BASE2 (Cheapernet)**
  - **IEEE 10BASE-T (TPE)**
- **Simple, High-Performance Control and Data Interface**
  - **Control and Status via $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ Lines**
  - **Data Transfers via DMA Interface**
  - **Two Clocks per DMA Transfer**
  - **Programmable Bus Throttle Timer**
- **High-Performance Networking Functions**
  - **Automatic Retransmission from Internal FIFO**
  - **Back-to-Back Frame Reception with No CPU Intervention**
  - **Receive Ring Buffer Memory Structure**
  - **Transmit Frame Chaining**
  - **96-Byte Transmit FIFO and 96-Byte Receive FIFO**
- **High Speed, 5V CHMOS IV (P648.8) Technology**
- **Serial Bit Rates up to 20 Mb/s (82593SX)**
  - **Direct Interface to Intel 82C501AD ESI or AMD 7992 SIA**
  - **Conforms to 802.3 CSMA/CD Standard**
- **On-Board Diagnostics**
  - **Internal and External Loopback Operation**
  - **Internal Register Dump**
  - **TDR Functionality**
- **44-Lead PLCC Package Type N (82593SX), 44-Lead QFP Package Type S (82593SX) or 28-Pin PDIP**
  - **82593SX (8/16-Bit) System Clock up to 20 MHz**
  - **82593SX Package Pin Compatible with Intel 82592 PLCC**

(See Packaging Spec., Order No. 240800-001 Package Type N, S and P)

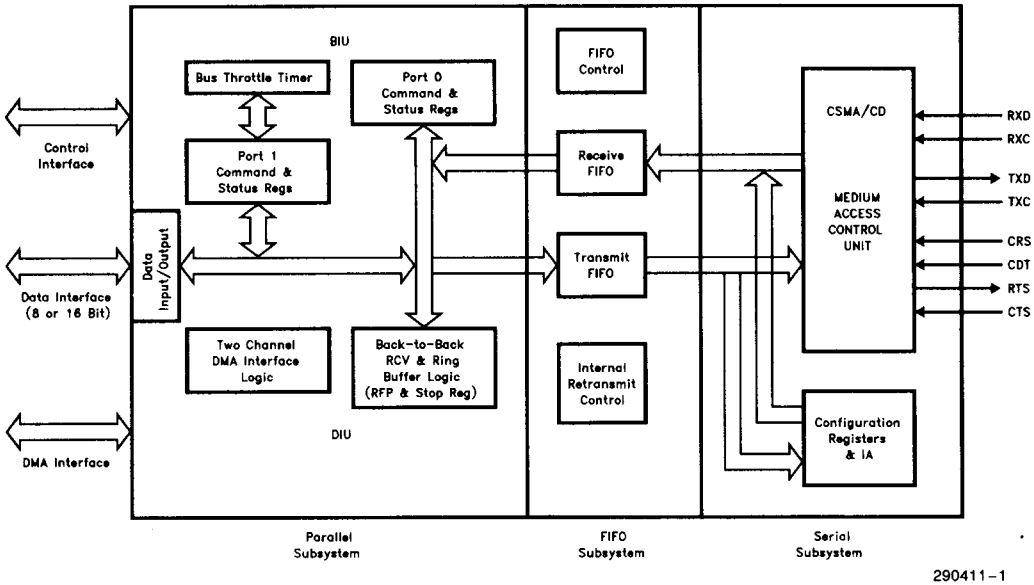

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Figure 1. 82593 Block Diagram

*Ethernet is a registered trademark of Xerox Corporation.

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Order Number: 290411-004

82593
CSMA/CD Core LAN Controller

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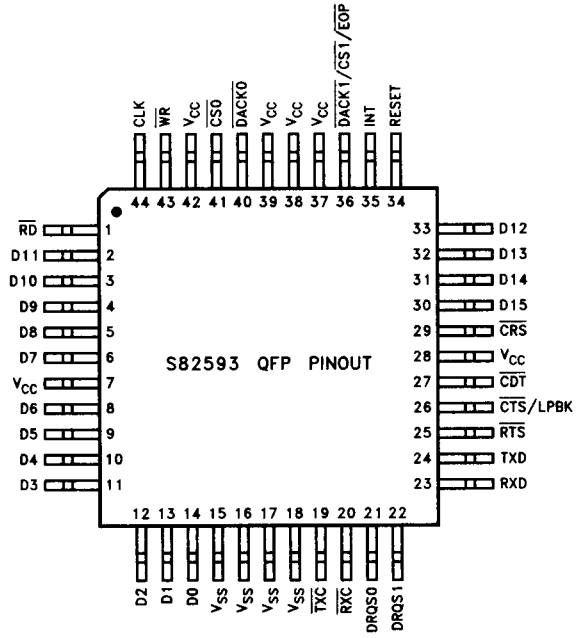
S82593 Pin Configuration



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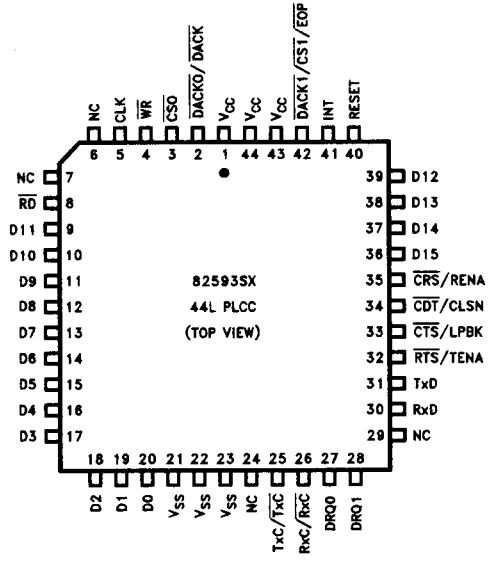
N82593SX Pin Configuration



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INTRODUCTION

The 82593 is a new generation CMOS Local Area Network controller designed for cost sensitive applications. It allows for maximum flexibility in designing and creating differentiated solutions. The 82593 features a simple, high-performance system interface which allows it to function as a CSMA/CD core for custom LAN designs. Designers can determine the performance and complexity of their solution based on the design of the logic interfaced to the 82593. This allows OEMs to develop proprietary LAN solutions that protect both their hardware and software investment into their solution. The 82593 is optimized to support IEEE 802.3 protocols such as Ethernet*, Cheapernet, and Twisted Pair Ethernet.

The 82593 contains a number of high-performance networking features that offload time-critical tasks from the CPU. The 82593 performs automatic retransmission upon collision by accessing the data for retransmission from within its 96-byte-deep transmit FIFO. This requires no intervention by the CPU as well as no need to reset the transmit DMA channel. For frame reception, the 82593, along with industry standard DMA controllers (e.g., 8237, 82380/370, etc.) or buses (ISA, EISA, etc.), implements a recyclable ring buffer structure. This structure allows reception of back-to-back receive frames without the need for CPU processing of each frame. These features also allow the 82593 to operate in embedded control applications when interfaced to embedded processors such as the Intel 80C186 and 80C188.

The 82593 is fully compatible with the IEEE 802.3 standard. When used with the Intel 82C501AD ESI it provides a complete CMOS Ethernet solution. When used with the Intel 82C501AD and 82506TB, or 82503 it provides a complete CMOS Twisted Pair Ethernet (TPE) solution.

The 82593 is compatible with the 82590 and 82592 LAN Controllers (*) operating in High Speed mode (Mode 1). The 82593SX is packaged in a 28-pin PDIP package, and is the 8-bit version of this device. The 82593SX comes in a 44-lead PLCC package, and in a 44-lead QFP package, both can be configured to have an 8- or 16-bit data bus. The 82593SX is pin compatible with the 82590. It runs at speeds up to 16 MHz for both the parallel and serial subsystems. The 82593SX in PLCC package is pin compatible with the 82592 PLCC package, with both the parallel and serial interface running at speeds up to 20 MHz. The 82593 is fabricated with Intel's reliable CHMOS IV technology.

*In this document, the 82590 and 82592 are generically referred to as the 82590 unless otherwise specified.

PIN DESCRIPTIONS

Table 1. Pin Description

Symbol	Pin No. 82593SX PLCC	Pin No. 82593SX QFP	Type	Name and Function
D15	36	30	I/O	**DATA BUS:** The Data Bus lines are bidirectional, three-state lines connected to the CPU's Data Bus for transfers of data, commands, status, and parameters. The 82593SX has an 8- or 16-bit data bus.
D14	37	31		
D13	38	32		
D12	39	33		
D11	9	2		
D10	10	3		
D9	11	4		
D8	12	5		
D7	13	6		
D6	14	8		
D5	15	9		
D4	16	10		
D3	17	11		
D2	18	12		
D1	19	13		
D0	20	14		

Table 1. Pin Description (Continued)

Symbol	Pin No. 82593SX PLCC	Pin No. 82593SX QFP	Type	Name and Function
$\overline{RD}$	8	1	I	**READ:** Together with $\overline{CS0}$, $\overline{CS1}$, $\overline{DACK0}$, or $\overline{DACK1}$, Read controls data or status transfers out of the 82593.
$\overline{WR}$	4	43	I	**WRITE:** Together with $\overline{CS0}$, $\overline{CS1}$, $\overline{DACK0}$, or $\overline{DACK1}$, Write controls data or command transfers into the 82593.
$\overline{CS0}$	3	41	I	**CHIP SELECT (PORT 0):** When LOW, the 82593 is selected by the CPU for command or status transfer through PORT 0.
RESET	40	34	I	**RESET:** A HIGH signal on this pin causes the 82593 to terminate current activity. This signal is internally synchronized and must be held HIGH for at least four Clock (CLK) cycles. The system should allow a minimum of 50 μs after the delta between V_{CC} and V_{SS} has reached at least 2.4V and CLK has reached minimum V_{IL}/V_{IH} levels.
INT	41	35	O	**INTERRUPT:** A HIGH signal on this pin notifies the CPU that the 82593 is requesting an interrupt.
DRQ0	27	21	O	**DMA REQUEST (CHANNEL 0):** This pin is used by the 82593 to request DMA transfers. DRQ0 remains HIGH as long as the 82593 requires DMA transfers. Burst transfers are thus possible. When the 82593 is programmed for Continuous Mode with TCI signaling the 82593 notifies the DMA controller of the status of transmission or reception, using this pin together with $\overline{EOP}$.
DRQ1	28	22	O	**DMA REQUEST (CHANNEL 1):** This pin is used by the 82593 to request DMA transfer. DRQ1 remains HIGH as long as the 82593 requires DMA transfers. Burst transfers are thus possible. When the 82593 is programmed for Continuous Mode with TCI signaling the 82593 notifies the DMA controller of the status of transmission or reception, using this pin together with $\overline{EOP}$.
$\overline{DACK0}$/ $\overline{DACK}$	2	40	I	**DMA ACKNOWLEDGE (CHANNEL 0):** When LOW, this input signal from the DMA controller notifies the 82593 that the requested DMA cycle is in progress. This signal acts similarly to Chip Select for data and parameter transfers, using DMA channel 0. **DMA ACKNOWLEDGE (CHANNELS 0 AND 1):** When the $\overline{DACK1}/\overline{CS1}/\overline{EOP}$ pin is programmed to $\overline{CS1}/\overline{EOP}$, this pin provides a DMA acknowledge for both channels 0 and 1. Two DMA acknowledge signals from the DMA controller, $\overline{DACK0}$ and $\overline{DACK1}$, must be externally ANDed in this mode of operation.

Table 1. Pin Description (Continued)

Symbol	Pin No. 82593SX PLCC	Pin No. 82593SX QFP	Type	Name and Function
$\overline{DACK1}$ $\overline{CS1}/\overline{EOP}$	42	36	I	This is a multifunction, bidirectional pin which can be programmed to $\overline{DACK1}$ or $\overline{CS1}/\overline{EOP}$ during configuration. When it is configured for $\overline{EOP}$, it provides an open-drain output. **DMA ACKNOWLEDGE (CHANNEL 1):** When LOW, this input signal from the DMA controller notifies the 82593 that the requested DMA cycle is in progress. This signal acts similarly to Chip Select for data and parameter transfers, using DMA channel 1.
			I/O	**CHIP SELECT (PORT 1):** When LOW, the 82593 is selected by the CPU for command or status transfer through PORT 1. **END OF PROCESS:** A LOW output signal requests the DMA controller to terminate the active DMA service.
CLK	5	44	I	**CLOCK:** A TTL-compatible clock input to this pin provides the timing for the 82593 parallel subsystem.
$\overline{TXC}$/ TXC	25	19	I	**TRANSMIT CLOCK:** This input provides the fundamental timing for the serial subsystem. This clock is also used to transmit data synchronously on the TXD pin. The polarity of this pin is programmable. Data is transferred to the TXD pin on the High to Low transition of the Transmit Clock.
$\overline{RXC}$/ RXC	26	20	I	**RECEIVE CLOCK:** This input used to synchronously sample data on the RXD pin. The polarity of this pin is programmable. The state of the RXD pin is sampled on the High to Low transition of the Receive Clock.
$\overline{CRS}$/ RENA	35	29	I	**CARRIER SENSE/RECEIVE ENABLE:** This pin is used to notify the 82593 that the serial link is active. The polarity and timings of this input are programmable.
$\overline{CDT}$/ CLSN	34	27	I	**COLLISION DETECT:** This input notifies the 82593 that a collision has occurred. The polarity and timings of this input are programmable.
RxD	30	23	I	**RECEIVE DATA:** This pin receives serial data. It must be HIGH when not receiving.
TxD	31	24	O	**TRANSMIT DATA:** This pin transmits data to the serial link. It is HIGH when not transmitting.
$\overline{RTS}$/ TENA	32	25	O	**REQUEST TO SEND/TRANSMIT ENABLE:** When this signal is active, the 82593 notifies the serial interface device that it has data to transmit. The polarity of this pin is programmable. It is tri-state on power-up until the first configuration is performed. A pull-up or pull-down resistor should be connected to this pin to guarantee it is at an inactive level prior to the initial configuration.

Table 1. Pin Description (Continued)

Symbol	Pin No. 82593SX PLCC	Pin No. 82593SX QFP	Type	Name and Function
$\overline{CTS}$/ LPBK	33	26	I/O	This pin's polarity is programmable. When CTS is active high, $\overline{LPBK}$ is active low. Conversely, when $\overline{CTS}$ is active low, LPBK is active high.
CTS/ $\overline{LPBK}$				**CLEAR TO SEND:** This signal enables the 82593 transmitter. Deasserting this signal stops the transmission.
				LOOPBACK: This pin, in conjunction with a pull-down or pull-up resistor, can be programmed to provide a loopback signal to the serial interface device.
V_{CC}	1 43 44	7, 28, 37, 38, 39, 42		**POWER:** +5V ±10%.
V_{SS}	21 22 23	15, 16, 17, 18		**GROUND:** 0V.

INTERNAL ARCHITECTURE

The 82593 consists of a parallel subsystem, a serial subsystem, and a FIFO subsystem (see Figure 1).

PARALLEL SUBSYSTEM

The parallel subsystem consists of a bus interface unit (BIU), through which commands can be written and status registers can be read by the CPU, a DMA interface unit (DIU) through which configuration parameters and data can be written and read from memory and a 10-bit bus throttle timer.

The BIU is composed of two I/O ports, Port 0 through which time-critical tasks and configurations are executed and Port 1, which is used for auxiliary commands. The 8-bit Port 0 command and status registers are interfaced to the CPU via the data lines D0–D7. Operation and initialization commands such as TRANSMIT, RCV-ENABLE, and CONFIGURE are issued to the 82593 via the Port 0 Command Register. The resultant status of these commands, as well as the states (Idle, Active, Ready, etc.) of the 82593's RCV and EXEC units are contained in the Port 0 Status Registers.

Port 1 command and status registers are also 8 bits wide. The Port 1 Command Register is used for additional commands such as POWER-DOWN and STOP-REG-UPDATE. The Port 1 status registers, Status Bank 1, contain the values of the Bus Throttle Timer, the RCV Stop Register and the Power Down and Hi-Impedance status.

The DIU is composed of two separate DMA channels, Channel 0 and Channel 1. The DMA channels are 8 bits wide for the 82593SX, and 8 or 16 bits wide for the 82593SX depending on its configuration. When the 82593SX is reset, the DMA channels are initialized for an 8-bit data path. The CPU can then configure the 82593SX for a 16-bit data path if desired. Once the 82593SX is configured for a 16-bit data path, all subsequent DMA transfers are performed on the data lines D0–D15. The two DMA channels are independent of each other. Both channels can request DMA service simultaneously for operations such as transmission and reception.

Dedicated logic in the DIU enables back-to-back transmission and reception when configured to Continuous Mode. This means that continuous transmissions and receptions can be handled by the 82593 without real time intervention of the CPU. In this mode, the DRQ and $\overline{EOP}$ pins can be used to discriminate between successful and unsuccessful operations.

The Bus Throttle Timer controls the maximum amount of time the 82593 can actively hold the bus (via the DMA controller) during a DMA cycle. This feature is programmable during configuration. The timer is started at the beginning of the first DMA cycle in a DMA burst ($\overline{DACK}$ and $\overline{RD}$ or $\overline{WR}$ active). It stops and is reset upon the $\overline{DACK}$ signal going inactive (the end of the DMA burst). If the timer expires, and the 82593 is still requesting DMA service, the 82593 will deassert its DMA request (DRQ0 or DRQ1) on the next DMA cycle, ending the DMA burst and releasing the bus. The 82593 will then reassert its DMA request after a minimum of two 82593 CLK period to complete the necessary DMA transfers.

SERIAL SUBSYSTEM

The 82593's Serial Subsystem is highly flexible in implementing the CSMA/CD protocol. It can operate in a variety of IEEE 802.3 and other CSMA/CD LAN environments, including 10BASE5 (Ethernet), 10BASE2 (Cheapernet), 10BASE-T (Twisted Pair Ethernet), 10BASE-F (Fiber Optic Ethernet), and 1BASE5 (StarLAN). The 82593 can be configured to interface directly with the Intel 82C501AD Ethernet Serial Interface device or to the AMD SIA device. Unlike the 82590, the 82593 does not provide encoding/decoding mechanisms for Manchester and NRZI (82590 High Integration Mode).

The programmable parameters include:

- Address Field Length
- Station Priority (Linear and Exponential Priority)
- Interframe Spacing
- Slot Time
- CRC-32 or CRC-16
- Preamble Length

The CSMA/CD unit is capable of running at speeds from dc to 20 Mb/s for the 82593SX, and dc to 16 Mb/s for the 82593SX.

The 82593 detects a collision when an active signal is driven on its $\overline{CDT}$/CLSN input. This signal is usually driven from the serial interface device (for example the Intel 82C501AD). It detects a carrier on the link when an active signal is driven on its $\overline{CRS}$/RENA input. The 82593 can be configured to filter the collision or carrier sense signal so that it must be active for at least 1 to 7 TXC periods before it is recognized.

FIFO SUBSYSTEM

The FIFO subsystem is located between the parallel subsystem and the serial subsystem. It consists of a 96-byte XMT FIFO, a 96-byte RCV FIFO, and FIFO control logic. The XMT and RCV FIFOs are independent, and individually provide an interface between the parallel and serial subsystems which may be running from different clock sources.

When configured to its 82590 compatible mode, the 82593 FIFO length defaults to 32 bytes for both the RCV and XMT FIFO, and the FIFO threshold (the level where a DMA request is asserted or deasserted) is fixed at 16 bytes. In all other configurations, the FIFO length is 96 bytes, with the FIFO threshold programmable through configuration. The 82593 can also be configured to delay the start of transmission until the programmed XMT FIFO threshold has been reached.

Expansion of the XMT FIFO to 96 bytes allows the 82593 to perform automatic transmission from within the XMT FIFO when a collision occurs during transmission.

PROGRAMMING MODEL—REGISTER OVERVIEW

Port 0

Figure 2 shows the 82593 Port 0 Command Register. Figure 3 shows the Port 0 commands. Port 0 is accessed when $\overline{CS0}$ is asserted, along with the assertion of the $\overline{RD}$ or $\overline{WR}$ signal. However, if the SWIT-TO-PORT-1 command is issued to the 82593, Port 1 will become the active port, even though $\overline{CS0}$ is asserted. To return to Port 0, the SWIT-TO-PORT-0 command is executed. Port switching should be used when the hardware does not support the second chip select line, $\overline{CS1}$. Port switching is disabled when hardware accesses to Port 1 via $\overline{CS1}$ are enabled.

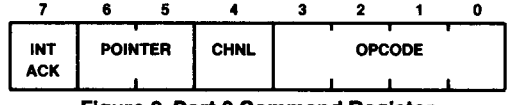


Figure 2. Port 0 Command Register

The 82593 can be configured to have 4 or 6 bytes of status registers in Port 0 (see Figures 5, 6, and 7). For the 4-byte status configuration, the first three registers (STATUS 0 through 2) contain the information about the last command executed, or the last frame received. The last status register, STATUS 3, contains the state of the 82593 Execution and Receive units. When the 82593 is configured to 6 bytes of status registers, the two additional bytes of status are used to report a more complete status of the most recently received frame, and also transmit chaining status (Continuous mode only).

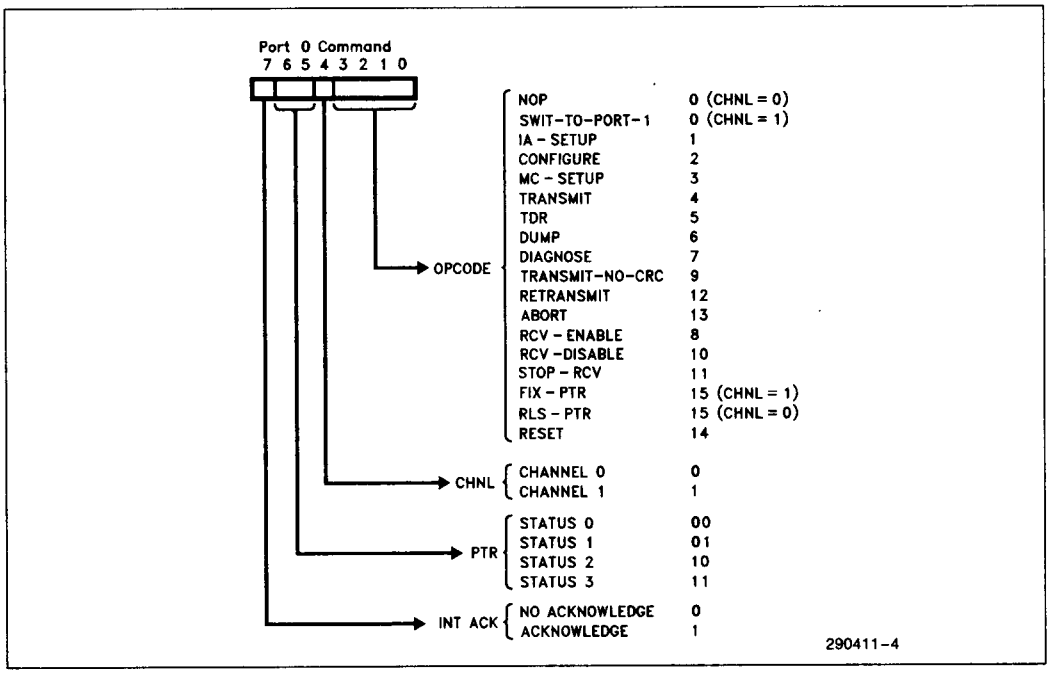


Figure 3. Port 0 Channels

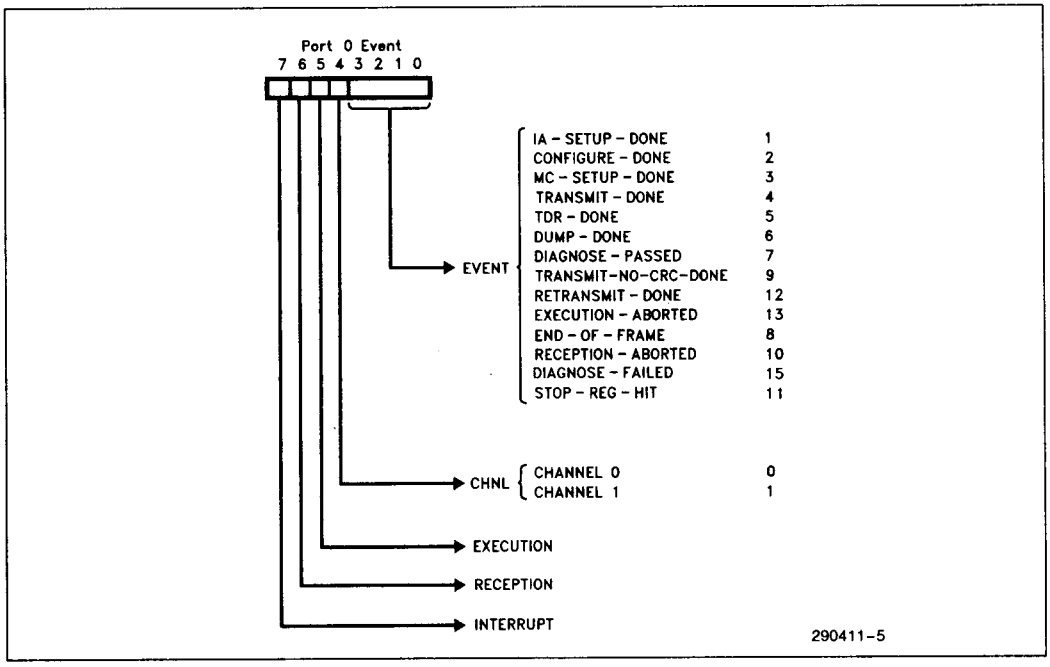


Figure 4. Port 0 Events

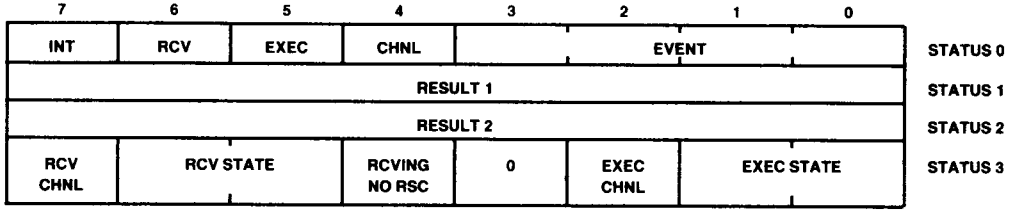


Figure 5. Port 0 Status Registers—4 Bytes

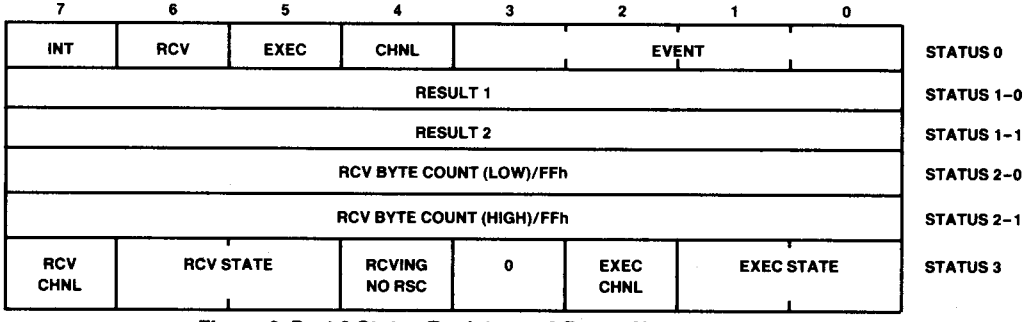


Figure 6. Port 0 Status Registers—6 Bytes, Noncontinuous Mode

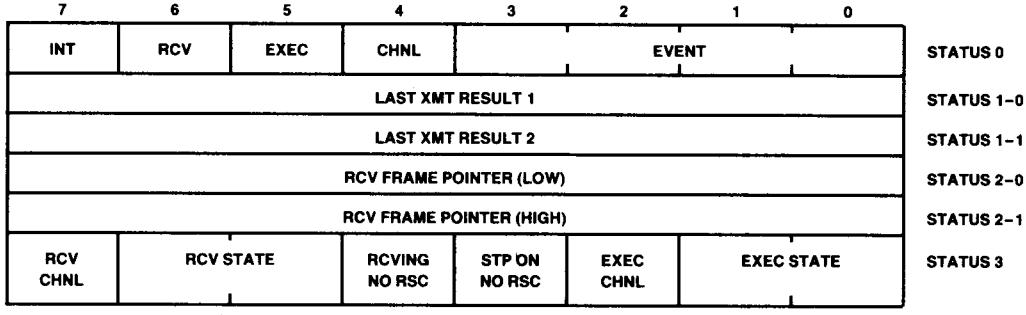


Figure 7. Port 0 Status Registers—6 Bytes, Continuous Mode

Port 1

Figures 8 and 9 show the 82593 Port 1 command register. The command register has two formats, a format for issuing the STOP-REGISTER-UPDATE command, and a format for all other commands issued to Port 1. Figure 10 shows the Port 1 commands. Port 1 is accessed when $\overline{CS1}$ is asserted, along with the assertion of the $\overline{RD}$ or $\overline{WR}$ signal. If the hardware configuration does not support $\overline{CS1}$, the SWIT-TO-PORT-1 command will switch the active port from Port 0 to Port 1. To return to Port 0, the SWIT-TO-PORT-0 command is executed.

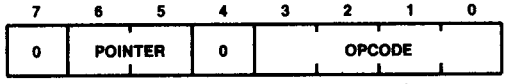


Figure 8. Port 1 Command Register, General Purpose Commands

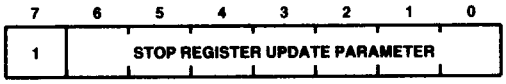


Figure 9. Port 1 Command Register, Stop Register Update Command

The Port 1 status registers are called Status Bank 1. The three registers contained in Status Bank 1 are shown in Figure 11. Status Bank 1 holds the value of the Stop Register, the Bus Throttle Timer, and the power down and high impedance states.

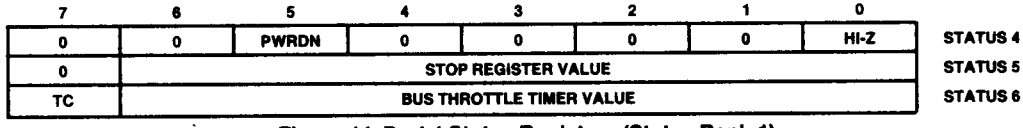


Figure 11. Port 1 Status Registers (Status Bank 1)

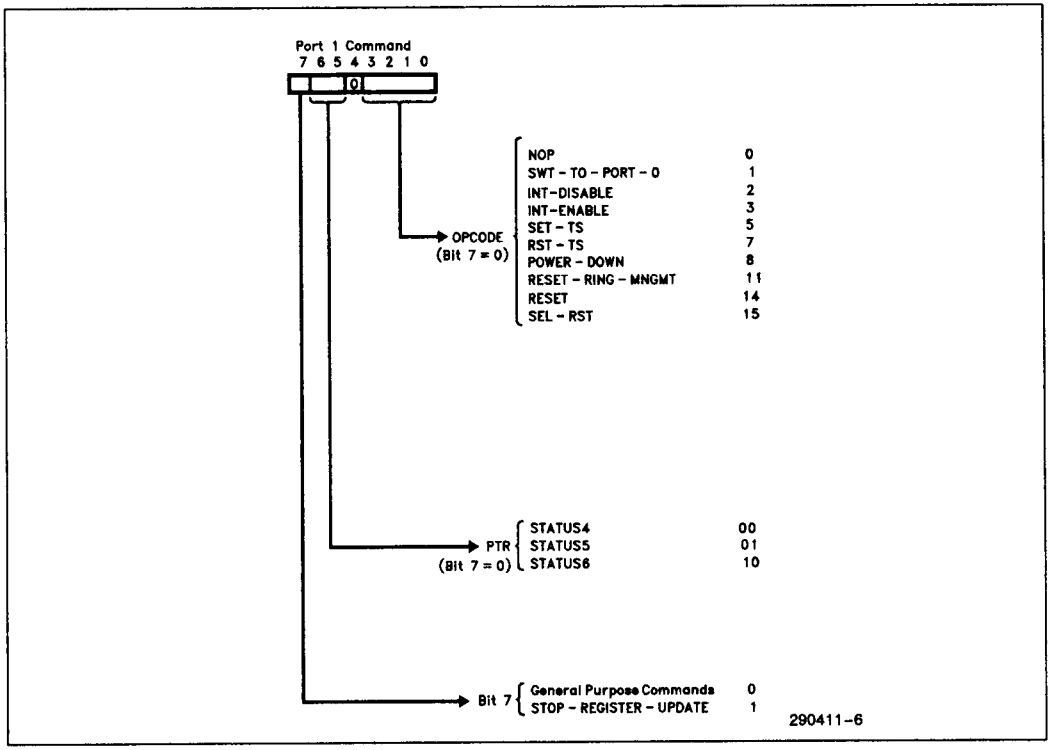


Figure 10. Port 1 Commands

82593 AND HOST CPU INTERACTION

The CPU interacts with the 82593 through the system's memory and the 82593's on-chip registers (see Figure 12). The CPU writes commands to the 82593 using the $\overline{CS0}$ (or $\overline{CS1}$) and $\overline{WR}$ signals, and reads status using $\overline{CS0}$ (or $\overline{CS1}$) and $\overline{RD}$. Parametric commands such as TRANSMIT, CONFIGURE, etc., require the transfer of data parameters from memory to the 82593. These data transfers are requested by the 82593 via its DRQ0 or DRQ1 lines, and are usually performed by an external DMA controller. When these data (or DMA) transfers are performed, $\overline{DACK0}$ or $\overline{DACK1}$ is asserted to the 82593 along with assertion of the $\overline{RD}$ or $\overline{WR}$ lines. Table 2 summarizes this operation.

Prior to issuing a parametric command to the 82593, the CPU creates a data structure in memory, and programs the external DMA controller with the start address and byte count of the memory block. For commands which require no transfer of parameters to the 82593, i.e.; TDR, DIAGNOSE, etc. the CPU issues the command to the device, without creating a data structure in memory. The 82593 performs the command with no further involvement from the CPU. Any parameters or data associated with the command are transferred between the memory and the 82593 by the DMA controller. Upon completion of the operation, the 82593 updates the appropriate status registers and asserts its INT line to the CPU.

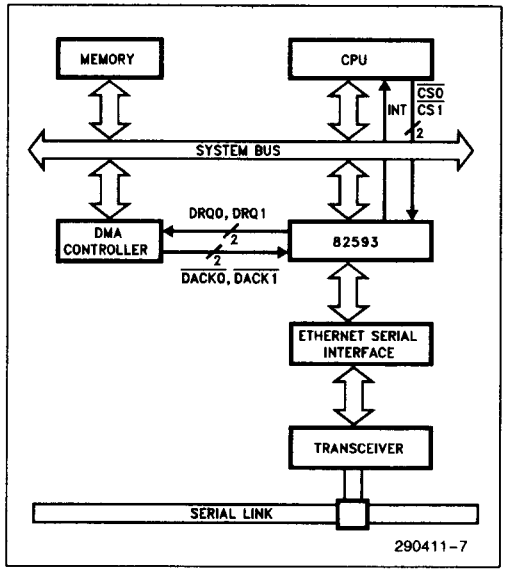


Figure 12. 82593 Host CPU Interaction

Table 2. Data Bus Control Signals and Functions

Pin Name			Function
$\overline{CS0}$ / $\overline{CS1}$*	$\overline{RD}$	$\overline{WR}$	
1	X	X	No Transfer to/from
0	1	1	Command/Status
0	0	0	Illegal
0	0	1	Read from Status Register
0	1	0	Write to Command Register
$\overline{DACK0}$ / $\overline{DACK1}$*	$\overline{RD}$	$\overline{WR}$	
1	X	X	No DMA Transfer
0	1	1	
0	0	0	Illegal
0	0	1	Data Read from DMA Channel 0 (or 1)
0	1	0	Data Write to DMA Channel 0 (or 1)

*Only one of $\overline{CS0}$, $\overline{CS1}$, $\overline{DACK0}$, or $\overline{DACK1}$ may be active at any time.

FRAME TRANSMISSION

To transmit a frame, the CPU prepares a Transmit Data Block in memory as shown in Figure 13. Its first two bytes specify the length of the rest of the block. The next few bytes (up to six) contain the destination address of the station the frame is being sent to. The rest of the block is the data field. The CPU programs the DMA controller with the start address of the block, length of the block, and other control information and then issues a TRANSMIT command to the 82593. Upon receiving this command, the 82593 fetches the first two bytes of the block to determine its length. If the link is free and at least one data byte is loaded into the 82593's XMT FIFO, the 82593 begins transmitting the preamble and concurrently requests more bytes from the transmit buffer which are loaded into the XMT FIFO to keep them ready for transmission. The 82593 can also be configured to start transmission only after the initial 64 bytes of the transmit frame are written into its XMT FIFO. The 82593 independently resolves access and possible contention on the link (collisions). When the transmission is completed, the 82593 updates its status registers and raises its INT signal to inform the CPU of the completed transmission.

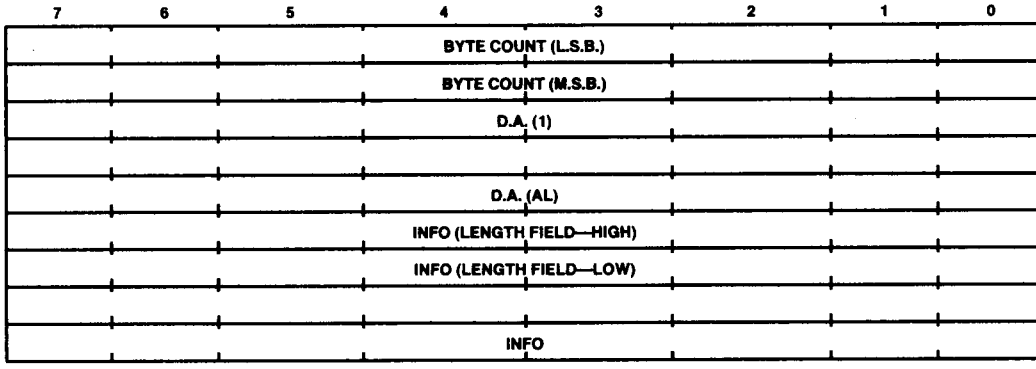


Figure 13. Transmit Frame Memory Structure

TRANSMIT FRAME CHAINING

When configured to Continuous mode, the 82593 can transmit consecutive frames without having the CPU issue the TRANSMIT command for each frame. This is called transmit frame chaining. Figure 14 shows the memory structure used for transmit chaining with the 82593 in 8-bit configuration. Figure 15 shows the structure for a 16-bit configuration. The CPU can place multiple transmit frames in memory, with each frame separated from the next by a TRANSMIT command byte. The command byte immediately follows the last byte of the transmit frame. It must contain one of three commands: TRANSMIT (04H), TRANSMIT-NO-CRC (09H) or NOP (00H).

Following a successful transmission, the 82593 requests the command byte which follows the last data byte of a frame. $\overline{EOP}$ is asserted during this cycle, indicating a successful transmission. Assertion of $\overline{EOP}$ in this mode can also be disabled.

If the command byte contains the TRANSMIT opcode, the 82593 will behave as if another TRANSMIT command has been issued by the CPU, and will attempt to transmit the new frame as soon as deferring is completed. A NOP in the command byte indicates that the preceding frame was the last frame to be transmitted and no other frames follow.

7	0	
BYTE COUNT (L.S.B.)		← Beg of the 1st Frame
BYTE COUNT (M.S.B.)		
DEST. ADDRESS		
DEST. ADDRESS (A.L.)		
LENGTH FIELD (LOW)		
LENGTH FIELD (HIGH)		
DATA FIELD		
LAST DATA FIELD BYTE		
COMMAND BYTE = 04H (TRANSMIT)		← Com for the 2nd Frame
BYTE COUNT (L.S.B.)		← Beg of the 2nd Frame
BYTE COUNT (M.S.B.)		
DEST. ADDRESS		
DEST. ADDRESS (A.L.)		
LENGTH FIELD (LOW)		
LENGTH FIELD (HIGH)		
DATA FIELD		
LAST DATA FIELD BYTE		
COMMAND BYTE = 09H (TX-NO-CRC)		← Com for the 3rd Frame
BYTE COUNT (L.S.B.)		← Beg of the 3rd Frame
BYTE COUNT (M.S.B.)		
DEST. ADDRESS		
DEST. ADDRESS (A.L.)		
LENGTH FIELD (LOW)		
LENGTH FIELD (HIGH)		
DATA FIELD		
LAST DATA FIELD BYTE		
CRC FIELD (4 BYTES)		
COMMAND BYTE = 00H (NOP)		← End of XMT Chain

Figure 14. Transmit Chaining Data Structure In Byte Mode

15 8	7 0	
BYTE COUNT (M.S.B.)	BYTE COUNT (L.S.B.)	← Beg of 1st Frame
D.A.	D.A.	
D.A. (ADDRESS LENGTH)		
INFO (LENGTH FIELD - HIGH)	INFO (LENGTH FIELD - LOW)	
INFO (LAST DATA BYTE)		
	COMMAND BYTE = 04H (TRANSMIT)	← Com for the 2nd Frame
BYTE COUNT (M.S.B.)	BYTE COUNT (L.S.B.)	← Beg of 2nd Frame
D.A.	D.A.	
D.A. (ADDRESS LENGTH)		
INFO (LENGTH FIELD - HIGH)	INFO (LENGTH FIELD - LOW)	
	INFO (LAST DATA BYTE)	
	COMMAND BYTE = 09 (TX-NO-CRC)	← Com for the 3rd Frame
BYTE COUNT (M.S.B.)	BYTE COUNT (L.S.B.)	← Beg of 3rd Frame
D.A.	D.A.	
D.A. (ADDRESS LENGTH)		
INFO (LENGTH FIELD - HIGH)	INFO (LENGTH FIELD - LOW)	
INFO (LAST DATA BYTE)		
CRC1	CRC0	
CRC3	CRC2	
	COMMAND BYTE = 00H	← End of XMT Chain

NOTE:
The second frame has an odd number of information bytes in this example.

Figure 15. Transmit Chaining Data Structure In Word Mode

AUTOMATIC RETRANSMISSION ON COLLISION

If the 82593 is configured for Internal Retransmission, the FIFO depth can be used to retransmit without the DMA controller involvement when a collision occurs. In an Ethernet network a collision should occur within the first 64 bytes (512 bits) of the transmission (within one slot time). When this configuration is used, the serial parameters should remain configured for Ethernet. A collision that occurs later than this window of 64 bytes will be flagged as a late collision and retransmission will not be attempted. The 82593 automatically prevents overwrite of the first 64 bytes in the FIFO until they have all been read out by the Serial Subsystem. The read counter of the XMT FIFO is reset, and the retransmission attempt is made using the data that is already contained in the FIFO. This process is performed automatically by the 82593. It is not necessary to reset the DMA channel for the retransmission attempt, nor is any CPU intervention required.

FRAME RECEPTION

The 82593 is ready to receive frames once it has been through its initial configuration and its receiver has been enabled. The 82593 checks incoming frames for an address match for an individual address, a multicast address, or a broadcast address. In the Promiscuous mode the 82593 receives all frames. When the address match is successful, the 82593 transfers the frame to memory using the DMA controller. Before enabling the receiver, it is the CPU's responsibility to make a memory buffer area available to the receiver and program the starting address of the DMA controller properly. The received frame can be transferred to memory via two different modes, Continuous Reception mode, or Single Frame mode.

CONTINUOUS RECEPTION MODE

In the Continuous Reception mode the 82593 can receive back-to-back frames without the need for the CPU to individually process and acknowledge each frame. In other words, in this mode the 82593 can continue to receive frames even though previous incoming received frames were not acknowledged by the CPU.

This mode makes use of a contiguous Receive Frame Area (RFA) in which multiple frames are stored sequentially. The structure in which a RCV frame is transferred to memory in this mode is shown in Figure 16 (8-bit mode) and Figure 17 (16-bit mode). The last two fields of the frame which are transferred to memory are the Status field and the Byte Count. The 82593 maintains an internal pointer which provides an offset value which can be used to point to the Byte Count of the last frame that was transferred from the 82593 to memory. This pointer is called the RCV Frame Pointer. The action of the RCV Frame Pointer, and the structure with which the frame is transferred to memory allows for back-to-back frame reception without CPU intervention. This process also allows for recovery of these frames once the CPU has responded to an incoming frame interrupt.

The RCV Frame Pointer provides an offset which is used to produce an address which always points to the location immediately following the Byte Count field of the last frame that has been transferred from the 82593 to the RFA. The beginning address of the frame can be calculated by subtracting the value of the Byte Count field from the address which points to this field. The Byte Count of a previously received (and unprocessed) frame resides one address location before the first byte of the current RCV frame. That frame, and any additional RCV frames that may have preceeded it (and have yet to be processed) can be recovered by the same calculation used to recover the last frame. This process allows frames to be continually stored in the RFA buffer without CPU intervention, and to be recovered by the CPU for processing. Figure 18 illustrates the process of back-to-back frame reception.

7	6	5	4	3	2	1	0
DESTINATION ADDRESS L.S.B.							
DESTINATION ADDRESS M.S.B.							
SOURCE ADDRESS L.S.B.							
SOURCE ADDRESS M.S.B.							
INFO (LENGTH FIELD—HIGH)							
INFO (LENGTH FIELD—LOW)							
INFO LAST BYTE							
CRC BYTE 0 (*)							
CRC BYTE 1 (*)							
CRC BYTE 2 (*)							
CRC BYTE 3 (*)							
SRT FRM	0	0	1	NO SFD	NAD MCH	IA MCH	RCLD
TYP/LEN	0	RCV OK	LEN ERR	CRC ERR	ALG ERR	0	OVR RUN
BYTE COUNT LOW							
BYTE COUNT HIGH							

NOTE:
*The CRC bytes marked with asterisks are transferred to memory only when the device is configured to do so.

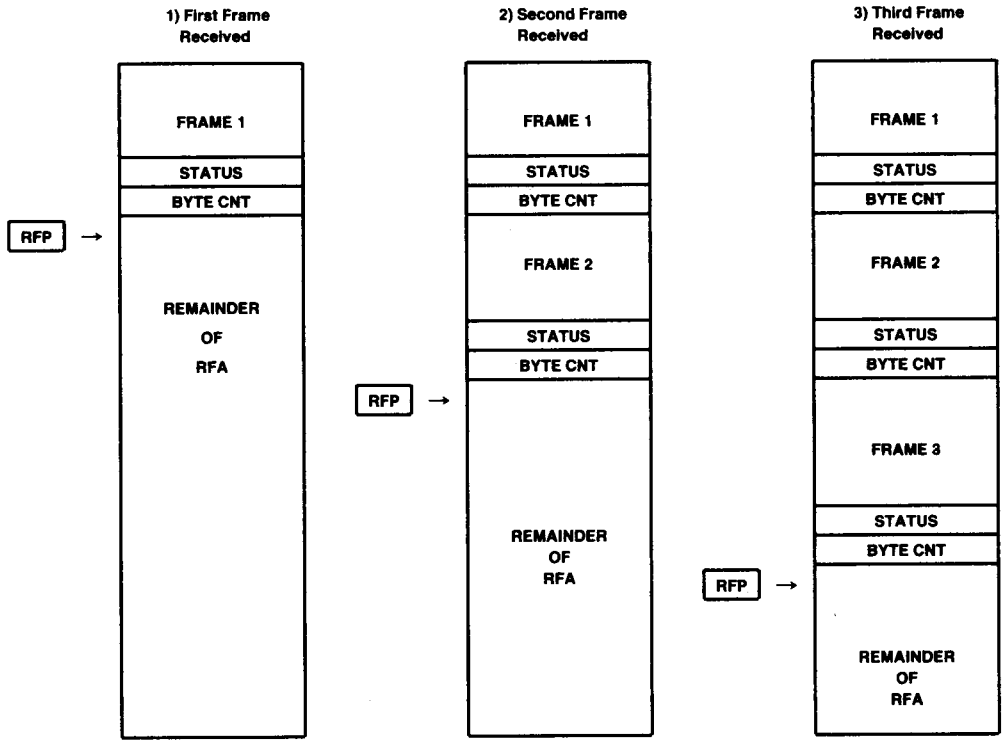
Figure 16. RCV Frame Format in Continuous Reception Mode (8-Bit Configuration)

15 — 8	7 — 0
DESTINATION ADD 2nd Byte	DESTINATION ADDRESS L.S.B.
DESTINATION ADDRESS M.S.B.	
SOURCE ADD 2nd Byte	SOURCE ADDRESS L.S.B.
SOURCE ADDRESS M.S.B.	
INFO (LENGTH FIELD—LOW)	INFO (LENGTH FIELD—HIGH)
INFO LAST WORD/BYTE	
CRC BYTE 1 (*)	CRC BYTE 0 (*)
CRC BYTE 3 (*)	CRC BYTE 2 (*)

XX	SRT FRM	0	0	1	NO SFD	NAD MCH	IA MCH	RCV CLD
XX	TYP /LN	0	RCV OK	LEN ERR	CRC ERR	ALG ERR	0	OVR ERR
FF	BYTE COUNT LOW							
FF	BYTE COUNT HIGH							

NOTE:
*The CRC bytes marked with asterisks are transferred to memory only when the device is configured to do so. If the total number of data bytes is odd, CRC Byte 3 will be written to both the LSB and MSB of the last CRC word. However, the Byte Count will ignore this duplication of the last byte, counting only four bytes of CRC.

Figure 17. Receive Format In Continuous Reception Mode (16-Bit Configuration)



NOTE:
The RFP always points to the location immediately following the last frame that was transferred to memory. Based on the value of the RFP and the byte count of each frame, the CPU recovers the RCV frames.

Figure 18. Back-to-Back Frame Reception in Continuous Reception Mode

RECEIVE STOP REGISTER (Ring Buffer Implementation)

The 82593 contains a Receive Stop Register. This feature, along with the Receive Frame Pointer, allows for implementation of a recyclable ring buffer when the 82593 is interfaced to a DMA controller (8237A, 82380/370, etc.) or bus (PC AT** compatible, EISA, etc.) which feature an auto-initialize mode. The Stop Register indicates the last location that has been processed in the RFA. This area of the RFA is now available for storage of new incoming frames. This allows the RFA to be continually recycled as it wraps around its ring buffer memory structure.

SINGLE FRAME RECEPTION

In Single Frame mode, the entire RCV frame is contained in one continuous buffer. Upon completion of reception, the status of the frame is appended at the end of the received frame and the total number of bytes transferred to memory is loaded into status registers 1 and 2. An interrupt is then generated to the CPU indicating that a frame has been received.

In this mode, the 82593 can receive one additional frame if an interrupt is pending from a previous reception. In other words, in this mode it can receive two frames without an acknowledge from the CPU. If a third frame arrives before one of the first two frames has been acknowledged, this frame will not be transferred to memory and may eventually overrun internally in the 82593. Figure 19 shows the format with which a received frame is transferred to memory from the 82593 in Single Frame mode in Byte mode. Figure 20 shows frame format in Word mode.

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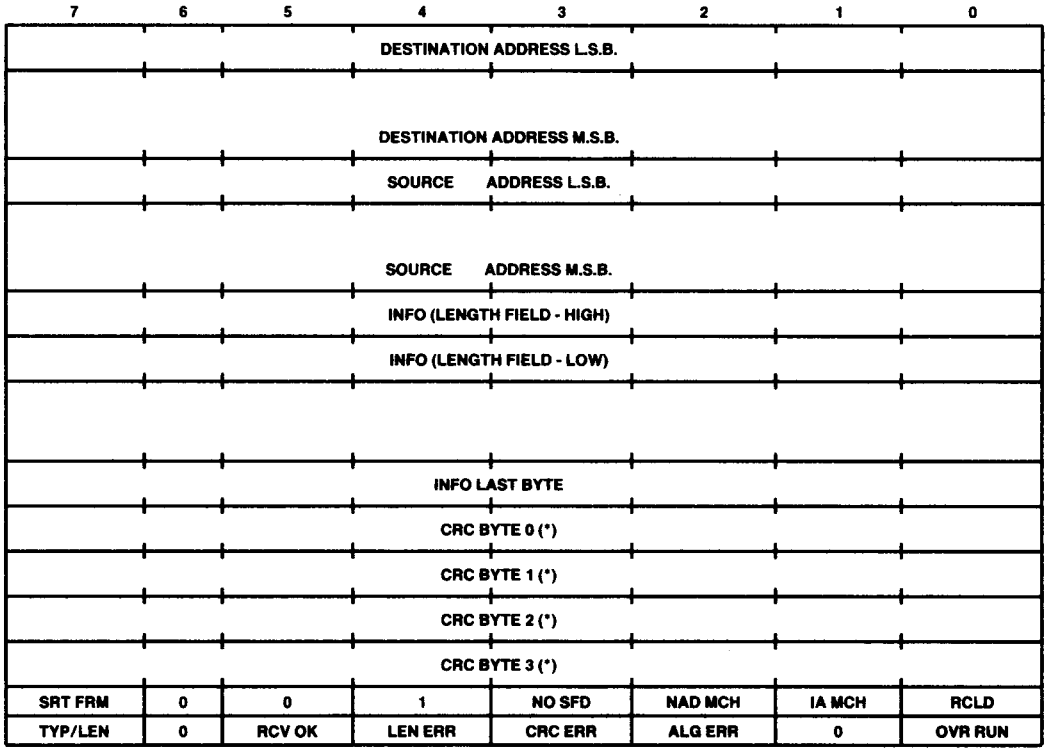


NOTE:
*The CRC bytes marked with asterisks are transferred to memory only when the device is configured to do so.

Figure 19. Receive Format in Byte, Single Buffer Reception Mode

15 — 8	7 — 0
DESTINATION ADD 2nd Byte	DESTINATION ADDRESS L.S.B.
DESTINATION ADDRESS M.S.B.	
SOURCE ADD 2nd Byte	SOURCE ADDRESS L.S.B.
SOURCE ADDRESS M.S.B.	
INFO (LENGTH FIELD—LOW)	INFO (LENGTH FIELD—HIGH)
INFO LAST WORD/BYTE	
CRC BYTE 1 (*)	CRC BYTE 0 (*)
CRC BYTE 3 (*)	CRC BYTE 2 (*)

XX	SRT FRM	0	0	1	NO SFD	NAD MCH	IA MCH	RCV CLD
XX	TYP /LN	0	RCV OK	LEN ERR	CRC ERR	ALG ERR	0	OVR ERR

NOTE:
*The CRC bytes marked with asterisks are transferred to memory only when the device is configured to do so. If the total number of data bytes is odd, CRC Byte 3 will be written to both the LSB and MSB of the last CRC word. However, the Byte Count will ignore this duplication of the last byte, counting only four bytes of CRC.

Figure 20. Receive Format In Word, Single Buffer Reception Mode

82593 CHANGES FROM THE 82590

The 82593 has a number of functional changes from the 82590. Some changes are functional enhancements from the 82590, while some changes are deletions of currently existing 82590 functionality.

This section is provided for the reader who is currently familiar with the 82590. For more information on the 82590 please consult the Intel LAN Components User's Manual.

Enhancements

Parallel Subsystem Enhancements

- **FIFO Subsection**—The RCV and XMT FIFOs of the 82593 are both expanded to 96 bytes deep, giving a total of 192 bytes of buffering on the device. The 82593 FIFOs can be configured to an 82590 compatible mode of 32 bytes each, and a threshold set at 16.
- **Internal Retransmission From XMT FIFO**—The 82593 can be programmed to hold the first part of a transmit frame internally in its XMT FIFO. In the case of a collision, the data for retransmission is automatically retransmitted from the XMT FIFO.
- **Start of Transmit Threshold**—The 82593 can be configured to delay start of transmission until the XMT FIFO threshold has been reached.
- **Bus Throttle Timer**—The 82593 can be programmed to a maximum time that it can have access to a system bus. When this timer expires, the 82593 will deassert its DMA request releasing the bus.
- **RCV Frame Pointer**—The 82593 contains a counter and a status register which points to the last RCV frame transferred to memory. This enables back-to-back frame reception without CPU intervention or the addition of external glue. The size of the counter is programmable.
- **RCV STOP Register**—The 82593 contains a RCV Stop Register which can be used to implement a recyclable ring buffer in conjunction with the RCV Frame Pointer.
- **Dynamic CRC Enable/Disable on XMT**—The 82593 can dynamically enable or disable insertion of CRC for individual transmit frames.
- **Transmit Frame Chaining Statistics**—The 82593 provides the status of each frame in a chain of transmissions in its status registers until it is replaced by the next frame in the chain. The $\overline{EOP}$ pin signals to the system that a status is available.
- **Synchronous DRQ Deassertion**—The 82593 can be configured to always deassert its transmit DRQ line synchronously to the falling edge of $\overline{WR}$ even when transmission is terminated due to an error condition such as Underrun, Lost CRS or CTS, etc.
- **Port 1 Redefined**—Port 1 functionality has been reduced and modified. Port 1 supports maintenance commands and new commands controlling the RCV Frame Pointer and RCV Stop Register. Port 1 status contents has also been redefined. It now holds the Stop Register and Bus Throttle Timer contents and the Power-Down Status.
- **Big Endian (Byte Swapping) Redefined**—When the Big Endian mode is enabled, the Byte Count field is not swapped. Only the Data field of transmit and receive packets are swapped.

Serial Subsystem Enhancements

- **LPBK/CTS Pin Polarity**—The 82593 LPBK output, and CTS input polarity is selectable by configuration. This allows for a direct interface to the 82C501AD LPBK input.
- **IFS Window Implementation**—The 82593's IFS (Inter Frame Space) counter can be configured to be retriggerable for up to ⅔ of the IFS after frame transmission.
- **Late Collision Detection**—The 82593 interprets a late collision as one which occurs after a slot time has expired from the beginning of the preamble.
- **CRS1 Mode**—The 82583 CRS1 mode provides carrier lost detection for broadband applications.
- **RCV Grace Period**—The 82593 can be configured to delay sampling of receive data for the first 8-bit times of the preamble.
- **Hash Table Decode**—The 82593 can be configured to decode writing into its Hash Table during a MC Setup by two different hashing methods.
- **Length/Type Field Discrimination**—The 82593 can be configured to interpret the Length/Type field as a Type field for values in this field greater than 1500.
- **$\overline{RTS}$ Pin State**—$\overline{RTS}$ is guaranteed to be in the inactive state on power up (regardless of whether TXC or CLK is active), before and during reset assertion. Hardware reset triggers this pin from the high impedance state.
- **OR CDT/CRS**—The 82593 can be configured to logically OR internally the CDT and CRS pins during transmission.
- **Foreign ESI Mode**—The 82593 provides configurability of the serial interface pins polarity and timing in order to be compatible with either the Intel 82C501AD or the AMD SIA serial interface device.

DELETIONS

Serial Subsystem Deletions

- **Deterministic Collision Resolution Mode (DCR)**—DCR is not implemented in the 82593.
- **82590 Mode 0 Functionality**—The Mode 0, or High Integration Mode of the 82590, and its associated functionality, is not included in the 82593.
- **INT CDT/CDBBC**—Internal CDT and the CDBBC mode of collision detect are not included in the 82593.
- **RCV Jabber**—RCV jabber functionality is not included in the 82593. XMT jabber is still included.
- **Serial Parameters Configurability Reduced**—The 82593 supports a reduced set of configurable serial parameters.
- **Manchester Encoding**—The 82590 Mode 1 Manchester Encoding functionality is not included in the 82593.
- **HDLC Framing**—HDLC framing is not supported in the 82593.
- **Preamble until CRS**—This mode is not supported in the 82593.

Parallel Subsystem Deletions

- **General Purpose Timer**—The General Purpose Timer is not included in the 82593.
- **Event Counters**—The three Event Counters are not included in the 82593.
- **Remote Power Down**—The 82593 has only the Local Power Down mode (referred to as Power Down). Remote Power Down mode has been deleted.
- **RCV Buffer Chaining and Frame Switching Modes**—The RCV Buffer Chaining and RCV Frame Switching modes are not implemented in the 82593.
- **Non TCI EOP Modes**—The XMT and RCV EOP modes have been deleted. The 82590 TCI mode remains in the 82593. It is called Continuous mode. The $\overline{EOP}$ and DRQ pins maintain the previous TCI signals handshake. As an option, TCI signalling may be disabled.
- **Port Switching Simplified**—Software switching between ports (Port 0 or 1) is not enabled if hardware access to both ports (both $\overline{CS0}$ and $\overline{CS1}$ are enabled) is implemented. The 82593, however, keeps compatibility with the workaround fix of the "SWIT-TO-PORT-1 erratum" of the 82590.
- **Frame Count In Status**—The 82593 does not record the Frame Count field in its RCV status registers.

APPLICATIONS

PC MOTHERBOARD APPLICATIONS

The 82593 has several unique features that enable implementing a high-performance LAN connection on a PC motherboard with minimal cost and complexity.

Figure 21 shows a 82593 based LAN design on a PC motherboard. It consists of an 82593, a PLD, and two transceivers.

This solution uses the available system resources (DMA and memory) to provide those functions normally added to a LAN solution. Removing DMA and local memory reduces cost and complexity of a LAN solution. Two host DMA channels, one for receive and one for transmit, are used. The DMA interface from the 82593 (through the PLD) is the standard handshake of DMA request and acknowledge. The required memory buffer size depends on the specific applications and the amount of free memory available. The buffer size can be specified by the programmer.

Peripherals on a motherboard must compete for access to the system bus. Because there is no local buffer for intermediate buffering of data, data transfers take place in real time over the system bus to system memory. A very large internal storage area (96-byte receive and transmit FIFOs) enables the 82593 to wait for access to the system bus while serial data is being received or transmitted. The depth of the transmit FIFO allows the 82593 to retransmit the data without DMA involvement, thus reducing the load on the PC bus. The on-chip logic of the 82593 provides a recyclable ring buffer on the PC bus without any external glue.

CUSTOMIZED APPLICATIONS

The 82593 can be interfaced to an ASIC (or Gate Array) device which provides a custom solution for a variety of applications. The 82593 functions as the CSMA/CD core of this type of solution, with the ASIC providing the control and interface functionality usually performed by several ICs. This allows for the implementation of a low component count, cost effective solution for a variety of buses, including buses for which highly integrated, customized silicon is not currently offered. Figure 22 illustrates a 82593SX/ASIC solution.

The ASIC can provide a direct interface to the host system (the host can be either a proprietary or standard bus), performing functions such as address decoding, and control and data interface. The ASIC also directly supports the 82593 and any local mem-

ory required in the solution. The ASIC asserts the $\overline{CS}$ and $\overline{RD}$ or $\overline{WR}$ to the 82593 for host accesses to its command or status registers. The ASIC provides the control for host accesses to the local memory, to allow the host to access data for transmission, reception, or initialization. It provides DMA support to the 82593 during operations such as transmission, configuration, and reception. The ASIC also arbitrates simultaneous accesses to the local memory between the host system and the 82593.

EMBEDDED APPLICATIONS

The 82593 can also work in a variety of embedded applications. These applications can include industrial control, interconnect, and print servers among others. These applications can utilize the 82593 interfaced to an ASIC or interfaced to standard components such as the Intel 80C186 embedded processor. The 82593 has a glueless interface to the 80C186 (or 80C188). The 80C186 is a highly integrated embedded processor. It contains a DMA unit, address decoding, a control unit, and an interrupt controller. These functions allow it to directly control the 82593 without the need for external logic. Its two channel DMA unit services the 82593 receive and transmit DMA requests, transferring data between the 82593 and the local memory resources. Its control and address decoding allow direct access to the 82593's command and status registers via the 80C186's Data, $\overline{PCS}$ and $\overline{RD}$ or $\overline{WR}$ lines. The 82593 interrupts the 80C186 through one of the 80C186 INT lines. Figure 23 illustrates the interface between the 80C186 and the 82593.

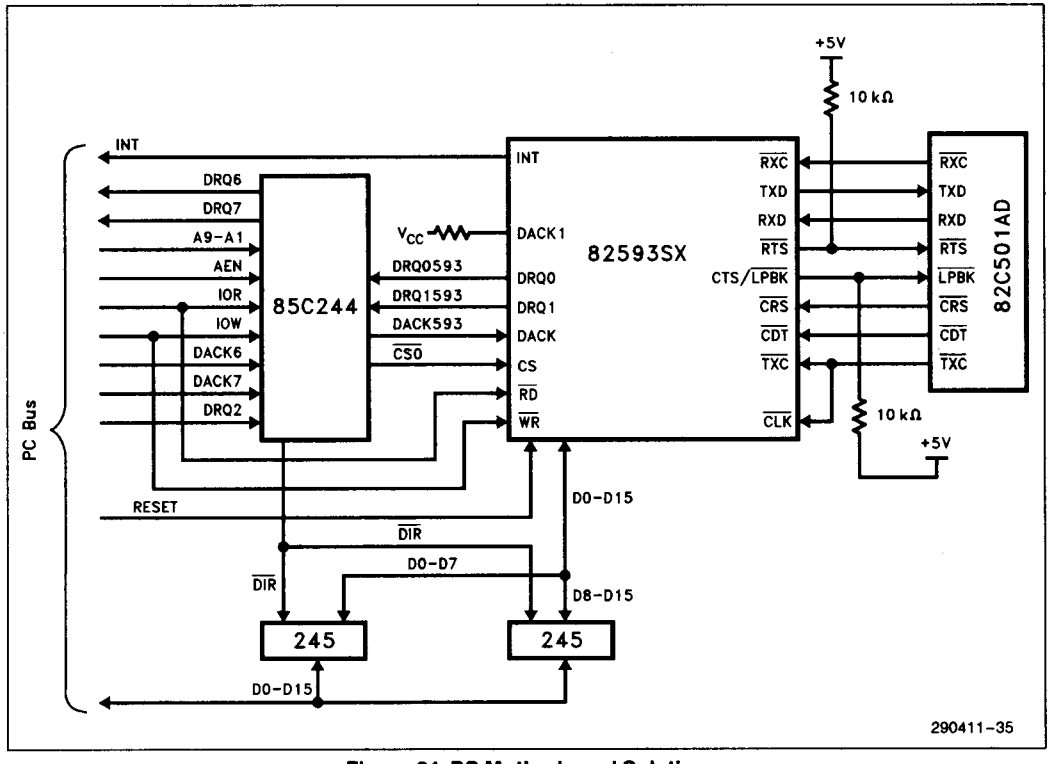


Figure 21. PC Motherboard Solution

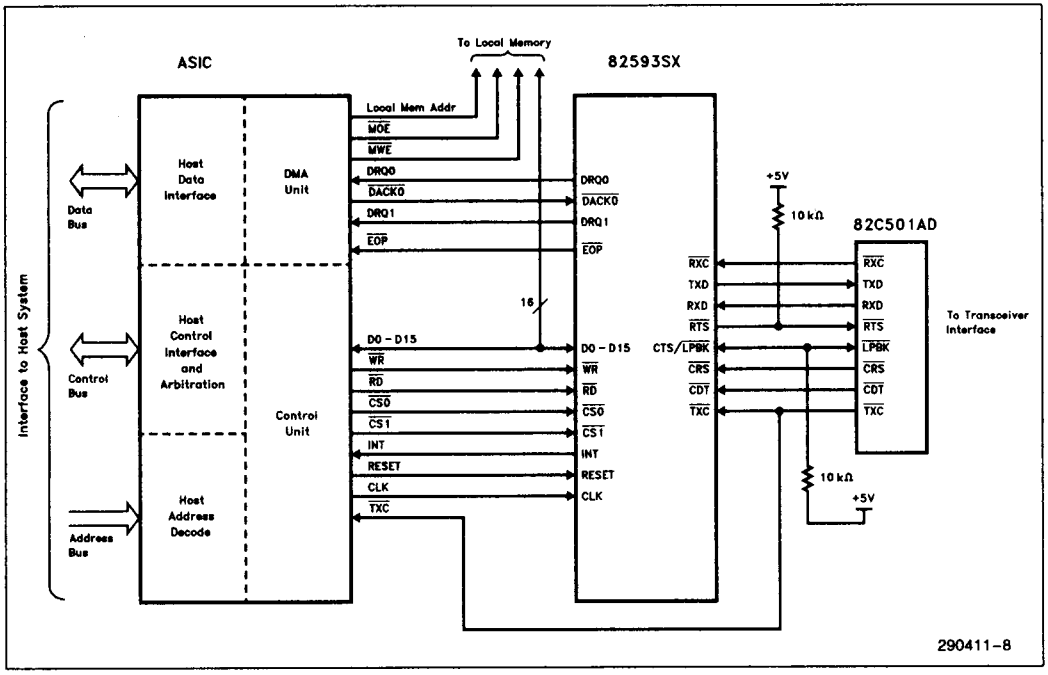


Figure 22. 82593SX/ASIC Design Example

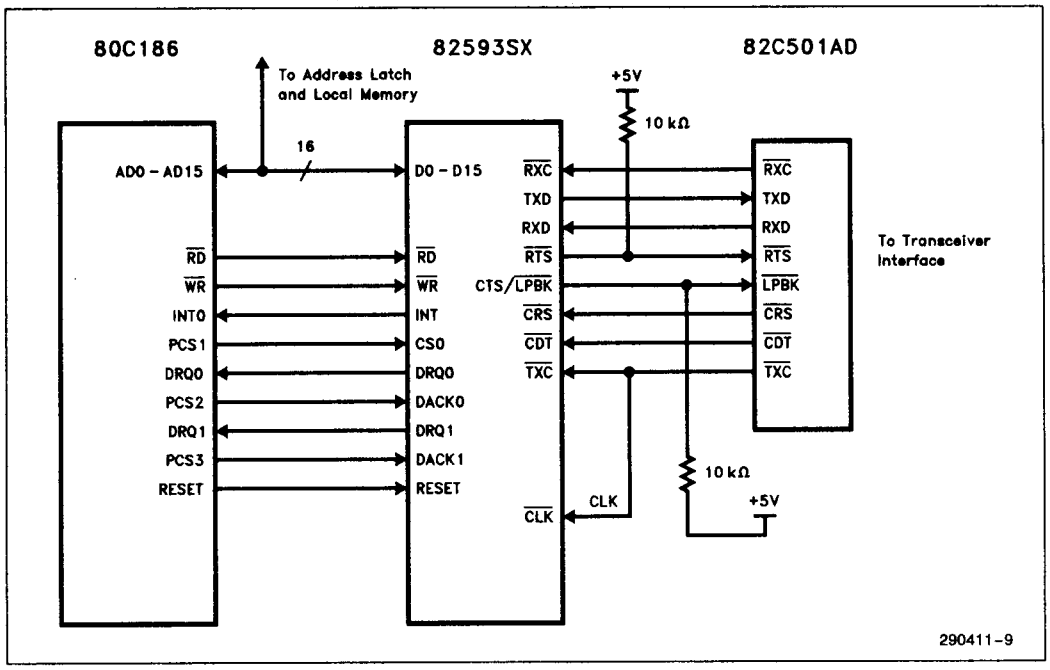


Figure 23. 82593SX/80C186 Interface

ABSOLUTE MAXIMUM RATINGS

Case Temperature (T_C) Under Bias
- Plastic ..... 0°C to +85°C
- PLCC ..... 0°C to +85°C

Storage Temperature ..... −65°C to +140°C

Voltage on any Pin with Respect to Ground ..... −1V to +7V

Power Dissipation ..... 330 mW

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

PACKAGE THERMAL SPECIFICATIONS

Parameter	Thermal Resistance	
	PLCC	PDIP
θJunction-to-Case	16 C°/Watt	36 C°/Watt
θJunction-to-Ambient	36 C°/Watt	96 C°/Watt

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±10%; I_{CC} = 60 mA

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (TTL)	−0.5	+0.8	V	
V_{IH}	Input High Voltage (TTL)	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (TTL)		0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage (TTL)	2.4		V	I_{OH} = −400 μA
I_{LI}	Input Leakage Current		±10	μA	$0 \le V_{IN} \le V_{CC}$
I_{LO}	Output Leakage Current		±10	μA	$0.45 \le V_{OUT} \le V_{CC}$
C_{IN}	Capacitance of Input Buffer		10	pF	FC = 1 MHz
C_{OUT}	Capacitance of Input/Output Buffer		20	pF	FC = 1 MHz
I_{CC}	Power Supply Current		60 7	mA mA	Active Power Down

NOTES:
1. D0–D15 capacitance is 20 pF–125 pF. All other pins capacitance is 20 pF–50 pF.
2. $\overline{RTS}$/TENA I_{OH} is 2.4 mA in Foreign ESI mode, $\overline{CTS}$/LPBK I_{OH} is 2.4 mA when LPBK is asserted and R_{VSS} = 2.2K.
3. All currents without loading.
4. Power down mode—all inputs at idle level except CLK input.

SYSTEM INTERFACE A.C. TIMINGS

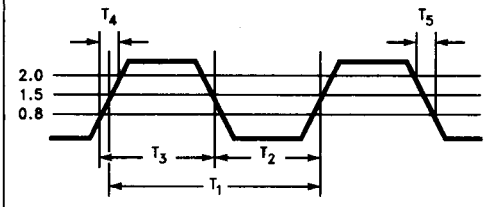
A.C. Timings Test Waveform

The measurements should be done at:

290411-10

A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 1.5V for both a logic "1" and "0".
Rise and fall time of inputs and outputs signals are measured between 0.8V and 2V respectively.

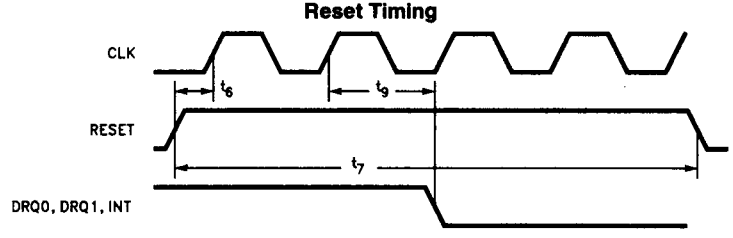
System Clock Timing



290411-11

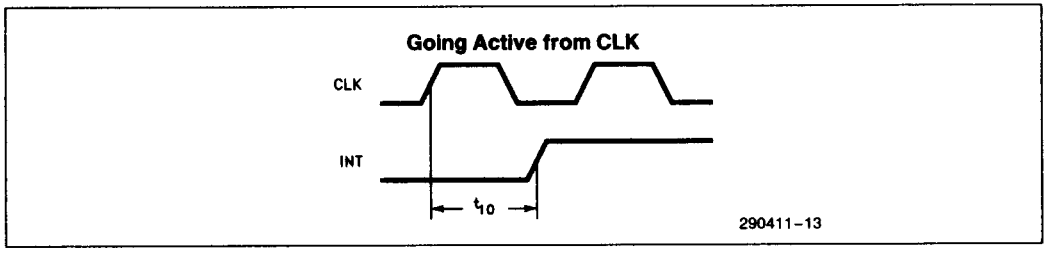
For CLK: t3 and t2 are 20 ns minimum @ 20 MHz.

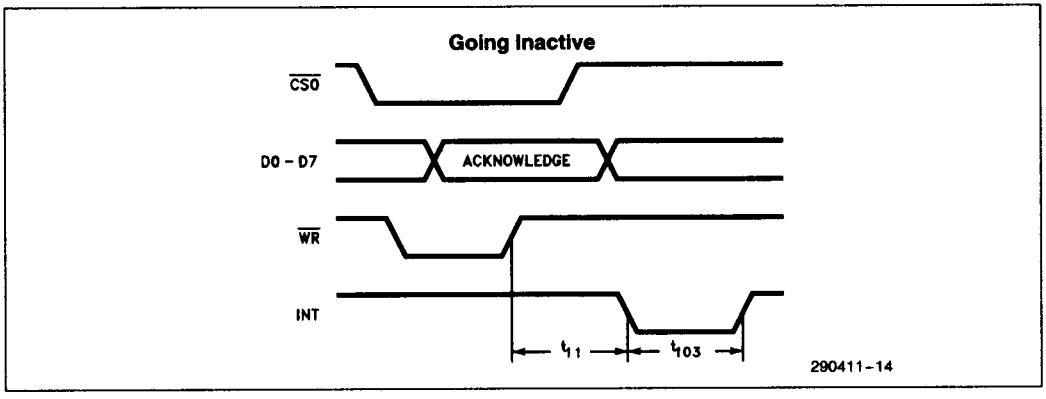
Reset Timing Diagram

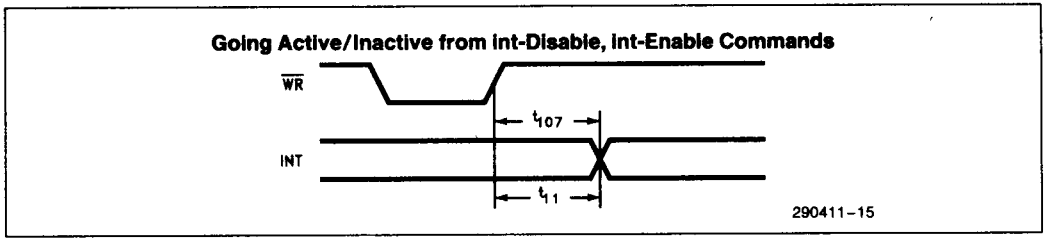


290411-12

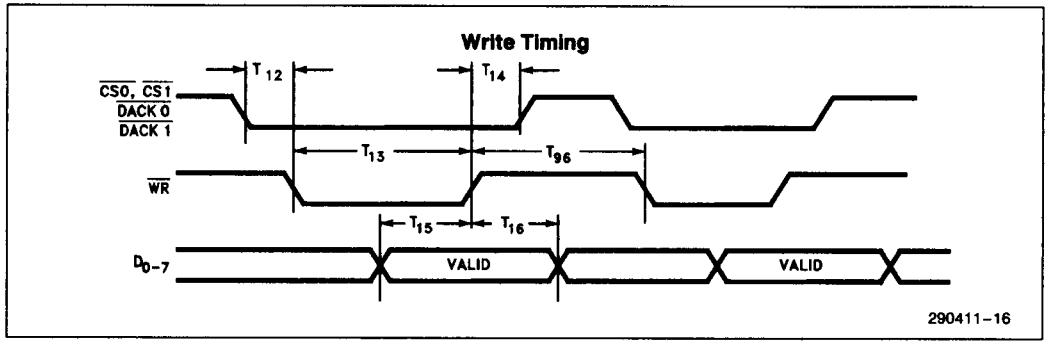
Interrupt Timing Diagrams

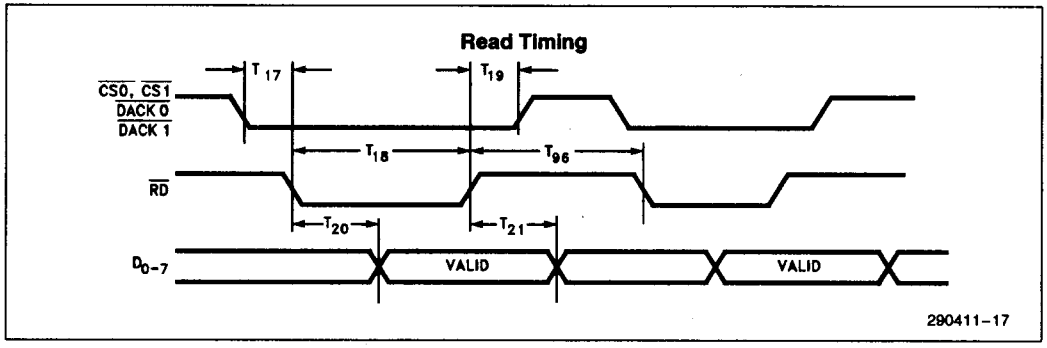






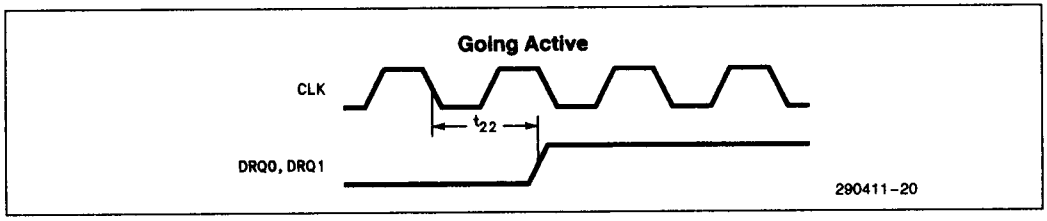
Write/Read Timing Diagrams

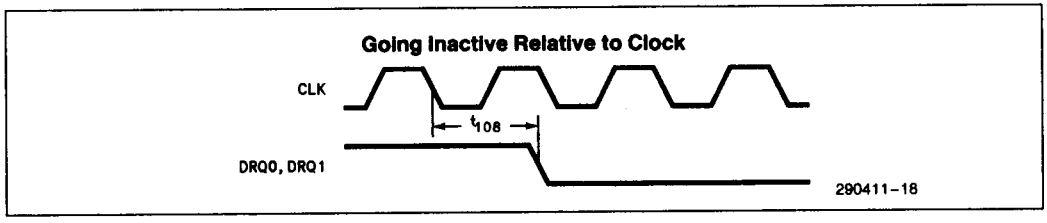


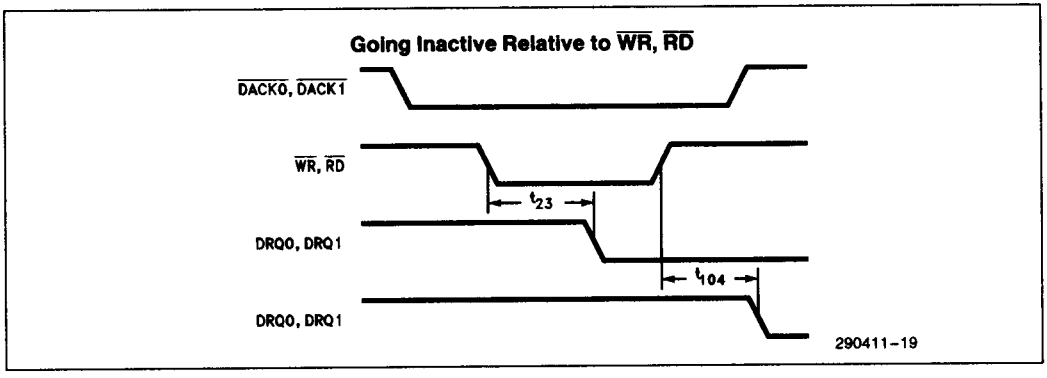


DRQ, EOP Timing Diagrams

DMA REQUEST

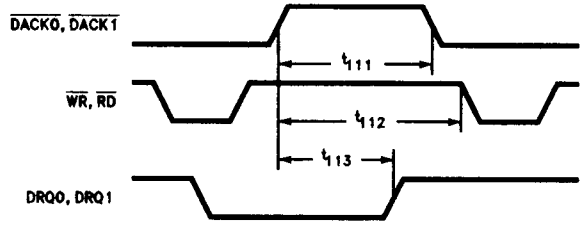






DRQ, EOP Timing Diagrams (Continued)

DMA Acknowledge Inactive Timing



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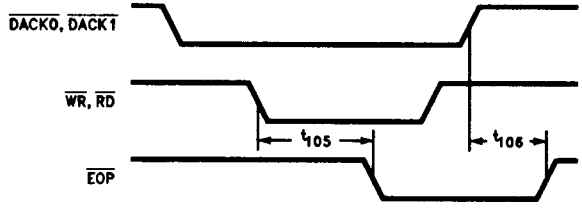
EOP Timing



290411-22

SYSTEM INTERFACE TIMING CHARACTERISTIC VALUES

C1 on all outputs is 20 pF–125 pF for D0–D15 and 20 pF–50 pF for other pins.

Symbol	Parameter	Min	Max	Units	Note
CLOCK INPUT PARAMETERS					
t1 t1a	CLK Cycle Period (16 MHz) CLK Cycle Period (20 MHz)	62.5 50.0	1000 1000	ns ns	
t2 t2a	CLK Low Time (16 MHz) CLK Low Time (20 MHz)	24 20		ns ns	5 5
t3 t3a	CLK High Time (16 MHz) CLK High Time (20 MHz)	24 20		ns ns	5 5
t4	CLK Rise Time		5	ns	1
t5	CLK Fall Time		5	ns	2
RESET PARAMETERS					
t6	Reset Active to Clock High	16		ns	3
t7	Reset Pulse Width	4*t1		ns	
t9 t9a	CTRL Inact aft Reset (16 MHz) CTRL Inact aft Reset (20 MHz)		125 100	ns ns	
INTERRUPT PARAMETERS					
t10	CLK High to Interrupt Active		45	ns	
t11	$\overline{WR}$ Idle to Interrupt Idle		45	ns	
t103	Int Low to Int High Gap	2*t1		ns	
t107	$\overline{WR}$ Idle to Interrupt Active		45	ns	
WRITE PARAMETERS					
t12	$\overline{CS0}$, $\overline{CS1}$, $\overline{DACK0}$, or $\overline{DACK1}$ Setup to $\overline{WR}$ Low	0		ns	
t13 t13a	$\overline{WR}$ Pulse Width (16 MHz) $\overline{WR}$ Pulse Width (20 MHz)	55 45		ns ns	
t14	$\overline{CS0}$, $\overline{CS1}$, $\overline{DACK0}$ or $\overline{DACK1}$ Hold after $\overline{WR}$ High	0		ns	
t15	Data Setup to $\overline{WR}$ High	25		ns	
t16	Data Hold after $\overline{WR}$ High	0		ns	
t96 t96a	CTRL/CTRL Inactive (16 MHz) CTRL/CTRL Inactive (20 MHz)	55 45		ns ns	10 10
READ PARAMETERS					
t17	$\overline{CS0}$, $\overline{CS1}$, $\overline{DACK0}$ or $\overline{DACK1}$ Setup to $\overline{RD}$ Low	0		ns	
t18 t18a	$\overline{RD}$ Pulse Width (16 MHz) $\overline{RD}$ Pulse Width (20 MHz)	55 45		ns ns	
t19	$\overline{CS0}$, $\overline{CS1}$, $\overline{DACK0}$ or $\overline{DACK1}$ Hold after $\overline{RD}$ High	0		ns	

SYSTEM INTERFACE TIMING CHARACTERISTIC VALUES (Continued)

C1 on all outputs is 20 pF–125 pF for D0–D15 and 20 pF–50 pF for other pins.

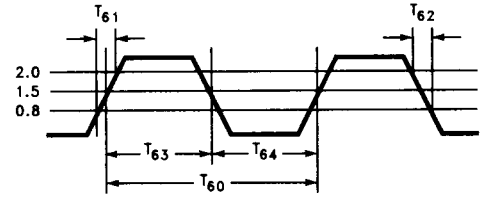
Symbol	Parameter	Min	Max	Units	Note
READ PARAMETERS (Continued)					
t20 t20a	$\overline{RD}$ Low to Data Valid (16 MHz) $\overline{RD}$ Low to Data Valid (20 MHz)		45 35	ns ns	6 6
t21	Data Float after $\overline{RD}$ High	2	30	ns	
DMA PARAMETERS					
t22	CLK Low to DRQ0/1 Active		45	ns	
t23	$\overline{WR}$/$\overline{RD}$ Low to DRQ0/1 Inactive		33	ns	
t104	$\overline{WR}$/$\overline{RD}$ High to DRQ0/1 Inactive, NOK TCI Signal	5	45	ns	
t105	$\overline{WR}$ or $\overline{RD}$ Low to $\overline{EOP}$ Active		30	ns	7
t106	$\overline{EOP}$ Float after $\overline{DACK0}$ or $\overline{DACK1}$ Going Inactive	2	40	ns	7
t108	CLK Low to DRQ0 or DRQ1 Inactive		45	ns	8
THROTTLE PARAMETERS					
t111	$\overline{DACK}$ High to $\overline{DACK}$ Low	2*t1		ns	9
t112	$\overline{DACK}$ High to Next DMA $\overline{WR}$/$\overline{RD}$	2.5*t1		ns	9
t113	$\overline{DACK}$ High to DRQ Reassertion	1*t1		ns	

NOTES:
1. 0.8V to 2.0V.
2. 2.0V to 0.8V.
3. To guarantee recognition at next clock.
5. Measured at 1.5V.
6. 60 ns with up to 200 pF load (NMOS compatible).
7. Open collector IO pin.
8. Valid for ABORT only.
9. None of the A.C. parameters related to the CLK out pin.
10. For Command to Command $\overline{WR}$ minimum is 9 t1 + t96.
    For $\overline{WR}$ to $\overline{RD}$, minimum is 3 t1 + t96.
    For $\overline{CS0/1}$ $\overline{WR}$ to $\overline{CS0/1}$ $\overline{WR}$, minimum is 9 t1 + t96.
    For $\overline{CS0/1}$ $\overline{RD}$ to $\overline{CS0/1}$ $\overline{WR}$, minimum is 3 t1 + t96.
    For DMA access to CS0/1# access, minimum is 2 t1.
    For $\overline{CS0/1}$ access to DMA access, minimum is 2 t1.
    For Status 2 to 3 $\overline{RD}$ to $\overline{RD}$ access, minimum is 2 t1 + t96.
    Maximum DMA rate is 1 Transfer for each 2 t1.

SERIAL INTERFACE A.C. TIMINGS

Clock Timing

Serial Input Clock Timing



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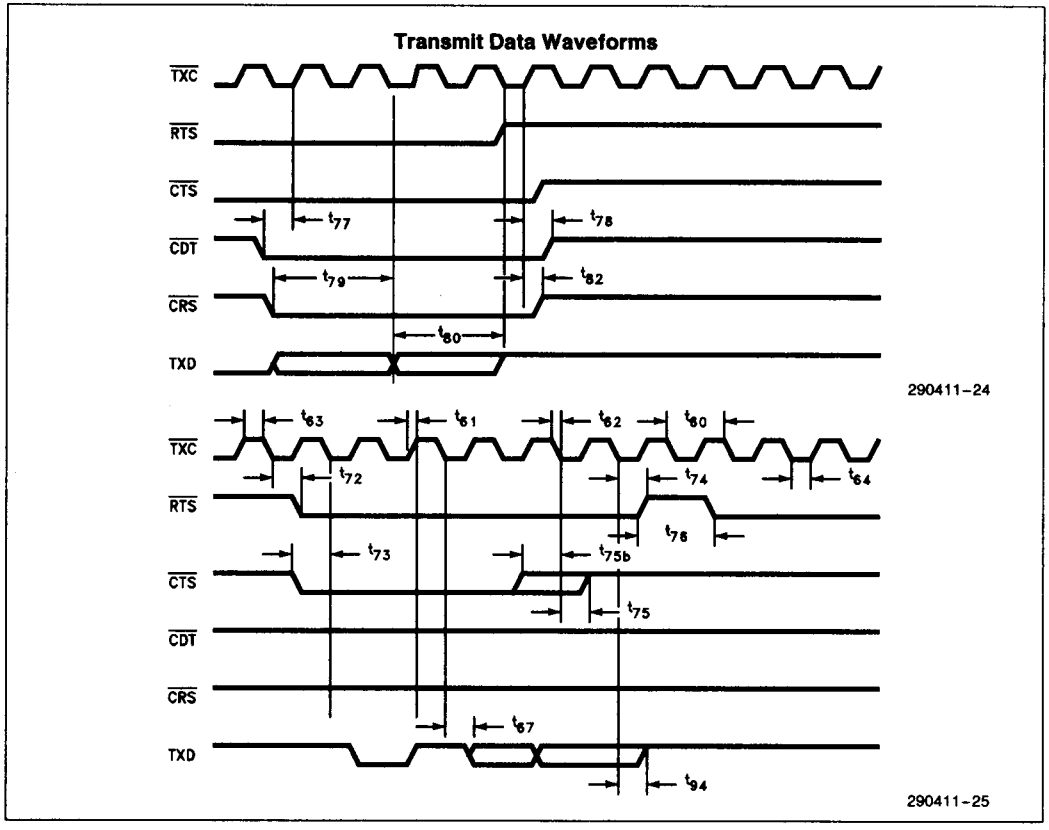
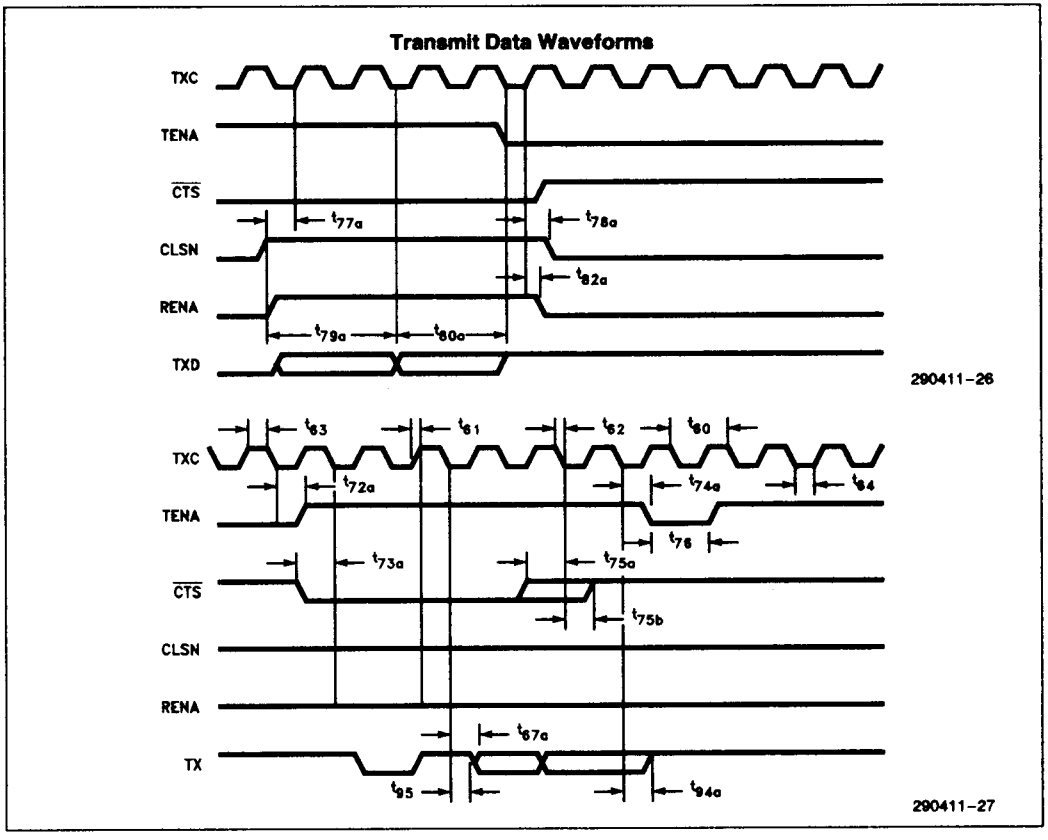
NOTES:
High level may vary with V_{CC}. A tolerance of ±100 PPM is required for Ethernet only. The 82593 can operate with the 82501 $\overline{RXC}$ and $\overline{TXC}$ and the SIA TXC and RXC parameters at 10 MHz as described in their respective data sheet.

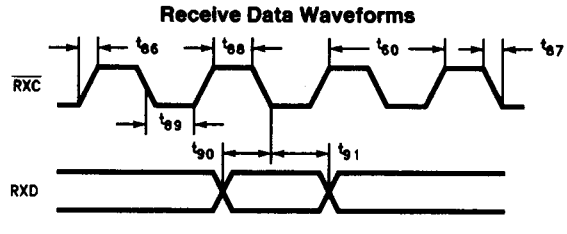
Transmit Data Timing Diagrams—82C501 Mode



Transmit Data Timing Diagrams—Foreign ESI Mode



Receive Data Timing Diagrams—82C501 Mode



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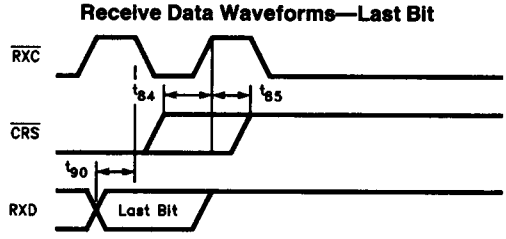

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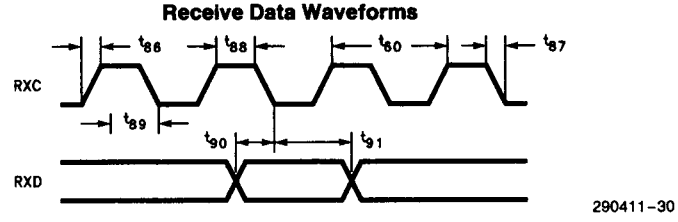
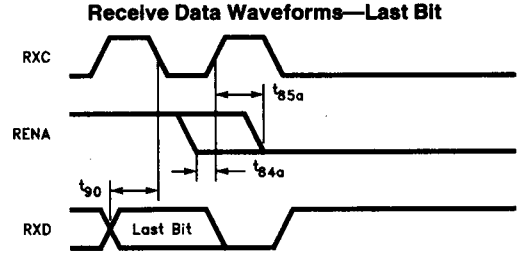
Receive Data Timing Diagrams—Foreign ESI Mode

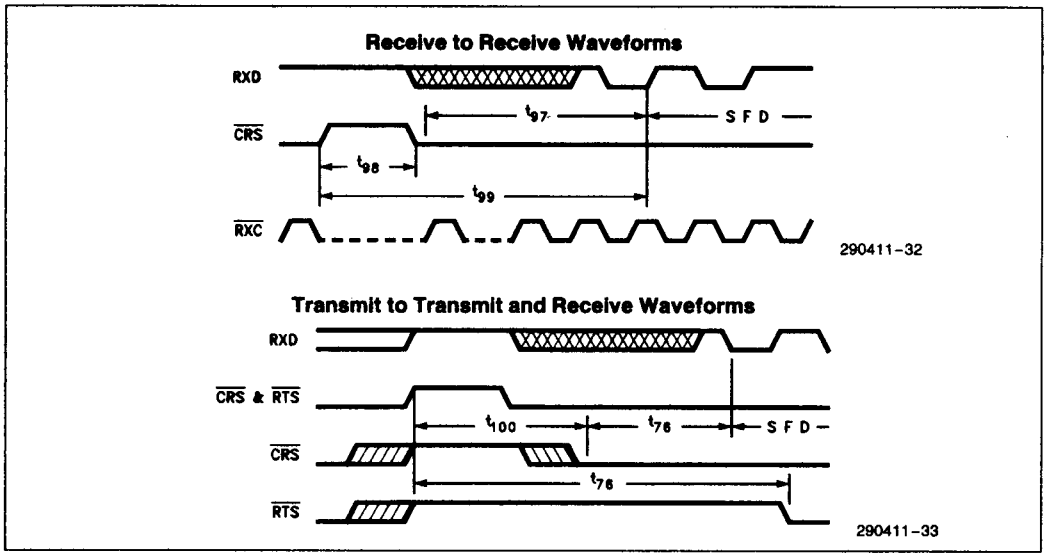


290411-30

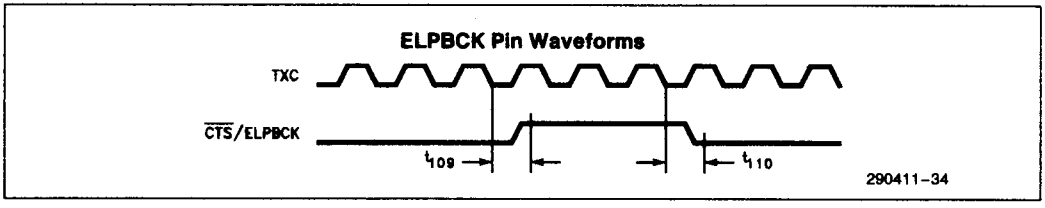


290411-31

Interframe Spacing Timings



External Loopback Timings



SERIAL A.C. TIMING CHARACTERISTIC VALUES

Symbol	Parameter	16 MHz		20 MHz		Units	Notes	ESI
		Min	Max	Min	Max			
TRANSMIT/RECEIVE CLOCK PARAMETERS								
t60	$\overline{RXC}$, $\overline{TXC}$ Cycle	62.5		50		ns	1	B
t61	$\overline{TXC}$ Rise Time		4		5	ns	1	B
t62	$\overline{TXC}$ Fall Time		4		5	ns	1	B
t63	$\overline{TXC}$ High Time	23		19		ns	1	B
t64	$\overline{TXC}$ Low time	23		18		ns	1	B
TRANSMIT DATA PARAMETERS								
t65	TXD Rise Time		10		10	ns	4	B
t66	TXD Fall time		10		10	ns	4	B
t67	$\overline{TXC}$ Low to TXD Valid		30		25	ns	4	I
t94	$\overline{TXC}$ Low to TXD High (At The Transmission End)		30		25	ns	4	I
t94a	TXC Low to TXD High (At The Transmission End)				25	ns	4	A
t67a	TXC Low to TXD Valid				25	ns	4	A
t95	TX Hold after TXC Low			5		ns	4	A
RTS, CTS PARAMETERS								
t72	$\overline{TXC}$ Low to $\overline{RTS}$ Low Time to Activate $\overline{RTS}$		30		25	ns	5	I
t73	$\overline{CTS}$ Low to $\overline{TXC}$ Low $\overline{CTS}$ Setup Time		25		20	ns	2	I
t73a	$\overline{CTS}$ Low to TXC Low $\overline{CTS}$ Setup Time		25		20	ns	2	A
t74	$\overline{TXC}$ Low to $\overline{RTS}$ High		30		25	ns	5	I
t75	$\overline{TXC}$ Low to $\overline{CTS}$ Invalid $\overline{CTS}$ Hold Time			10		ns	7 2	I
t75b	$\overline{CTS}$ High to $\overline{TXC}$ Low $\overline{CTS}$ Setup Time to Stop Trans.	25		20		ns	7 2	I
t72a	TXC Low to TENA High Time to Activate TENA				25	ns	5	A
t74a	TXC Low to TENA Low				25	ns	5	A
t75a	TXC Low to $\overline{CTS}$ Invalid $\overline{CTS}$ Hold Time			10		ns	7 2	A
t96	TENA Hold after TXC Low			5		ns		A

SERIAL A.C. TIMING CHARACTERISTIC VALUES (Continued)

Symbol	Parameter	16 MHz		20 MHz		Units	Notes	ESI
		Min	Max	Min	Max			
CRS, CDT PARAMETERS								
t77	$\overline{CDT}$, Low to $\overline{TXC}$ High External Coll. Detect Setup Time	25		20		ns		I
t78	$\overline{TXC}$ High to $\overline{CDT}$ Inactive $\overline{CDT}$ Hold Time	10		10		ns	14	I
t79	$\overline{CDT}$ Low to Jam Start					ns	10	I
t77a	CLSN High to TXC High External Coll.			20		ns	15	A
t78a	TXC High to CLSN Inactive CLSN Hold time			10		ns	14 15	A
t79a	CLSN High to Jam Start					ns	10, 15	A
t80	Jamming Period					ns	11	B
t81	$\overline{CRS}$ Low to $\overline{TXC}$ High Carrier Sense Setup Time	25		20		ns		I
t82	$\overline{TXC}$ High to $\overline{CRS}$ Inactive $\overline{CRS}$ Hold Time	10		10		ns	14	I
t81a	RENA High to TXC High Carrier Sense Setup time			20		ns	15	A
t82a	TXC High to RENA Inactive RENA Hold Time			10		ns	14	A
t83	$\overline{CRS}$ High to Jamming Start (Internal Collision Detect)					ns	12	B
CRS, CDT PARAMETERS								
t84	$\overline{CRS}$ High to $\overline{RXC}$ High $\overline{CRS}$ Inactive Setup Time	35		30		ns		I
t85	$\overline{RXC}$ High to CRS High $\overline{CRS}$ Inactive Hold Time	10		10		ns		I
t84a	RENA Low to RXC High RENA Inactive Setup Time			10		ns	15	A
t85a	RXC High to RENA Low RENA Inactive Hold Time			10		ns	15	A

SERIAL A.C. TIMING CHARACTERISTIC VALUES (Continued)

Symbol	Parameter	16 MHz		20 MHz		Units	Notes	ESI
		Min	Max	Min	Max			
RECEIVE CLOCK PARAMETERS								
t86	$\overline{RXC}$ Rise Time		4		5	ns	1	B
t87	$\overline{RXC}$ Fall time		4		5	ns	1	B
t88	$\overline{RXC}$ High Time	23		19		ns	1	B
t89	$\overline{RXC}$ Low Time	23		18		ns	1	B
RECEIVE DATA PARAMETERS								
t90	RXD Setup Time	15		15		ns		I
t91	RXD Hold Time	15		15		ns		I
t90a	RX Setup Time	12		12		ns	15	A
t91a	RX Hold Time	10		10		ns	15	A
t92a	RXD Rise Time		10		10	ns		B
t93	RXD Fall Time		10		10	ns		B
EXTERNAL LOOP BACK PIN PARAMETERS								
t109	$\overline{TXC}$/ Low to ELPBCK Valid		35		35	ns	4	B
t110	$\overline{TXC}$/ Low to ELPBCK Float		35		35	ns	4	B

Symbol	Parameter	Min	Max	Units	Notes	ESI
INTERFRAME SPACING PARAMETERS						
t76	Inter Frame Delay				9	B
t97	CRS/RENA to SFD Min	8Trcy	11*T60	ns		B
t98	CRS Inactive to Active		8*T60	ns		B
t99	End of Accepted RCV to Next SFD		34*T60	ns		B
t100	End of Tx to CRS Accepted		42*T60	ns		B

NOTES:
1. MOS levels.
2. CTS and LPBK timings are independent of the polarity of these signals.
4. 1 TTL load + 50 pF.
5. 1 TTL load + 100 pF.
7. Abnormal end to transmission: CTS expires before RTS.
8. Normal end to transmission.
9. Programmable value:
   For non-Foreign Mode: t76 = Nifs x t60 (ns)
   For Foreign Mode: t76 = (Nifs + 1) x t60 (ns)
   Nifs—the IFS configuration value.
10. Programmable value:
    t79 = N_{cdf} x t60 + (12 to 15) x t60 (ns) (if collision occurs after preamble)
    N_{cdf}—the collision detect filter configuration value.
11. t80 = 32 x t60
12. Programmable value:
    t83 = N_{csf} x t60 + (12 to 15) x t60
14. To guarantee recognition on the next clock.
15. For 10 Mb/s SIA, TxC and RxC are both 10 MHz.

ESI—I: INTEL 82C501
A: AMD 7992B (Foreign Mode)
B: Applies to both