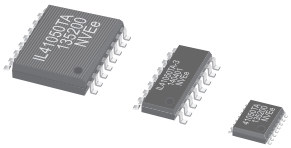
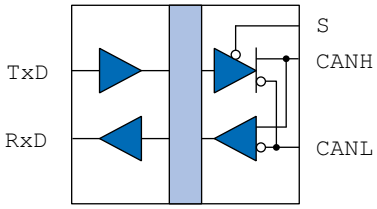
# Isolated CAN FD Transceiver



## Functional Diagram




**IL41050TFD**

| $V_{DD2}$ (V) | TxD[1] | S[2] | CANH | CANL | Bus State | RxD |
|---|---|---|---|---|---|---|
| 4.75 to 5.25 | ↓ | Low | High | Low | Dominant | Low |
| 4.75 to 5.25 | X | High | $V_{DD2}/2$ | $V_{DD2}/2$ | Recessive | High |
| 4.75 to 5.25 | ↑ | X | $V_{DD2}/2$ | $V_{DD2}/2$ | Recessive | High |
| <2V (no pwr) | X | X | 0<V<2.5 | 0<V<2.5 | Recessive | High |
| 2<$V_{DD2}$<4.75 | >2V | X | 0<V<2.5 | 0<V<2.5 | Recessive | High |

**Table 1.** Function table.

**Notes:**
X = don't care.

1. TxD input is edge triggered: ↑ = Logic Lo to Hi, ↓ = Hi to Lo.

2. S-pin has an internal pull-up resistor; unconnected pin will be logic HIGH.

## Features

- Flexible data rate up to 5 Mbps
- 136 ns typical loop delay
- 5 mA typ. quiescent recessive supply current
- −55 °C to +125 °C operating temperature
- 3 V to 5.5 V power supplies
- >110-node fan-out
- 44000 year barrier life
- No carrier or clock for low emissions and EMI susceptibility
- Silent mode to disable transmitter
- Transmit data (TxD) dominant time-out function
- Edge triggered, non-volatile input improves noise performance
- Thermal shutdown protection
- Bus power short-circuit protection
- 2500 $V_{RMS}$ isolation voltage
- VDE V 0884-11 / IEC 60747-17 and UL 1577 pending
- QSOP, 0.15" SOIC, or 0.3" True 8™ mm 16-pin packages

## Applications

- Factory automation
- Battery management systems
- Noise-critical CAN
- DeviceNet

## Description

The IL41050TFD is a galvanically isolated, CAN (Controller Area Network) transceiver, designed as the interface between the CAN protocol controller and the physical bus.

The wide-body version provides true 8 mm creepage. Narrow-body and QSOP packages offer unprecedented miniaturization.

The IL41050 family provides isolated differential transmit capability to the bus and isolated differential receive capability to the CAN controller via NVE's patented* IsoLoop spintronic Giant Magnetoresistance (GMR) technology.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

Advanced features facilitate reliable bus operation. Unpowered nodes do not disturb the bus, and a unique non-volatile programmable power-up feature prevents unstable nodes. The devices also have a hardware-selectable silent mode that disables the transmitter.

Designed for harsh CAN and DeviceNet environments, IL41050TFD transceivers have transmit data dominant time-out, bus pin transient protection, a rugged Charged Device Model ESD rating, thermal shutdown protection, and short-circuit protection. Unique edge-triggered inputs improve noise performance.





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## Absolute Maximum Ratings[1][2]

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Storage temperature | $T_S$ | −55 | | 150 | °C | |
| Junction temperature | $T_J$ | −55 | | 150 | °C | |
| Ambient operating temperature | $T_A$ | −55 | | 125 | °C | |
| DC voltage at CANH and CANL pins | $V_{CANH}$, $V_{CANL}$ | −42 | | 42 | V | 0 V< $V_{DD2}$ < 5.25 V; indefinite duration |
| Supply voltage | $V_{DD1}$, $V_{DD2}$ | −0.3 | | 6 | V | |
| Digital input voltage | $V_{TxD}$, $V_S$ | −0.3 | | $V_{DD}$ + 0.3 | V | |
| Digital output voltage | $V_{RxD}$ | −0.3 | | $V_{DD}$ + 0.3 | V | |
| DC voltage at $V_{REF}$ | $V_{REF}$ | −0.3 | | $V_{DD}$ + 0.3 | V | |
| Transient voltage at CANH or CANL | $V_{trt(CAN)}$ | −150 | | 150 | V | |
| Electrostatic discharge at all pins | $V_{esd}$ | −4000 | | 4000 | V | Human body model |
| Electrostatic discharge at all pins | $V_{esd}$ | −500 | | 500 | V | Machine model? |

## Recommended Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD1}$<br>$V_{DD2}$ | 3.0<br>4.75 | | 5.5<br>5.25 | V | |
| Junction temperature | $T_J$ | −55 | | 140 | °C | |
| Input voltage at any bus terminal (separately or common mode) | $V_{CANH}$<br>$V_{CANL}$ | −12 | | 12 | V | |
| High-level digital input voltage[3][4] | $V_{IH}$ | 2<br>2.4<br>2 | | $V_{DD1}$<br>$V_{DD1}$<br>$V_{DD2}$ | V | $V_{DD1}$ = 3.3 V<br>$V_{DD1}$ = 5 V<br>$V_{DD2}$ = 5 V |
| Low-level digital input voltage[3][4] | $V_{IL}$ | 0 | | 0.8 | V | |
| Digital output current (RxD) | $I_{OH}$ | −8 | | 8 | mA | $V_{DD1}$ = 3.3V to 5V |
| Ambient operating temperature | $T_A$ | −55 | | 125 | °C | |
| Digital input signal rise and fall times | $t_{IR}$, $t_{IF}$ | | | 1 | µs | |
| Fanout | | 110 | | | Nodes | |

## Insulation Specifications

| Parameter | | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| Creepage distance (external) | IL41050TFD-1E (QSOP) | | 3.2 | | | mm | |
| | IL41050TFD-3E (0.15" SOIC) | | 4 | | | | |
| | IL41050TFDE (0.3" SOIC) | | 8.03 | 8.3 | | | Per IEC 60601 |
| Total barrier thickness (internal) | | | 0.012 | 0.013 | | mm | |
| Barrier resistance | | $R_{IO}$ | | $>10^{14}$ | | Ω | 500 V |
| Barrier capacitance | | $C_{IO}$ | | 7 | | pF | f = 1 MHz |
| Leakage current | | | | 0.2 | | $\mu A_{RMS}$ | 240 $V_{RMS}$, 60 Hz |
| Comparative Tracking Index | | CTI | ≥175 | | | V | Per IEC 60112 |
| High voltage endurance (maximum barrier voltage for indefinite life) | AC | $V_{IO}$ | 1000 | | | $V_{RMS}$ | At maximum operating temperature |
| | DC | | 1500 | | | $V_{DC}$ | |
| Barrier life | | | | 44000 | | Years | 100 °C, 1000 $V_{RMS}$, 60% CL activation energy |

## Thermal Characteristics

| Parameter | | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| Junction–Ambient Thermal Resistance | QSOP | $\theta_{JA}$ | | 63 | | °C/W | Soldered to double-sided board; free air |
| | 0.15" SOIC | | | 38 | | | |
| | 0.3" SOIC | | | 31 | | | |
| Junction–Case (Top) Thermal Resistance | QSOP | $\theta_{JT}$ | | 35 | | °C/W | |
| | 0.15" SOIC | | | 21 | | | |
| | 0.3" SOIC | | | 17 | | | |
| Power Dissipation | QSOP | $P_D$ | | | 675 | mW | |
| | 0.15" SOIC | | | | 700 | | |
| | 0.3" SOIC | | | | 800 | | |



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## Safety and Approvals

VDE V 0884-11 / IEC 60747-17 and UL 1577 pending.

## Soldering Profile

Per JEDEC J-STD-020C; MSL=1

## Notes:

1. Absolute Maximum specifications mean the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. All voltages are with respect to network ground except differential I/O bus voltages.
3. The TxD input is edge sensitive. Voltage magnitude of the input signal is specified, but edge rate specifications must also be met.
4. The maximum time allowed for a logic transition at the TxD input is 1 µs.



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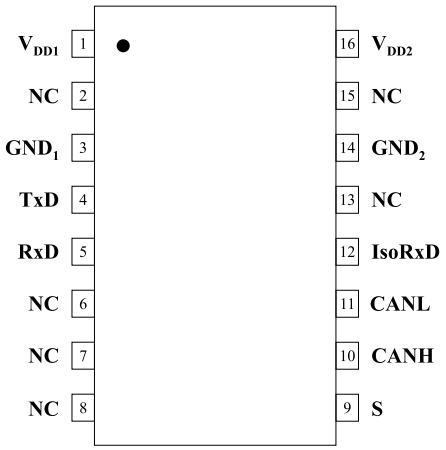
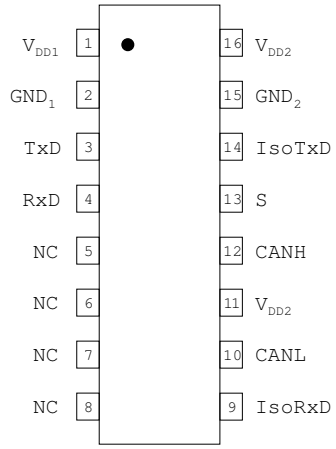
## IL41050TFD-1 Pin Connections (QSOP Package)

| | | |
|---|---|---|
| 1 | $V_{DD1}$ | $V_{DD1}$ power supply input |
| 2 | NC | No internal connection |
| 3 | $GND_1$ | $V_{DD1}$ power supply ground return |
| 4 | TxD | Transmit Data input |
| 5 | RxD | Receive Data output |
| 6 | NC | No internal connection |
| 7 | NC | No internal connection |
| 8 | NC | No internal connection |
| 9 | S | Mode select input. Set low for normal operation; set high or leave open for silent mode. |
| 9 | CANL | Low level CANbus line |
| 10 | CANH | High level CANbus line |
| 12 | IsoRxD | Isolated RxD output (normally not connected). |
| 13 | NC | No internal connection |
| 14 | $GND_2$ | Bus ground |
| 15 | NC | No internal connection |
| 16 | $V_{DD2}$ | Bus power supply input |




## IL41050TFD-3 Pin Connections (0.15" SOIC Package)

| | | |
|---|---|---|
| 1 | $V_{DD1}$ | $V_{DD1}$ power supply input |
| 2 | $GND_1$ | $V_{DD1}$ power supply ground return |
| 3 | TxD | Transmit Data input |
| 4 | RxD | Receive Data output |
| 5 | NC | No internal connection |
| 6 | NC | No internal connection |
| 7 | NC | No internal connection |
| 8 | NC | No internal connection |
| 9 | IsoRxD | Isolated RxD output (normally not connected). |
| 10 | CANL | Low level CANbus line |
| 11 | $V_{DD2}$ | $V_{DD2}$ CAN I/O bus circuitry power supply input* |
| 12 | CANH | High level CANbus line |
| 13 | S | Mode select input. Set low for normal operation; set high or leave open for silent mode. |
| 14 | IsoTxD | Isolated TxD output. No connection should be made to this pin. |
| 15 | $GND_2$ | $V_{DD2}$ power supply ground return |
| 16 | $V_{DD2}$ | $V_{DD2}$ isolation power supply input* |

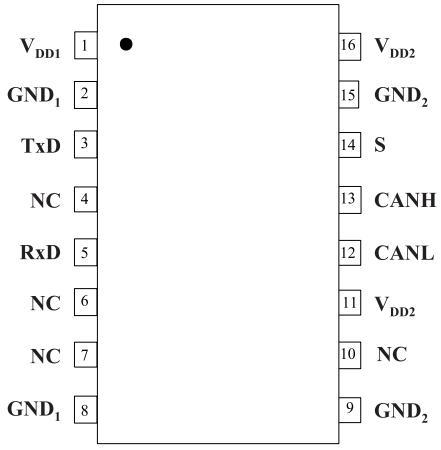



*Pin 11 is not internally connected to pin 16;
both should be connected to the $V_{DD2}$ power supply for normal operation.

### IL41050TFD Pin Connections (0.3" SOIC Package)

| | | |
|---|---|---|
| 1 | $V_{DD1}$ | $V_{DD1}$ power supply input |
| 2 | $GND_1$ | $V_{DD1}$ power supply ground return (pin 2 is internally connected to pin 8) |
| 3 | TxD | Transmit Data input |
| 4 | NC | No internal connection |
| 5 | RxD | Receive Data output |
| 6 | NC | No internal connection |
| 7 | NC | No internal connection |
| 8 | $GND_1$ | $V_{DD1}$ power supply ground return (pin 8 is internally connected to pin 2) |
| 9 | $GND_2$ | $V_{DD2}$ power supply ground return (pin 9 is internally connected to pin 15) |
| 10 | NC | No internal connection |
| 11 | $V_{DD2}$ | $V_{DD2}$ CAN I/O bus circuitry power supply input* |
| 12 | CANL | Low level CANbus line |
| 13 | CANH | High level CANbus line |
| 14 | S | Mode select input. Set low for normal operation; set high or leave open for silent mode. |
| 15 | $GND_2$ | $V_{DD2}$ power supply ground return (pin 15 is internally connected to pin 9) |
| 16 | $V_{DD2}$ | $V_{DD2}$ isolation power supply input* |

*Pin 11 is not internally connected to pin 16;
both should be connected to the $V_{DD2}$ power supply for normal operation.





## Operating Specifications

| **Electrical Specifications** ($T_{min}$ to $T_{max}$ and $V_{DD1}$, $V_{DD2}$= 4.75 V to 5.25 V unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** | **Test Conditions** |
| **Power Supply Current** | | | | | | |
| Quiescent supply current (recessive) | $IQ_{VDD1}$ | 1<br>0.7 | 1.75<br>1.4 | 3<br>2 | mA | dr = 0 bps; $V_{DD1}$ = 5 V<br>dr = 0 bps;$V_{DD1}$ = 3.3 V |
| Dynamic supply current (dominant) | $I_{VDD1}$ | 1.2<br>0.9 | 2<br>1.6 | 3.2<br>2.2 | mA | dr = 1 Mbps, $R_L$= 60Ω; $V_{DD1}$ = 5 V<br>dr = 1 Mbps, $R_L$= 60Ω; $V_{DD1}$ = 3.3 V |
| Quiescent supply current (recessive)<br>Dynamic supply current (dominant) | $IQ_{VDD2}$<br>$I_{VDD2}$ | 2<br>30 | 5<br>45 | 8<br>55 | mA | 0 bps<br>1 Mbps, $R_L$ = 60Ω |
| **Transmitter Data input (TxD)**[1] | | | | | | |
| High level input voltage ↑ | $V_{IH}$ | 2.4 | | 5.25 | V | $V_{DD1}$ = 5 V; recessive |
| High level input voltage ↑ | $V_{IH}$ | 2 | | 3.6 | V | $V_{DD1}$ = 3.3 V; recessive |
| Low level input voltage ↓ | $V_{IL}$ | −0.3 | | 0.8 | V | Output dominant |
| TxD input rise and fall time[2] | $t_r$ | | | 1 | µs | 10% to 90%  |
| High level input current | $I_{IH}$ | −10 | | 10 | µA | $V_{TxD}$ = $V_{DD1}$ |
| Low level input current | $I_{IL}$ | −300 | | −75 | µA | $V_{TxD}$ = 0 V |
| **Mode select input (S)** | | | | | | |
| High level input voltage | $V_{IH}$ | 2 | | $V_{DD2}$ + 0.3 | V | Silent mode |
| Low level input voltage | $V_{IL}$ | −0.3 | | 0.8 | V | High-speed mode |
| High level input current | $I_{IH}$ | −1 | 0 | 1 | µA | $V_S$ = $V_{DD2}$ |
| Low level input current | $I_{IL}$ | −15 | | −1 | µA | $V_S$ = 0 V |
| **Receiver Data output (RxD)** | | | | | | |
| High level output current | $I_{OH}$ | −8 | −3 | −1 | mA | $V_{RxD}$ = 0.8 $V_{DD1}$ |
| Low level output current | $I_{OL}$ | 1 | 6 | 12 | mA | $V_{RxD}$ = 0.45 V |
| **Failsafe supply voltage**[4] | $V_{DD2}$ | 3.5 | 4 | 4.3 | V | |
| **Bus lines (CANH and CANL)** | | | | | | |
| Recessive voltage at CANH pin | $V_{O(reces)}$ CANH | 2 | 2.5 | 3 | V | $V_{TxD}$ = $V_{DD1}$, no load |
| Recessive voltage at CANL pin | $V_{O(reces)}$ CANL | 2 | 2.5 | 3 | V | $V_{TxD}$ = $V_{DD1}$, no load |
| Recessive current at CANH pin | $I_{O(reces)}$ CANH | −2.5 | | +2.5 | mA | −27V < $V_{CANH}$< +32V; 0V < $V_{DD2}$<5.25V |
| Recessive current at CANL pin | $I_{O(reces)}$ CANL | −2.5 | | +2.5 | mA | −27V < $V_{CANL}$ < +32V; 0 V <$V_{DD2}$ < 5.25V |
| Dominant voltage at CANH pin | $V_{O(dom)}$ CANH | 3 | 3.6 | 4.25 | V | $V_{TxD}$ = 0 V |
| Dominant voltage at CANL pin | $V_{O(dom)}$ CANL | 0.5 | 1.4 | 1.75 | V | $V_{TxD}$ = 0 V |
| Differential bus input voltage ($V_{CANH}$ − $V_{CANL}$) | $V_{i(dif)(bus)}$ | 1.5 | 2.25 | 3 | V | $V_{TxD}$ = 0 V; dominant 42.5 Ω < $R_L$ < 60 Ω |
| | | −50 | 0 | +50 | mV | $V_{TxD}$ = $V_{DD1}$; recessive; no load |
| Short-circuit output current at CANH | $I_{O(sc)}$ CANH | −100 | −70 | −1 | mA | $V_{CANH}$ = 0 V, $V_{TxD}$ = 0 |
| Short-circuit output current at CANL | $I_{O(sc)}$ CANL | −1 | 70 | 100 | mA | $V_{CANL}$ = 36 V, $V_{TxD}$ = 0 |
| Differential receiver threshold voltage | $V_{i(dif)(th)}$ | 0.5 | 0.7 | 0.9 | V | −5 V <$V_{CANL}$< +10 V; −5 V <$V_{CANH}$< +10 V |
| Differential receiver input voltage hysteresis | $V_{i(dif)(hys)}$ | 50 | 70 | 100 | mV | −5 V <$V_{CANL}$< +10 V; −5 V <$V_{CANH}$< +10 V |
| Common Mode input resistance at CANH | $R_{i(CM)(CANH)}$ | 15 | 25 | 37 | kΩ | |
| Common Mode input resistance at CANL | $R_{i(CM)(CANL)}$ | 15 | 25 | 37 | kΩ | |
| Matching between Common Mode input resistance at CANH, CANL | $R_{i(CM)(m)}$ | −1 | 0 | +1 | % | $V_{CANL}$ = $V_{CANH}$ = 5V |

| **Electrical Specifications** ($T_{min}$ to $T_{max}$ and $V_{DD1}$, $V_{DD2}$= 4.5 V to 5.5 V unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** | **Test Conditions** |
| **Bus lines** (….cont) | | | | | | |
| Differential input resistance | $R_{i(diff)}$ | 25 | 50 | 75 | kΩ | |
| Input capacitance, CANH | $C_{i(CANH)}$ | | 7.5 | 20 | pF | $V_{TxD} = V_{DD1}$ |
| Input capacitance, CANL | $C_{i(CANL)}$ | | 7.5 | 20 | pF | $V_{TxD} = V_{DD1}$ |
| Differential input capacitance | $C_{i(dif)}$ | | 3.75 | 10 | pF | $V_{TxD} = V_{DD1}$ |
| Input leakage current at CANH | $I_{LI(CANH)}$ | −5 | 0 | 5 | µA | $V_{CANH}$= 5 V, $V_{DD2}$= 0 |
| Input leakage current at CANL | $I_{LI(CANL)}$ | −5 | 0 | 5 | µA | $V_{CANL}$= 5 V, $V_{DD2}$= 0 |
| **Thermal Shutdown** | | | | | | |
| Shutdown junction temperature | $T_{i(SD)}$ | 155 | 165 | 180 | °C | |

| **Timing Characteristics** (60 Ω / 100 pF bus loading; 20 pF RxD load; see Fig. 1) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** | **Test Conditions** |
| TxD to bus active delay | $t_{d(TxD-BUSon)}$ | | 83<br>83 | 100<br>100 | ns | $V_S$= 0 V; $V_{DD1}$ = 5 V<br>$V_S$ = 0 V; $V_{DD1}$ = 3.3 V |
| TxD to bus inactive delay | $t_{d(TxD-BUSoff)}$ | | 67<br>70 | 100<br>100 | ns | $V_S$ = 0 V; $V_{DD1}$ = 5 V<br>$V_S$ = 0 V; $V_{DD1}$ = 3.3 V |
| Bus active to RxD delay | $t_{d(BUSon-RxD)}$ | | 26<br>28 | 100<br>100 | ns | $V_S$ = 0 V; $V_{DD1}$ = 5 V<br>$V_S$ = 0 V; $V_{DD1}$ = 3.3 V |
| Bus inactive to RxD delay | $t_{d(BUSoff-RxD)}$ | | 51<br>55 | 100<br>100 | ns | $V_S$ = 0 V; $V_{DD1}$ = 5 V<br>$V_S$ = 0 V; $V_{DD1}$ = 3.3 V |
| Loop delay<br>low-to-high or high-to-low | $T_{LOOP}$ | | 136 | 200 | ns | $V_S$ = 0 V; "Typ." at 25°C and nominal loads |
| TxD dominant time for timeout | $T_{dom(TxD)}$ | 1 | - | 10 | ms | $V_{TxD}$ = 0 V<br>3.0 V > $V_{DD1}$ < 5.5 V |
| Common Mode Transient Immunity (TxD Logic High or Logic Low) | $\|CM_H\|,\|CM_L\|$ | 30 | 50 | | kV/µs | $R_L$ = 60 Ω;<br>$V_{CM}$ = 1500 $V_{DC}$;<br>$t_{TRANSIENT}$ = 25 ns |

| **Magnetic Field Immunity**(3) ($V_{DD2}$= 5V, 3V<$V_{DD1}$<5.5V) | | | | | | |
|---|---|---|---|---|---|---|
| Power Frequency Magnetic Immunity | $H_{PF}$ | | 6000 | | A/m | 50Hz/60Hz |
| Pulse Magnetic Field Immunity | $H_{PM}$ | | 7000 | | A/m | $t_p$ = 8 µs |
| Damped Oscillatory Magnetic Field | $H_{OSC}$ | | 7000 | | A/m | 0.1 Hz – 1 MHz |
| Cross-axis Immunity Multiplier | $K_X$ | | 2 | | | See Fig. 4 |

## Notes:

1. The TxD input is edge sensitive. Voltage magnitude of the input signal is specified, but edge rate specifications must also be met.
2. The maximum time allowed for a logic transition at the TxD input is 1 µs.
3. Test and measurement methods are given in the Electromagnetic Compatibility section on p. 10.
4. If $V_{DD2}$ falls below the specified failsafe supply voltage, RxD,TxD,S will go High-z.



## Timing Test Circuit

Timing parameters are measured with 60 Ω / 100 pF bus line loading and 20 pF on RxD as shown in Figure 1 below:

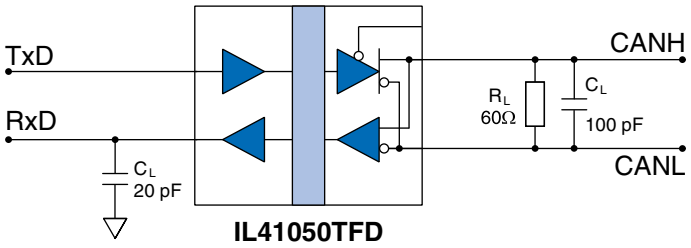



**Figure 1. Timing characteristics test circuit.**

## Block Diagram

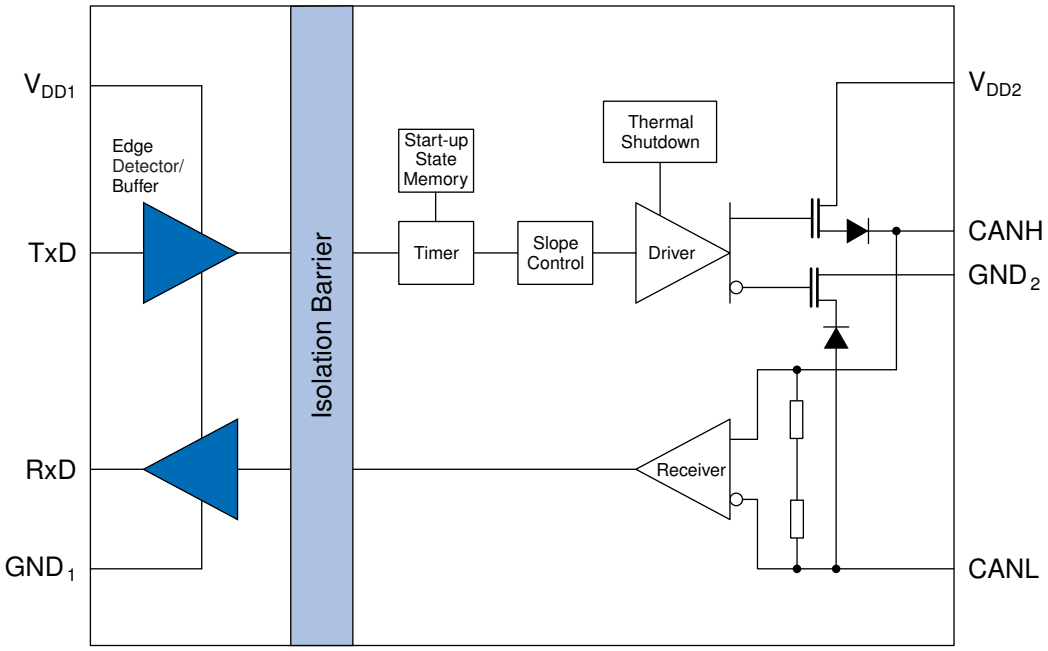



**Figure 2. IL41050TFD detailed functional diagram.**

## Application Information

As Figure 3 shows, the IL41050TFD can provide isolation and level shifting between a 5 volt CAN bus and a 3.3-volt microcontroller:

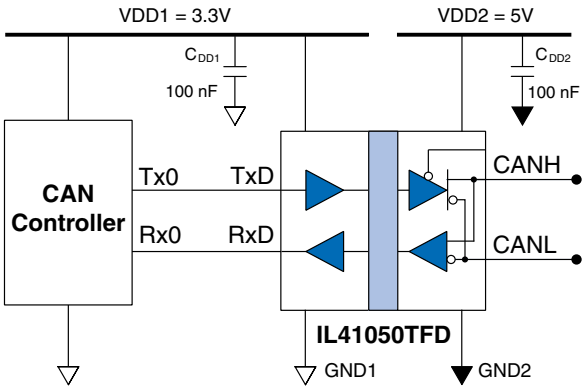



**Figure 3. Isolated CAN node using an IL41050TFD.**

### Bus-Side Power Supply Pins

On the 0.3" SOIC version, both $V_{DD2}$ power supply inputs (pins 11 and 16) must be connected to the bus-side power supply. On some parts the CAN I/O circuitry and bus-side isolation circuitry power are separated for testing purposes. The part may not operate without both pins powered, and operation without both pins powered can cause damage.

### Power Supply Decoupling

Both $V_{DD1}$ and $V_{DD2}$ must be bypassed with 0.1 µF ceramic capacitors. These supply the dynamic current required for the isolator switching and should be placed as close as possible to $V_{DD}$ and their respective ground return pins.

### Maintaining Creepage

Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

### Input Configurations

The TxD input should not be left open as the state will be indeterminate. If connected to an open-drain or open collector output, a pull-up resistor (typically 16 kΩ) should be connected from the input to $V_{DD1}$.

### Dominant Mode Time-out and Failsafe Receiver Functions

CAN bus latch up is prevented by an integrated Dominant mode timeout function. If the TxD pin is forced permanently low by hardware or software application failure, the time-out returns the RxD output to the high state no more than 10 ms after TxD is asserted dominant. The timer is triggered by a negative edge on TxD. If the duration of the low is longer than the internal timer value, the transmitter is disabled, driving the bus to the recessive state. The timer is reset by a positive edge on pin TxD.

If power is lost on Vdd2, the IL41050TFD asserts the RxD output high when the supply voltage falls below 3.8 V. RxD will return to normal operation when Vdd2 rises above approximately 4.2 V.

### Programmable Power-Up

A unique non-volatile programmable power-up feature prevents unstable nodes. A state that needs to be present at node power up can be programmed at the last power down. For example if a CAN node is required to “pulse” dominant at power up, TxD can be sent low by the controller immediately prior to power down. When power is resumed, the node will immediately go dominant allowing self-check code in the microcontroller to verify node operation. If desired, the node can also power up silently by presetting the TxD line high at power down. At the next power on, the IL41050TFD will remain silent, awaiting a dominant state from the bus.

The microcontroller can check that the CAN node powered down correctly before applying power at the next “power on” request. If the node powered down as intended, RxD will be set high and stored in the IL41050TFD’s non-volatile memory. The level stored in the RxD bit can be read before isolated node power is enabled, avoiding possible CAN bus disruption due to an unstable node.

## Replacing Non-Isolated Transceivers

The IL41050TFD is designed to replace common non-isolated CAN transceivers such as the NXP TJF1051 with minimal circuit changes. Some notable differences:

- Some non-isolated CAN transceivers have internal TxD pull-up resistors, but the IL41050TFD TxD input should not be left open. If connected to an open-drain or open collector output, a pull-up resistor (typically 16 kΩ) should be connected from the input to $V_{DD1}$.

- Initialization behavior varies between CAN transceivers. To ensure the desired power-up state, the IL41050TFD should be initialized with a TxD pulse (low-to-high for recessive initialization), or shut down the transceiver in the desired power-up state (the "programmable power-up feature").

- Many non-isolated CAN transceivers have a $V_{REF}$ output. Such a reference is available on the IL41050 wide-body version.

## IsoRxD / IsoTxD Outputs

The IsoRxD and IsoTxD outputs are isolated versions of the RxD and TxD signals. These outputs are provided for troubleshooting on the QSOP and narrow-body versions, but normally no connections should be made to the pins.

## The Isolation Advantage

Battery fire caused by over or under charging of individual lithium ion cells is a major concern in multi-cell high voltage electric and hybrid vehicle batteries. To combat this, each cell is monitored for current flow, cell voltage, and in some advanced batteries, magnetic susceptibility. The IL41050TFD allows seamless connection of the monitoring electronics of every cell to a common CAN bus by electrically isolating inputs from outputs, effectively isolating each cell from all other cells. Cell status is then monitored via the CAN controller in the Battery Management System (BMS).

Another major advantage of isolation is the tremendous increase in noise immunity it affords the CAN node, even if the power source is a battery. Inductive drives and inverters can produce transient swings in excess of 20 kV/µs. The traditional, non-isolated CAN node provides some protection due to differential signaling and symmetrical driver/receiver pairs, but the IL41050TFD typically provides more than twice the dV/dt protection of a traditional CAN node.



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Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

## Electromagnetic Compatibility

The IL41050TFD is fully compliant with IEC 61000-6-1 and IEC 61000-6-2 standards for immunity, and IEC 61000-6-3, IEC 61000-6-4, CISPR, and FCC Class A standards for emissions.

Immunity to external magnetic fields is higher if the field direction is “end-to-end” (rather than to “pin-to-pin”) as shown in the diagram below:

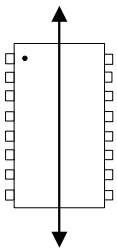

**Figure 4. Orientation for high field immunity.**



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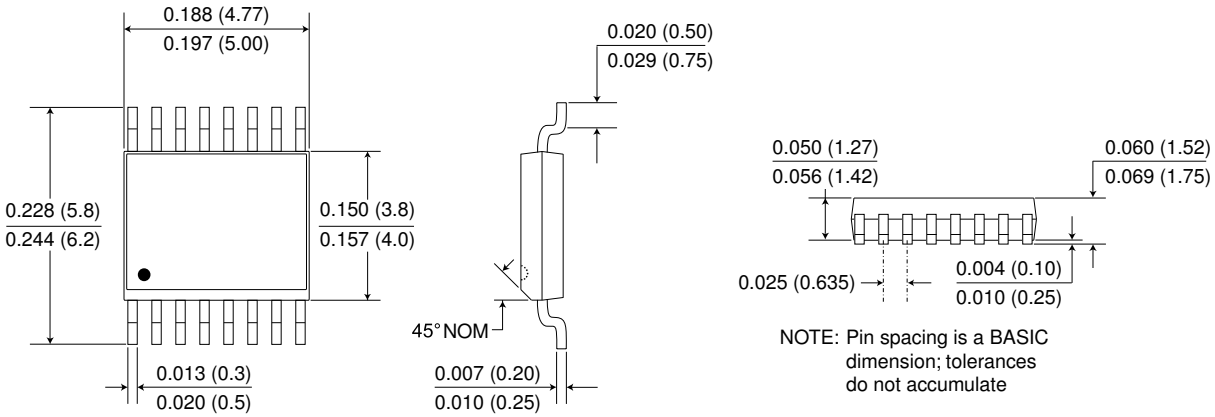
## Package Drawings

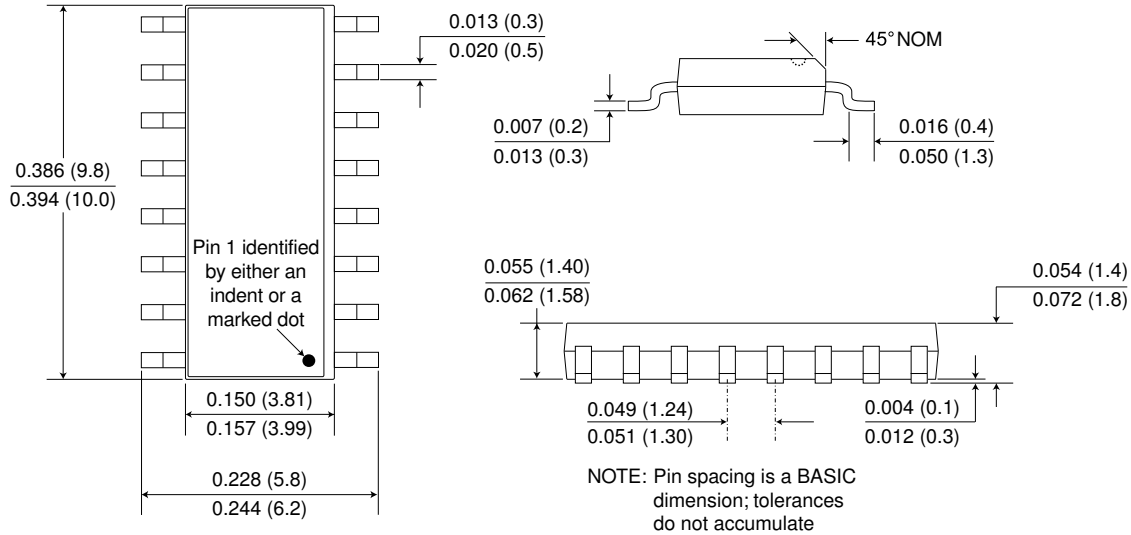
### **Ultraminiature 16-pin QSOP Package** (-1 suffix)

Dimensions in inches (mm); scale = approx. 5X




### **0.15" 16-pin SOIC Package** (-3 suffix)

Dimensions in inches (mm); scale = approx. 5X

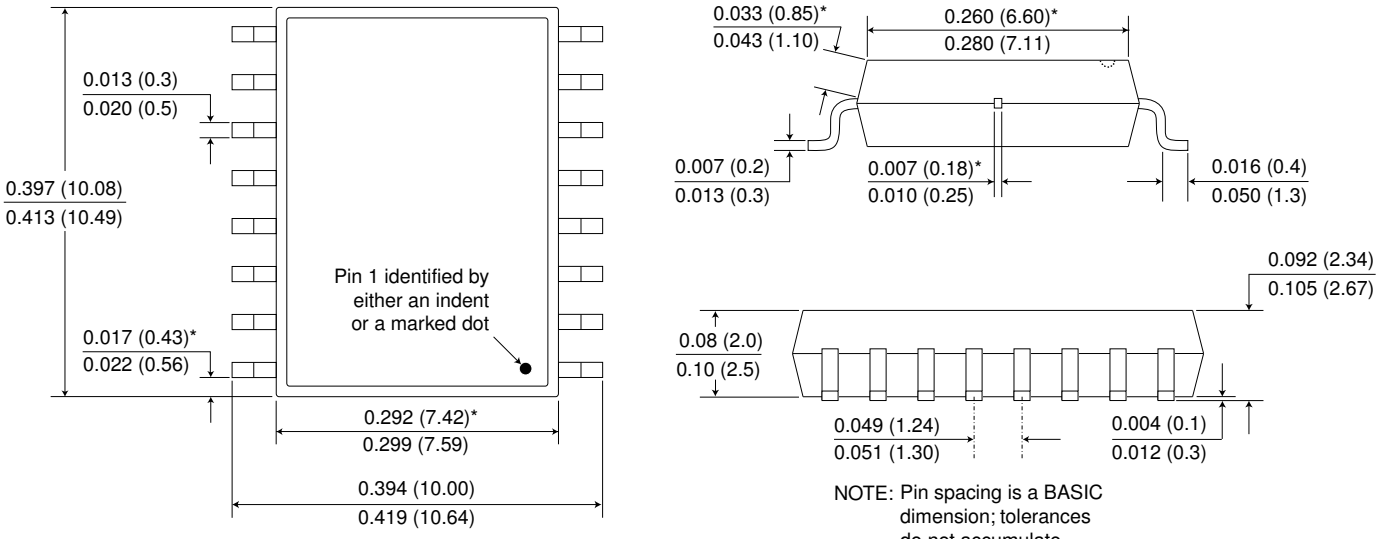




**0.3" 16-pin SOIC Package** (no suffix)

Dimensions in inches (mm); scale = approx. 5X




NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.

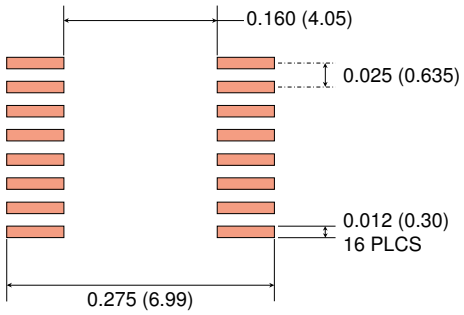


## Recommended Pad Layouts

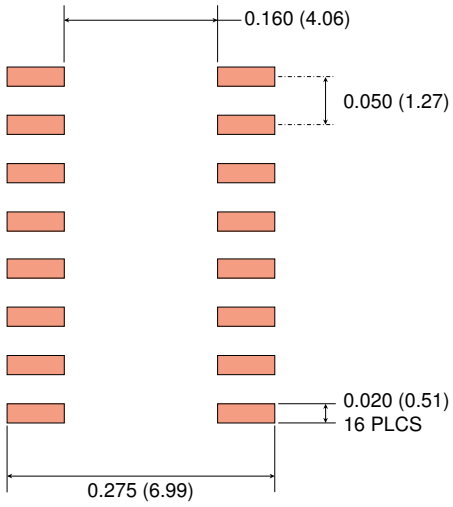
### 4 mm x 5 mm 16-pin QSOP Pad Layout

Dimensions in inches (mm); scale = approx. 5X




### 0.15" 16-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



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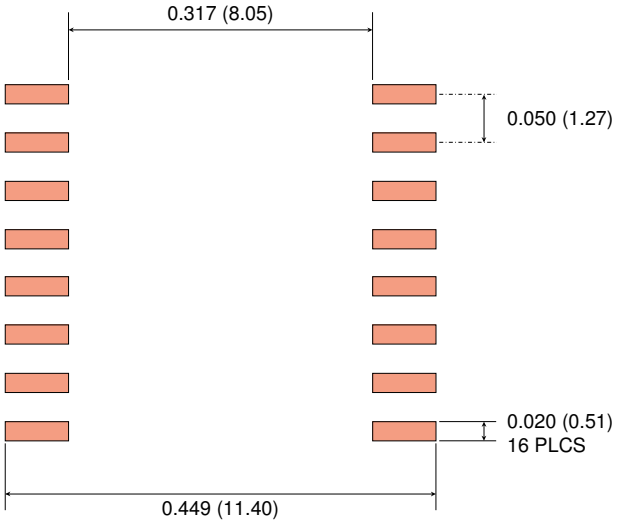
## 0.3" 16-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X





## Ordering Information and Valid Part Numbers

IL 4 1050 T FD-3 E TR13

**Bulk Packaging**
Blank = Tube (50 pcs)

TR7 = 7" Tape and Reel
(800 pcs 0.15" SOIC or
1000 pcs QSOP)

TR13 = 13" Tape and Reel
(1500 pcs 0.3" SOIC,
3000 pcs 0.15" SOIC, or
5000 pcs QSOP)

**Package**
E = RoHS Compliant

**Package Type**
Blank = 0.3" SOIC
-3 = 0.15" SOIC
-1 = 0.15" QSOP

**Part Subtype**
FD = Flexible data rate

**Temperature Range**
T = Extended
(-55°C to +125°C)

**Channel Configuration**
1050 = CAN Transceiver

**Base Part Number**
4 = Isolated Transceiver

**Product Family**
IL = Isolators

**Valid Part Numbers**
IL41050TFD
IL41050TFD TR13
IL41050TFD-3E
IL41050TFD-3E TR7
IL41050TFD-3E TR13
IL41050TFD-1E
IL41050TFD-1E TR7
IL41050TFD-1E TR13

RoHS COMPLIANT



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## Revision History

**ISB-DS-001-IL41050TFD-RevA**
**August 2019**

### Changes

- Initial release.

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ISB-DS-001-IL41050TFD-A

*August 2019*