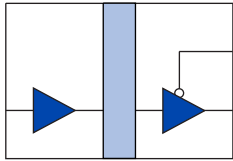
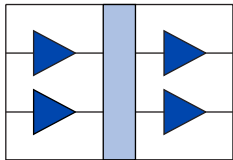


## DC-Correct High Speed Digital Isolators

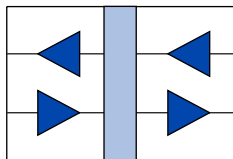
### Functional Diagrams



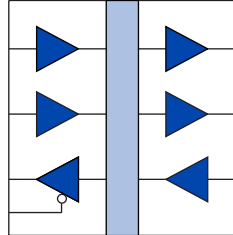
IL810



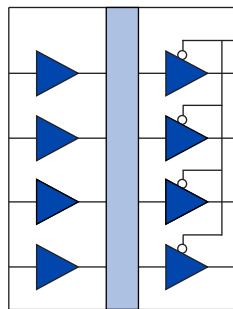
IL811



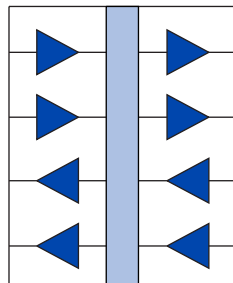
IL821



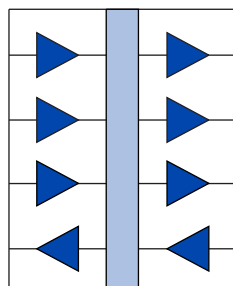
IL814



IL815



IL816



IL817

### Features

- DC-correct
- -40°C to 125°C operating temperature
- 110 Mbps
- 10 ns propagation delay
- 1.3 mA/channel typical quiescent current
- 50 kV/μs typ.; 30 kV/μs min. common mode transient immunity
- 600 V<sub>RMS</sub> working voltage per VDE 0884
- 44000 year barrier life
- 3 V to 5 V power supplies
- Low EMC footprint
- 8-pin MSOP and SOIC packages for one and two channels
- 16-pin QSOP, 0.15" SOIC, and 0.3" True 8™ SOIC for 3 and 4 channels
- IEC 60747-5-5 (VDE 0884) certified; UL 1577 recognized

### Applications

- ADCs and DACs
- Digital Fieldbus
- RS-485 and RS-422
- Multiplexed data transmission
- Data interfaces
- Board-to-board communication
- Digital noise reduction
- Ground loop elimination
- Peripheral interfaces
- Parallel bus
- Logic level shifting

### Description

IL800-Series isolators are high-speed, high temperature dc-correct isolators. An internal refresh clock ensures the outputs respond to dc states on inputs within a maximum of 9 μs.

The devices use NVE's patented\* IsoLoop® spintronic Giant Magnetoresistive (GMR) technology.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

## Absolute Maximum Ratings<sup>(1)</sup>

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	$T_S$	-55		150	°C	
Ambient Operating Temperature	$T_A$	-40		125	°C	
Supply Voltage	$V_{DD1}, V_{DD2}$	-0.5		7	V	
Input Voltage	$V_I$	-0.5		$V_{DD}+0.5$	V	
Output Voltage	$V_O$	-0.5		$V_{DD}+0.5$	V	
Output Current Drive	$I_O$			10	mA	
Lead Solder Temperature				260	°C	10 sec.
ESD			2		kV	HBM

## Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Ambient Operating Temperature	$T_A$	-40		125	°C	
Supply Voltage	$V_{DD1}, V_{DD2}$	3.0		5.5	V	
Logic High Input Voltage	$V_{IH}$	2.4		$V_{DD}$	V	
Logic Low Input Voltage	$V_{IL}$	0		0.8	V	
Input Signal Rise and Fall Times <sup>(10)</sup>	$t_{IR}, t_{IF}$		DC-Correct			

## Insulation Specifications

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage Distance (external)	MSOP QSOP 0.15" SOIC (8 or 16 pin) 0.3" SOIC	3.0 4.03 4.03 8.03	8.3		mm	Per IEC 60601
Total Barrier Thickness (internal)		0.012	0.013		mm	
Leakage Current			0.2		μA	240 $V_{RMS}$ , 60 Hz
Barrier Resistance	$R_{IO}$		$>10^{14}$		Ω	500 V
Barrier Capacitance	$C_{IO}$		4		pF	f = 1 MHz
Comparative Tracking Index	CTI	≥175			V	Per IEC 60112
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	AC DC	$V_{IO}$	1000 1500		$V_{RMS}$ $V_{DC}$	At maximum operating temperature
Barrier Life			44000		Years	100°C, 1000 $V_{RMS}$ , 60% CL activation energy

## Thermal Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Junction-Ambient Thermal Resistance	$\theta_{JA}$		60 60 60		°C/W	Soldered to double-sided board; free air
Junction-Case (Top) Thermal Resistance	$\Psi_{JT}$		10 10 20		°C/W	
Power Dissipation	$P_D$			675 700 800	mW	

## Safety and Approvals

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**IEC 60747-5-5 (VDE 0884)** (File Number 5016933-4880-0001)

- Working Voltage ( $V_{IORM}$ ) 600  $V_{RMS}$  (848  $V_{PK}$ ); basic insulation; pollution degree 2
- Transient overvoltage ( $V_{IOTM}$ ) and surge voltage ( $V_{IOSM}$ ) 4000  $V_{PK}$
- Each part tested at 1590  $V_{PK}$  for 1 second, 5 pC partial discharge limit
- Samples tested at 4000  $V_{PK}$  for 60 sec.; then 1358  $V_{PK}$  for 10 sec. with 5 pC partial discharge limit

**IEC 61010-1** (Edition 2; TUV Certificate Numbers N1502812; N1502812-101)

Reinforced Insulation; Pollution Degree II; Material Group III

Part No. Suffix	Package	Working Voltage
-1	MSOP/QSOP	150 $V_{RMS}$
-3	SOIC	150 $V_{RMS}$
None	Wide-body SOIC/True 8 <sup>TM</sup>	300 $V_{RMS}$

**UL 1577** (Component Recognition Program File Number E207481)

Each part tested at 3000  $V_{RMS}$  (4240  $V_{PK}$ ) for 1 second; each lot sample tested at 2500  $V_{RMS}$  (3530  $V_{PK}$ ) for 1 minute

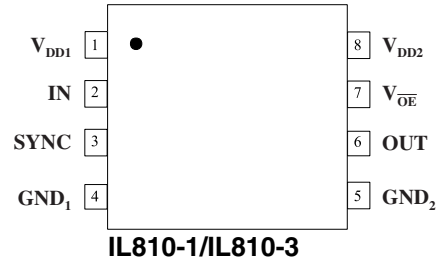
## Soldering Profile

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Per JEDEC J-STD-020C, MSL 1

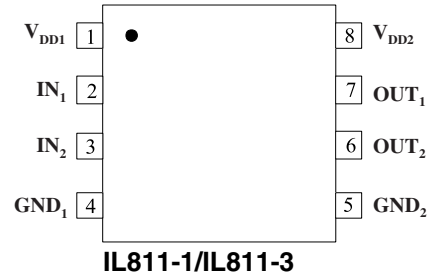
### IL810-1/IL810-3 Pin Connections

1	V <sub>DD1</sub>	Supply voltage
2	IN	Data in
3	SYNC	Internal refresh clock disable (normally enabled and internally held low with 10 kΩ)
4	GND <sub>1</sub>	Ground return for V <sub>DD1</sub>
5	GND <sub>2</sub>	Ground return for V <sub>DD2</sub>
6	OUT	Data out
7	V <sub>OE</sub>	Output enable (internally held low with 100 kΩ)
8	V <sub>DD2</sub>	Supply voltage



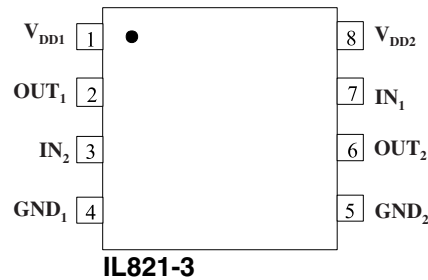
### IL811-1/IL811-3 Pin Connections

1	V <sub>DD1</sub>	Supply voltage
2	IN <sub>1</sub>	Data in, channel 1
3	IN <sub>2</sub>	Data in, channel 2
4	GND <sub>1</sub>	Ground return for V <sub>DD1</sub>
5	GND <sub>2</sub>	Ground return for V <sub>DD2</sub>
6	OUT <sub>2</sub>	Data out, channel 2
7	OUT <sub>1</sub>	Data out, channel 1
8	V <sub>DD2</sub>	Supply voltage



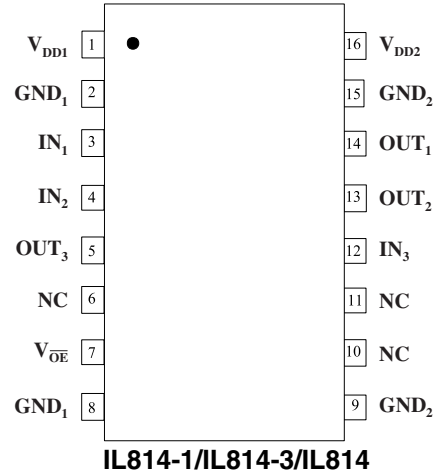
### IL821-3 Pin Connections

1	V <sub>DD1</sub>	Supply voltage
2	OUT <sub>1</sub>	Data out, channel 1
3	IN <sub>2</sub>	Data in, channel 2
4	GND <sub>1</sub>	Ground return for V <sub>DD1</sub>
5	GND <sub>2</sub>	Ground return for V <sub>DD2</sub>
6	OUT <sub>2</sub>	Data out, channel 2
7	IN <sub>1</sub>	Data in, channel 1
8	V <sub>DD2</sub>	Supply voltage



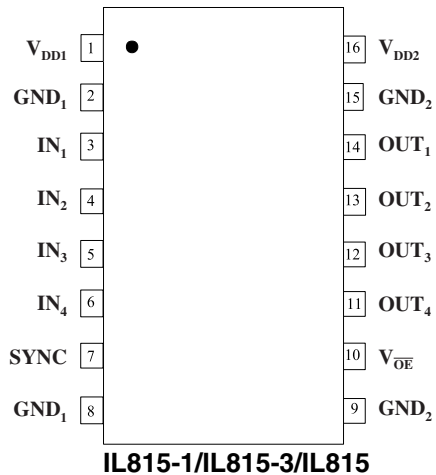
## IL814-1/IL814-3/IL814 Pin Connections

1	V <sub>DD1</sub>	Supply voltage 1
2	GND <sub>1</sub>	Ground return for V <sub>DD1</sub> (pin 2 internally connected to pin 8)
3	IN <sub>1</sub>	Data in, channel 1
4	IN <sub>2</sub>	Data in, channel 2
5	OUT <sub>3</sub>	Data out, channel 3
6	NC	No connection
7	V <sub>OE</sub>	Output enable, channel 3 (internally held low with 100 kΩ)
8	GND <sub>1</sub>	Ground return for V <sub>DD1</sub> (pin 8 internally connected to pin 2)
9	GND <sub>2</sub>	Ground return for V <sub>DD2</sub> (pin 9 internally connected to pin 15)
10	NC	No connection
11	NC	No connection
12	IN <sub>3</sub>	Data in, channel 3
13	OUT <sub>2</sub>	Data out, channel 2
14	OUT <sub>1</sub>	Data out, channel 1
15	GND <sub>2</sub>	Ground return for V <sub>DD2</sub> (pin 15 internally connected to pin 9)
16	V <sub>DD2</sub>	Supply voltage



## IL815-1/IL815-3/IL815 Pin Connections

1	V <sub>DD1</sub>	Supply voltage
2	GND <sub>1</sub>	Ground return for V <sub>DD1</sub> (pin 2 internally connected to pin 8)
3	IN <sub>1</sub>	Data in, channel 1
4	IN <sub>2</sub>	Data in, channel 2
5	IN <sub>3</sub>	Data in, channel 3
6	IN <sub>4</sub>	Data in, channel 4
7	SYNC*	Internal refresh clock disable (normally enabled and internally held low with 10 kΩ)
8	GND <sub>1</sub>	Ground return for V <sub>DD1</sub> (pin 8 internally connected to pin 2)
9	GND <sub>2</sub>	Ground return for V <sub>DD2</sub> (pin 9 internally connected to pin 15)
10	V <sub>OE</sub> *	Output enable for all outputs (internally held low with 100 kΩ)
11	OUT <sub>4</sub>	Data out, channel 4
12	OUT <sub>3</sub>	Data out, channel 3
13	OUT <sub>2</sub>	Data out, channel 2
14	OUT <sub>1</sub>	Data out, channel 1
15	GND <sub>2</sub>	Ground return for V <sub>DD2</sub> (pin 15 internally connected to pin 9)
16	V <sub>DD2</sub>	Supply voltage

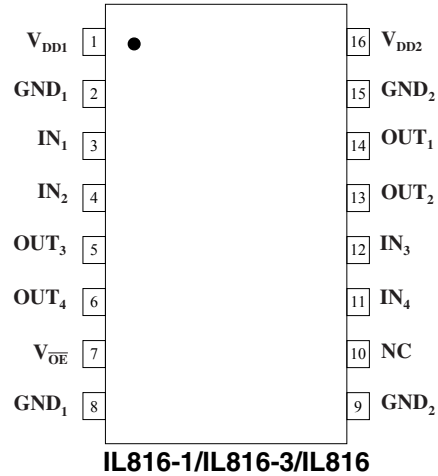


\*Wide-body version (IL815TE) only.

No internal connections to pins 7 or 10 in QSOP or narrow-body (IL815T-1E or IL815T-3E) versions.

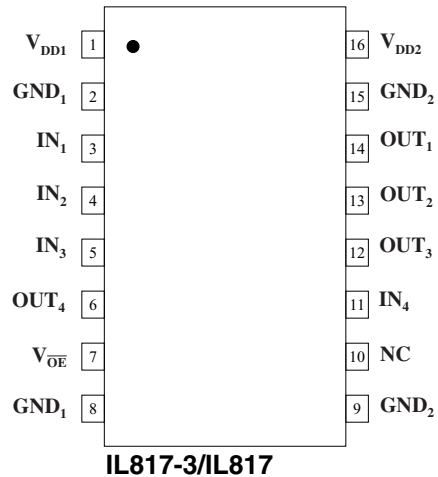
## IL816-1/IL816-3/IL816 Pin Connections

1	V <sub>DD1</sub>	Supply voltage
2	GND <sub>1</sub>	Ground return for V <sub>DD1</sub> (pin 2 internally connected to pin 8)
3	IN <sub>1</sub>	Data in, channel 1
4	IN <sub>2</sub>	Data in, channel 2
5	OUT <sub>3</sub>	Data out, channel 3
6	OUT <sub>4</sub>	Data out, channel 4
7	V <sub>OE</sub>	Output enable, channels 3 and 4 (internally held low with 100 kΩ)
8	GND <sub>1</sub>	Ground return for V <sub>DD1</sub> (pin 8 internally connected to pin 2)
9	GND <sub>2</sub>	Ground return for V <sub>DD2</sub> (pin 9 internally connected to pin 15)
10	NC	No connection
11	IN <sub>4</sub>	Data in, channel 4
12	IN <sub>3</sub>	Data in, channel 3
13	OUT <sub>2</sub>	Data out, channel 2
14	OUT <sub>1</sub>	Data out, channel 1
15	GND <sub>2</sub>	Ground return for V <sub>DD2</sub> (pin 15 internally connected to pin 9)
16	V <sub>DD2</sub>	Supply voltage



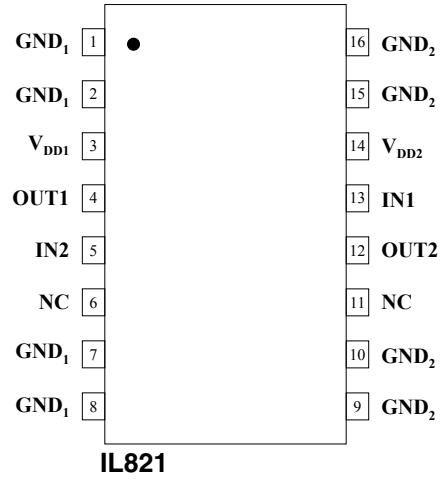
## IL817-3/IL817 Pin Connections

1	V <sub>DD1</sub>	Supply voltage
2	GND <sub>1</sub>	Ground return for V <sub>DD1</sub> (pin 2 internally connected to pin 8)
3	IN <sub>1</sub>	Data in, channel 1
4	IN <sub>2</sub>	Data in, channel 2
5	IN <sub>3</sub>	Data in, channel 3
6	OUT <sub>4</sub>	Data out, channel 4
7	V <sub>OE</sub>	Output enable, channel 4 (internally held low with 100 kΩ)
8	GND <sub>1</sub>	Ground return for V <sub>DD1</sub> (pin 8 internally connected to pin 2)
9	GND <sub>2</sub>	Ground return for V <sub>DD2</sub> (pin 9 internally connected to pin 15)
10	NC	No connection
11	IN <sub>4</sub>	Data in, channel 4
12	OUT <sub>3</sub>	Data out, channel 3
13	OUT <sub>2</sub>	Data out, channel 2
14	OUT <sub>1</sub>	Data out, channel 1
15	GND <sub>2</sub>	Ground return for V <sub>DD2</sub> (pin 15 internally connected to pin 9)
16	V <sub>DD2</sub>	Supply voltage

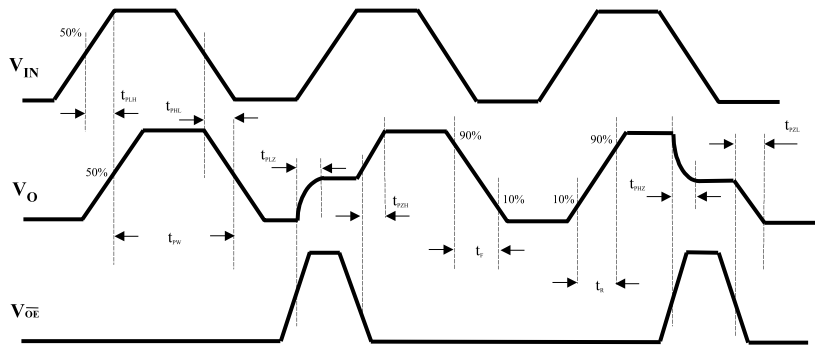


## IL821 Pin Connections

1	GND <sub>1</sub>	Ground return for V <sub>DD1</sub>
2	GND <sub>1</sub>	(pins 1, 2, 7, and 8 internally connected)
3	V <sub>DD1</sub>	Supply voltage
4	OUT <sub>1</sub>	Data out, channel 1
5	IN <sub>2</sub>	Data in, channel 2
6	NC	No connection
7	GND <sub>1</sub>	Ground return for V <sub>DD1</sub>
8	GND <sub>1</sub>	(pins 1, 2, 7, and 8 internally connected)
9	GND <sub>2</sub>	Ground return for V <sub>DD2</sub>
10	GND <sub>2</sub>	(pins 9, 10, 15, and 16 internally connected)
11	NC	No connection
12	OUT <sub>2</sub>	Data out, channel 2
13	IN <sub>1</sub>	Data in, channel 1
14	V <sub>DD2</sub>	Supply voltage
15	GND <sub>2</sub>	Ground return for V <sub>DD2</sub>
16	GND <sub>2</sub>	(pins 9, 10, 15, and 16 internally connected)



## Timing Diagrams



### Legend

$t_{PLH}$	Propagation Delay, Low to High
$t_{PHL}$	Propagation Delay, High to Low
$t_{PW}$	Minimum Pulse Width
$t_{PLZ}$	Propagation Delay, Low to High Impedance
$t_{PZH}$	Propagation Delay, High Impedance to High
$t_{PHZ}$	Propagation Delay, High to High Impedance
$t_{PZL}$	Propagation Delay, High Impedance to Low
$t_R$	Rise Time
$t_F$	Fall Time

## Truth Tables

### Output Enable

$V_I$	$V_{OE}$	$V_O$
L	L	L
H	L	H
L	H	Z
H	H	Z

### SYNC

SYNC	Internal Refresh Clock
0	Enabled
1	Disabled

**Note:** SYNC should be left open or connected to GND to enable the internal refresh clock, or connected to  $V_{DD}$  to disable the internal clock.



3.3 Volt Electrical Specifications (T <sub>min</sub> to T <sub>max</sub> unless otherwise stated)						
Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Quiescent Supply Current						
IL810, IL811, IL815	I <sub>DD1</sub>		15	30	μA	
IL812, IL814, IL817, IL821			1.3	1.8	mA	
IL816			2.6	3.6	mA	
Output Quiescent Supply Current						
IL810, IL812, IL821	I <sub>DD2</sub>		1.3	1.8	mA	
IL811, IL814, IL816			2.6	3.6	mA	
IL815			5.2	7.2	mA	
IL817			3.9	5.4	mA	
Logic Input Current	I <sub>I</sub>	-10		10	μA	
Logic High Output Voltage	V <sub>OH</sub>	$V_{DD} - 0.1$	$V_{DD}$		V	I <sub>O</sub> = -20 μA, V <sub>I</sub> = V <sub>IH</sub>
		$0.8 \times V_{DD}$	$0.9 \times V_{DD}$			I <sub>O</sub> = -4 mA, V <sub>I</sub> = V <sub>IH</sub>
Logic Low Output Voltage	V <sub>OL</sub>		0	0.1	V	I <sub>O</sub> = 20 μA, V <sub>I</sub> = V <sub>IL</sub>
			0.5	0.8		I <sub>O</sub> = 4 mA, V <sub>I</sub> = V <sub>IL</sub>

Switching Specifications (V <sub>DD</sub> = 3.3 V)						
Maximum Data Rate		100	110		Mbps	C <sub>L</sub> = 15 pF
Pulse Width <sup>(7)</sup>	PW	10			ns	V <sub>O</sub> 50% points;
Propagation Delay Input to Output (High to Low)	t <sub>PHL</sub>		12	18	ns	C <sub>L</sub> = 15 pF
Propagation Delay Input to Output (Low to High)	t <sub>PLH</sub>		12	18	ns	C <sub>L</sub> = 15 pF
Propagation Delay Enable to Output (High to High Impedance)	t <sub>PHZ</sub>			5	ns	C <sub>L</sub> = 15 pF
Propagation Delay Enable to Output (Low to High Impedance)	t <sub>PLZ</sub>			5	ns	C <sub>L</sub> = 15 pF
Propagation Delay Enable to Output (High Impedance to High)	t <sub>PZH</sub>			5	ns	C <sub>L</sub> = 15 pF
Propagation Delay Enable to Output (High Impedance to Low)	t <sub>PZL</sub>			5	ns	C <sub>L</sub> = 15 pF
Pulse Width Distortion <sup>(2)</sup>	PWD		2	3	ns	C <sub>L</sub> = 15 pF
Propagation Delay Skew <sup>(3)</sup>	t <sub>PSK</sub>		4	6	ns	C <sub>L</sub> = 15 pF
Output Rise Time (10%–90%)	t <sub>R</sub>		2	4	ns	C <sub>L</sub> = 15 pF
Output Fall Time (10%–90%)	t <sub>F</sub>		2	4	ns	C <sub>L</sub> = 15 pF
Common Mode Transient Immunity (Output Logic High or Logic Low) <sup>(4)</sup>	CM <sub>H</sub>  ,  CM <sub>L</sub>	30	50		kV/μs	V <sub>CM</sub> = 1500 V <sub>DC</sub> t <sub>TRANSIENT</sub> = 25 ns
Channel-to-Channel Skew	t <sub>CSK</sub>		2	3	ns	C <sub>L</sub> = 15 pF
SYNC Internal Clock Off Time <sup>(11)</sup>	t <sub>OFF</sub>			5	ns	
Dynamic Power Consumption <sup>(6)</sup>			140	240	μA/Mbps	per channel

Magnetic Field Immunity <sup>(8)</sup> (V <sub>DD2</sub> = 3V, 3V < V <sub>DD1</sub> < 5.5V)						
Power Frequency Magnetic Immunity	H <sub>PF</sub>	1000	1500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H <sub>PM</sub>	1800	2000		A/m	t <sub>p</sub> = 8μs
Damped Oscillatory Magnetic Field	H <sub>OSC</sub>	1800	2000		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier <sup>(9)</sup>	K <sub>X</sub>		2.5			

5 Volt Electrical Specifications ( $T_{min}$ to $T_{max}$ unless otherwise stated)						
Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Quiescent Supply Current						
IL810, IL811, IL815	$I_{DD1}$		24	40	$\mu$ A	
IL814, IL817, IL821			1.8	2.5	mA	
IL816			3.6	5	mA	
Output Quiescent Supply Current						
IL810, IL821	$I_{DD2}$		1.8	2.5	mA	
IL811, IL814, IL816			3.6	5	mA	
IL815			7.2	10	mA	
IL817			5.4	7.5	mA	
Logic Input Current	$I_I$	-10		10	$\mu$ A	
Logic High Output Voltage	$V_{OH}$	$V_{DD} - 0.1$	$V_{DD}$		V	$I_O = -20 \mu$ A, $V_I = V_{IH}$
		$0.8 \times V_{DD}$	$0.9 \times V_{DD}$			$I_O = -4 \text{ mA}$ , $V_I = V_{IH}$
Logic Low Output Voltage	$V_{OL}$		0	0.1	V	$I_O = 20 \mu$ A, $V_I = V_{IL}$
			0.5	0.8		$I_O = 4 \text{ mA}$ , $V_I = V_{IL}$

Switching Specifications						
Maximum Data Rate		100	110		Mbps	$C_L = 15 \text{ pF}$
Pulse Width <sup>(7)</sup>	PW	10			ns	$V_o$ 50% points
Propagation Delay Input to Output (High to Low)	$t_{PHL}$		10	15	ns	$C_L = 15 \text{ pF}$
Propagation Delay Input to Output (Low to High)	$t_{PLH}$		10	15	ns	$C_L = 15 \text{ pF}$
Propagation Delay Enable to Output (High to High Impedance)	$t_{PHZ}$			5	ns	$C_L = 15 \text{ pF}$
Propagation Delay Enable to Output (Low to High Impedance)	$t_{PLZ}$			5	ns	$C_L = 15 \text{ pF}$
Propagation Delay Enable to Output (High Impedance to High)	$t_{PZH}$			5	ns	$C_L = 15 \text{ pF}$
Propagation Delay Enable to Output (High Impedance to Low)	$t_{PZL}$			5	ns	$C_L = 15 \text{ pF}$
Pulse Width Distortion <sup>(2)</sup>	PWD		2	3	ns	$C_L = 15 \text{ pF}$
Propagation Delay Skew <sup>(3)</sup>	$t_{PSK}$		4	6	ns	$C_L = 15 \text{ pF}$
Output Rise Time (10%–90%)	$t_R$		1	3	ns	$C_L = 15 \text{ pF}$
Output Fall Time (10%–90%)	$t_F$		1	3	ns	$C_L = 15 \text{ pF}$
Common Mode Transient Immunity (Output Logic High or Logic Low) <sup>(4)</sup>	$ CM_H ,  CM_L $	30	50		kV/ $\mu$ s	$V_{CM} = 1500 V_{DC}$ $t_{TRANSIENT} = 25 \text{ ns}$
Channel-to-Channel Skew	$t_{CSK}$		3	5	ns	$C_L = 15 \text{ pF}$
SYNC Internal Clock Off Time <sup>(11)</sup>	$t_{OFF}$			5	ns	
Dynamic Power Consumption <sup>(6)</sup>			200	340	$\mu$ A/Mbps	per channel

Magnetic Field Immunity <sup>(8)</sup> ( $V_{DD2} = 5V$ , $3V < V_{DD1} < 5.5V$ )						
Power Frequency Magnetic Immunity	$H_{PF}$	2,800	3,500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	$H_{PM}$	4,000	4,500		A/m	$t_p = 8 \mu$ s
Damped Oscillatory Magnetic Field	$H_{OSC}$	4,000	4,500		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier <sup>(9)</sup>	$K_X$		2.5			

**Notes (apply to both 3.3 V and 5 V specifications):**

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1. Absolute maximum means the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. PWD is defined as  $|t_{pHL} - t_{pLH}|$ . %PWD is equal to PWD divided by pulse width.
3.  $t_{psk}$  is the magnitude of the worst-case difference in  $t_{pHL}$  and/or  $t_{pLH}$  between devices at 25°C.
4.  $CM_H$  is the maximum common mode voltage slew rate that can be sustained while maintaining  $V_o > 0.8 V_{DD2}$ .  $CM_L$  is the maximum common mode input voltage that can be sustained while maintaining  $V_o < 0.8 V$ . The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
5. Device is considered a two terminal device: pins on each side of the package are shorted.
6. Dynamic power consumption is calculated per channel and is supplied by the channel's input side power supply.
7. Minimum pulse width is the minimum value at which specified PWD is guaranteed.
8. The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 9.
9. External magnetic field immunity is improved by this factor if the field direction is "end-to-end" rather than to "pin-to-pin" (see diagram on p. 9).
10. If internal clock is used, devices will respond to DC states on inputs within a maximum of 9  $\mu$ s. Outputs may oscillate if the SYNC input slew rate is less than 1 V/ms.
11.  $t_{off}$  is the maximum time for the internal refresh clock to shut down.

## Application Information

### Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

### Electromagnetic Compatibility

IsoLoop Isolators have the lowest EMC footprint of any isolation technology. IsoLoop Isolators' Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards.

Additionally, on the IL810 and IL815, the internal clock can be disabled for even better EMC performance.

These isolators are fully compliant with generic EMC standards EN50081, EN50082-1 and the umbrella line-voltage standard for Information Technology Equipment (ITE) EN61000. NVE has completed compliance tests in the categories below:

EN50081-1

Residential, Commercial & Light Industrial  
Methods EN55022, EN55014

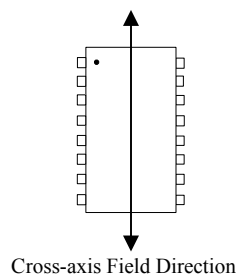
EN50082-2: Industrial Environment

Methods EN61000-4-2 (ESD), EN61000-4-3 (Electromagnetic Field Immunity), EN61000-4-4 (Electrical Transient Immunity), EN61000-4-6 (RFI Immunity), EN61000-4-8 (Power Frequency Magnetic Field Immunity), EN61000-4-9 (Pulsed Magnetic Field), EN61000-4-10 (Damped Oscillatory Magnetic Field)

ENV50204

Radiated Field from Digital Telephones (Immunity Test)

Immunity to external magnetic fields is even higher if the field direction is "end-to-end" rather than to "pin-to-pin" as shown in the diagram below:



### Power Supply Decoupling

Both power supplies to these devices should be decoupled with low ESR ceramic capacitors of at least 47 nF. Capacitors must be located as close as possible to the  $V_{DD}$  pins.

### Maintaining Creepage

Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

### Dynamic Power Consumption

IsoLoop Isolators achieve their low power consumption from the way they transmit data across the isolation barrier. A magnetic field is created around the GMR Wheatstone bridge by detecting the edge transitions of the input logic signal and converting them to narrow current pulses. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5 ns, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers, which have power consumption heavily dependent on mark-to-space ratio.

### DC Correctness, EMC, and the SYNC Function

NVE digital isolators have the lowest EMC noise signature of any high-speed digital isolator on the market today because of the dc nature of the GMR sensors used. It is perhaps fair to include optocouplers in that dc category too, but their limited parametric performance, physically large size, and wear-out problems effectively limit side by side comparisons between NVE's isolators and isolators coupled with RF, matched capacitors, or transformers.

IL800-Series isolators has an internal refresh clock which ensure the synchronization of input and output within 9  $\mu$ s of the supply passing the 1.5 V threshold. The IL810 and IL815 allow external control of the refresh clock through the SYNC pin thereby further lowering the EMC footprint. This can be advantageous in applications such as hi-fi, motor control and power conversion.

The isolators can be used with Power on Reset (POR) circuits common in microcontroller applications, as the means of ensuring the output of the device is in the same state as the input a short time after power up. Figure 1 shows a practical Power on Reset circuit:

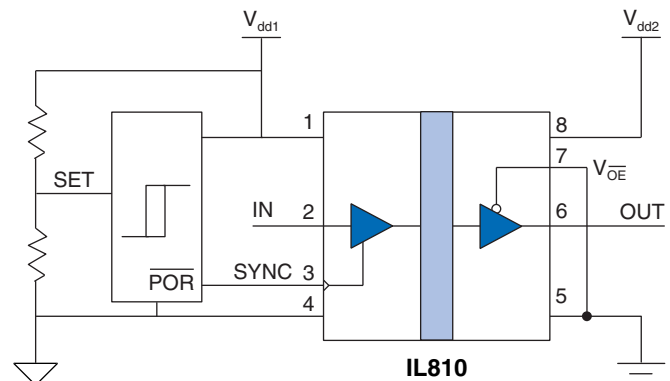
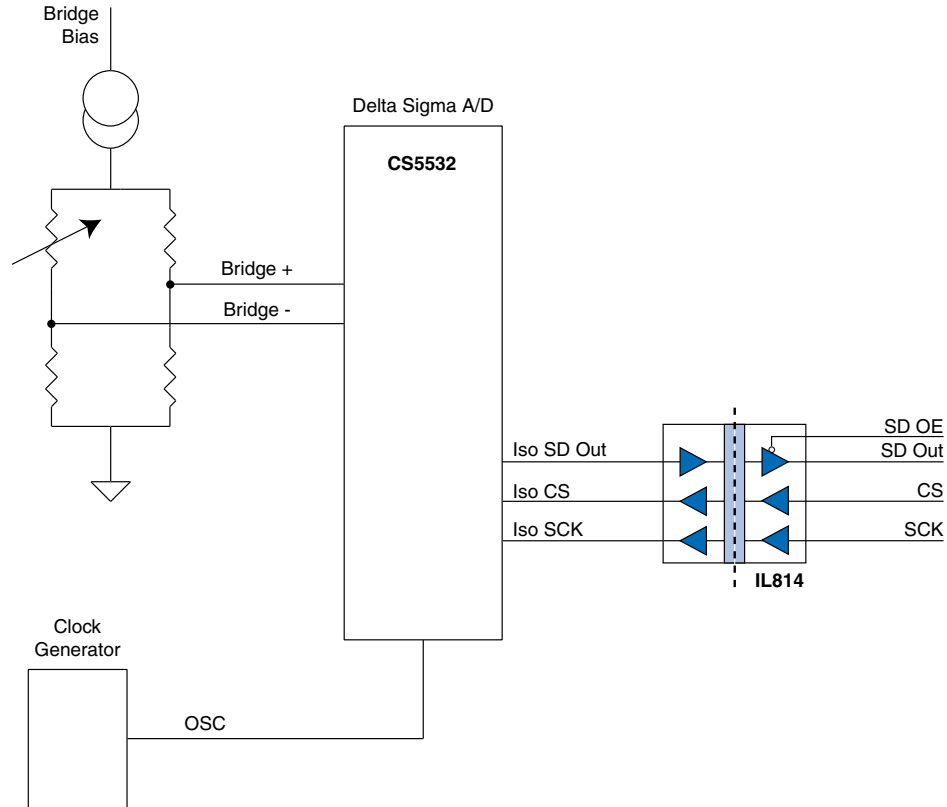


Fig. 1. Typical Power On Reset Circuit for IL810

After POR, the SYNC line goes high, the internal clock is disabled, and the EMC signature is optimized. Decoupling capacitors are omitted for clarity.

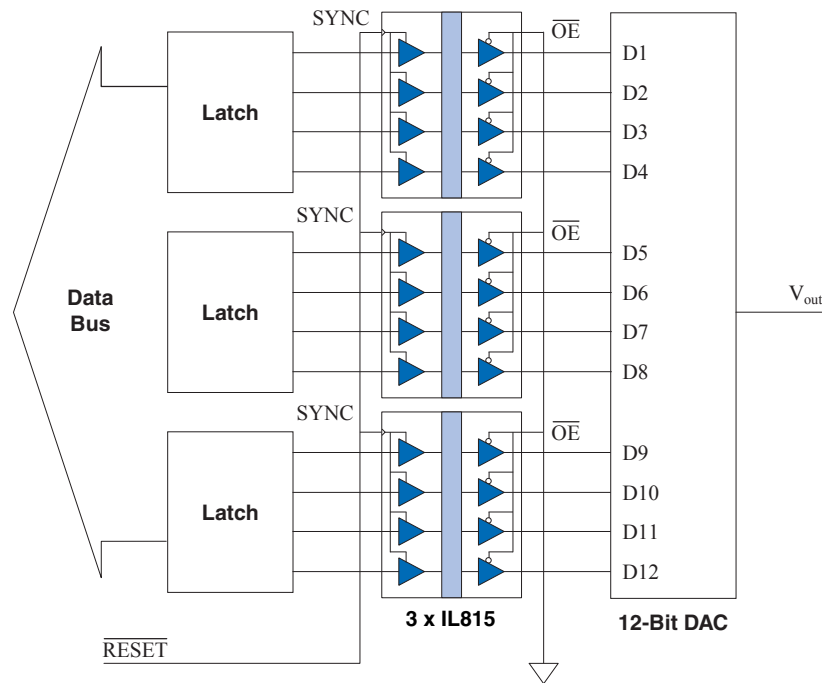
## Illustrative Applications

### Isolated A/D Converter



A delta-sigma A-D converter interfaced with the three-channel IL814. Multiple channels can easily be combined using the IL814's output enable function.

## 12-Bit D/A Converter Isolation

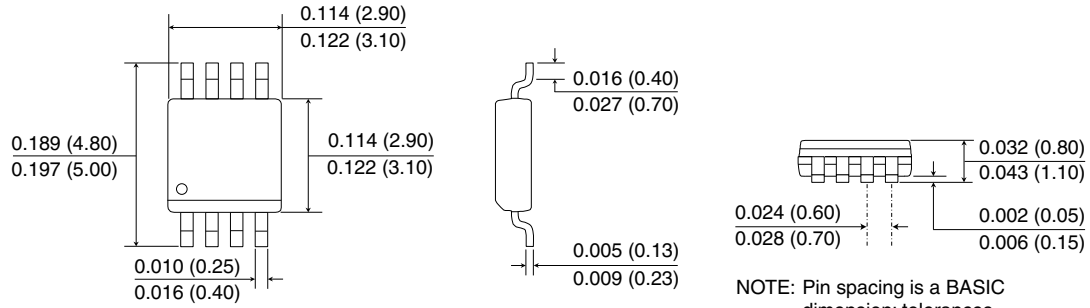


The IL815 four-channel isolator is ideally suited for parallel bus isolation. The circuit above uses three IL815s to isolate a 12-bit DAC. The SYNC function automatically synchronizes the outputs to the inputs, ensuring correct data on the isolator outputs. After the reset pulse goes high, data transfer from input to output is initiated by the leading edge of each changing data bit.

## Package Drawings

### 8-pin MSOP (-1 suffix; 1 and 2 channel)

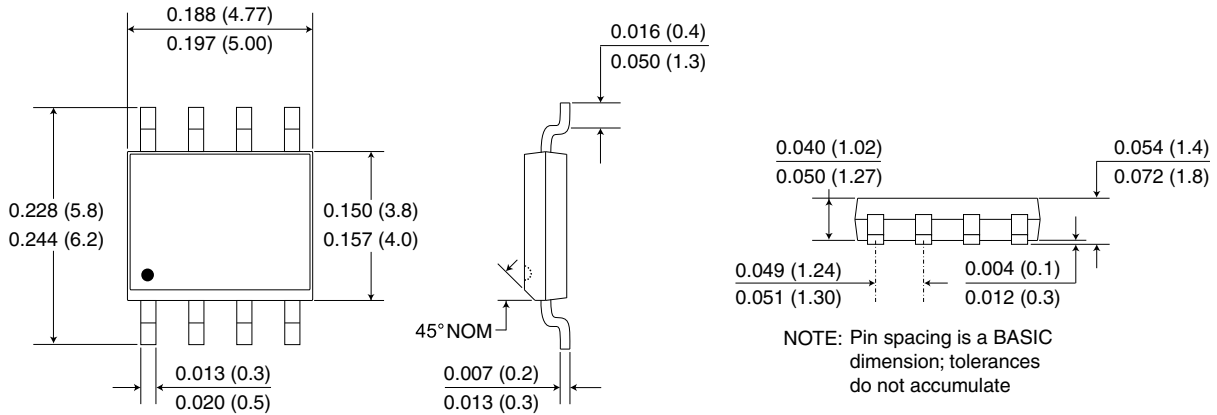
Dimensions in inches (mm); scale = approx. 5X



NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

### 8-pin SOIC Package (-3 suffix; 1 and 2 channel)

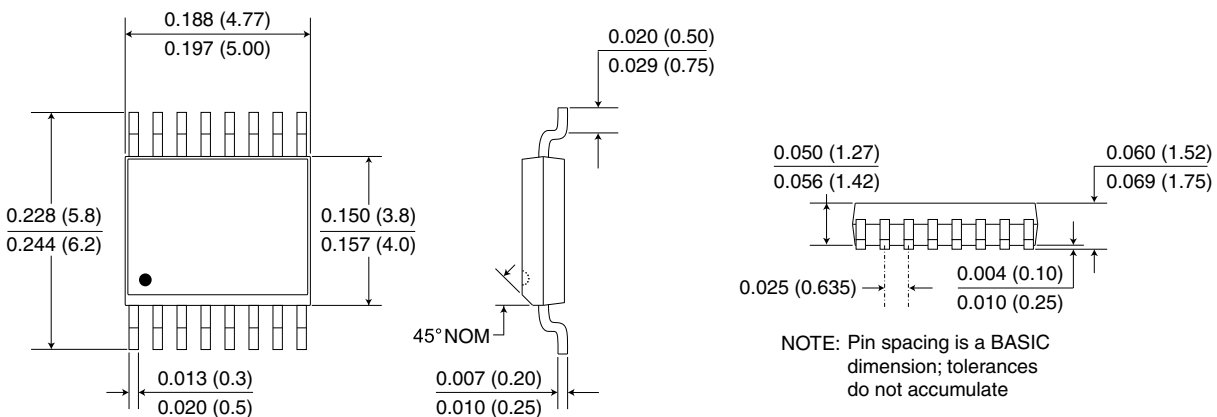
Dimensions in inches (mm); scale = approx. 5X



NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

### Ultraminiature 16-pin QSOP Package (-1 suffix; 3 and 4 channel)

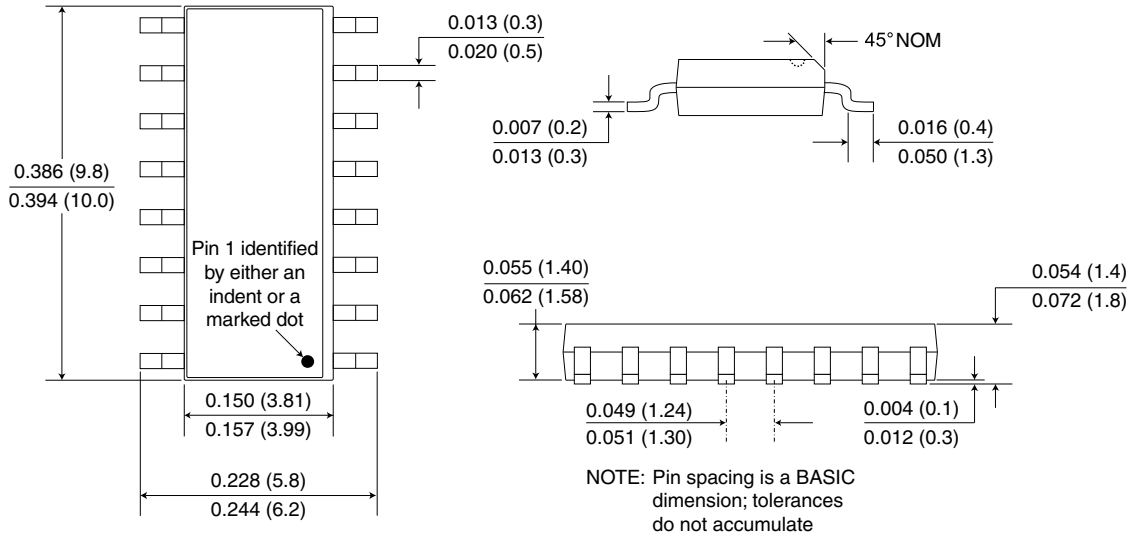
Dimensions in inches (mm); scale = approx. 5X



NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

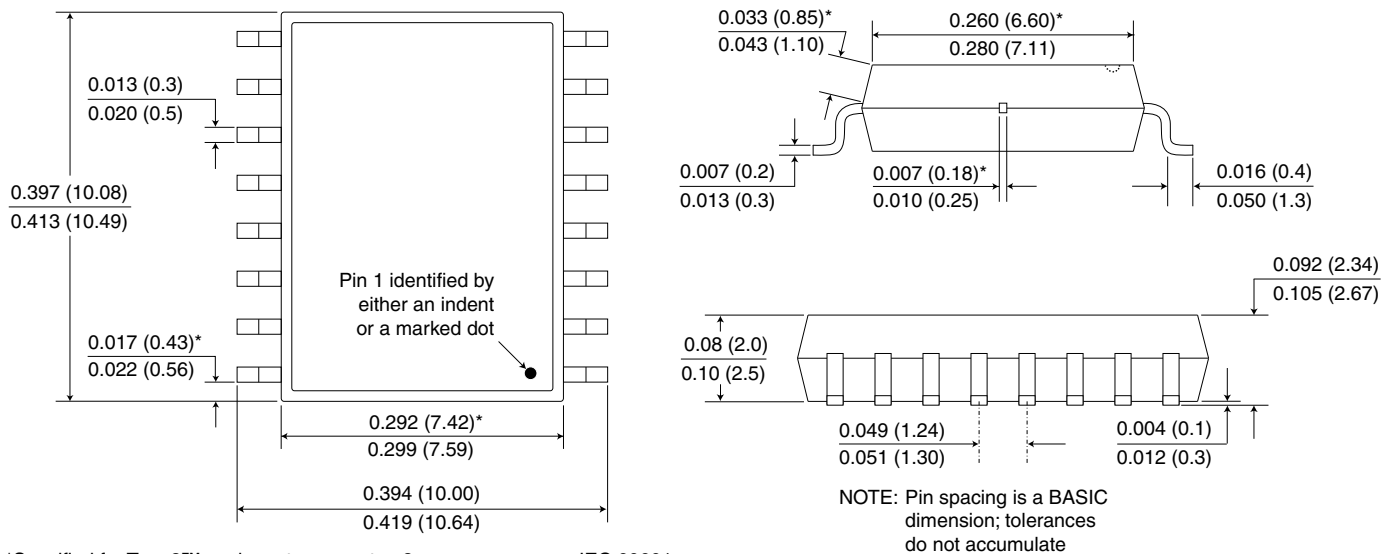
## 0.15" 16-pin SOIC Package (-3 suffix; 3 and 4 channel)

Dimensions in inches (mm); scale = approx. 5X



## True8™ 0.3" 16-pin SOIC Package (no suffix; 3 and 4 channel)

Dimensions in inches (mm); scale = approx. 5X



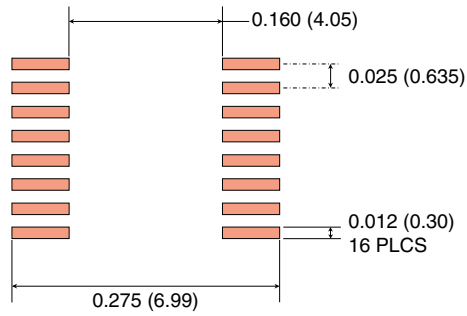
\*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.



## Recommended Pad Layouts

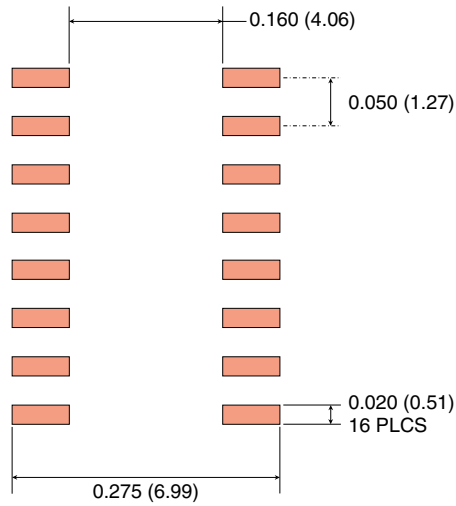
### 4 mm x 5 mm 16-pin QSOP Pad Layout

Dimensions in inches (mm); scale = approx. 5X



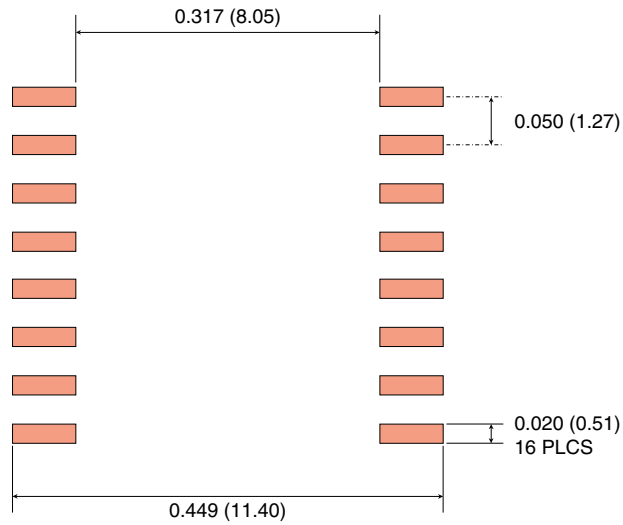
### 0.15" 16-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



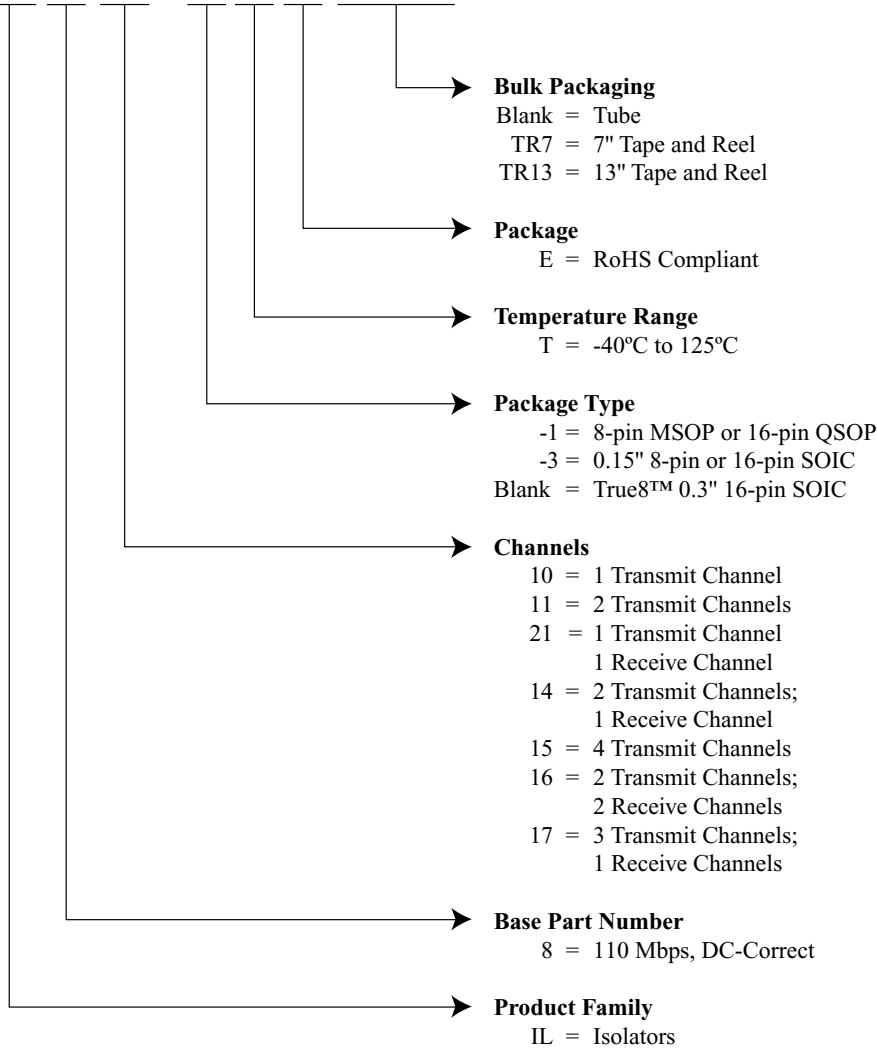
## 0.3" 16-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



## Ordering Information

### IL 8 16 - 3 T E TR13



Available Parts	Xmit Ch.	Rcv. Ch.	Package
IL810T-1E	1	0	MSOP-8
IL810T-3E	1	0	SOIC-8
IL811T-1E	2	0	MSOP-8
IL811T-3E	2	0	SOIC-8
IL821T-3E	1	1	SOIC-8
IL814T-1E	2	1	QSOP-16
IL814T-3E	2	1	0.15" SOIC-16
IL814TE	2	1	True8
IL815T-1E	4	0	QSOP-16
IL815T-3E	4	0	0.15" SOIC-16
IL815TE	4	0	True8
IL816T-1E	2	2	0.15" SOIC-16
IL816T-3E	2	2	0.15" SOIC-16
IL816TE	2	2	True8
IL817T-3E	3	1	0.15" SOIC-16
IL817TE	3	1	True8
IL821TE	1	1	True8

**ISB-DS-001-IL800-F**  
**June 2014**

**Changes:**

- Added IL814T-1, IL815T-1, and IL816T-1 QSOP versions.
- Dropped IL812 configuration in favor of IL821 two-channel bidirectional configuration.
- Updated thermal characteristics.
- Added recommended pad layouts.

**ISB-DS-001-IL800-E**  
**November 2013**

**Changes:**

- Added IL821TE part type (16-pin True8 wide-body package).
- Added output enables to IL816 and IL817.
- Clarified pinouts for different package types.
- IEC 60747-5-5 (VDE 0884) certification.
- Upgraded from MSL 2 to MSL 1.

**ISB-DS-001-IL800-D**  
**August 2013**

**Changes:**

- Tighter quiescent current specifications.
- Added IL817 part types.

**ISB-DS-001-IL800-C**  
**July 2013**

**Changes:**

- Added IL812-3 and IL821-3 part types (8-pin SOIC packages).

**ISB-DS-001-IL800-B**  
**June 2013**

**Changes:**

- Increased transient immunity specifications based on additional data.

**ISB-DS-001-IL800-A**  
**May 27, 2013**

**Changes:**

- Added “T” to full part numbers to indicate 125°C max. operating temperature.
- Added two-channel bidirectional versions (IL812 and IL821).
- Added list of available part types.

**ISB-DS-001-IL800-PREVIEW**  
**May 3, 2013**

**Changes:**

- Released product preview.

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ISB-DS-001-IL800T-F

*June 2014*