BURR - BROWN®

PCM1715U

Dual Voltage Output CMOS Delta-Sigma DIGITAL-TO-ANALOG CONVERTER With On-Chip Digital Filter

FEATURES

- **DUAL MULTI-LEVEL NOISE SHAPING DAC WITH ON-CHIP DIGITAL FILTER**
- **HIGH PERFORMANCE:**
  THD+N: 0.0025% (–92dB) typ
  Dynamic Range: 98dB typ
  S/N RATIO: 110dB typ
- **ANALOG VOLTAGE OUTPUT:**
  V_o = 3.2Vp-p
- **ON-CHIP ANALOG LOW PASS FILTER**
- **JITTER TOUGH AND LOW RADIO FREQUENCY INTERFERENCE ENERGY ARCHITECTURE**
- **SYSTEM CLOCK 256fs or 384fs**
- **ON-CHIP 8X OVERSAMPLING DIGITAL FILTER WITH:**
  Lch/Rch Individual Attentuator Control
  Digital De-Emphasis (44.1kHz)
  Analog Output Mode Select
- **SINGLE +5V POWER SUPPLY OPERATION**
- **SMALL 28-PIN SOIC PACKAGE**

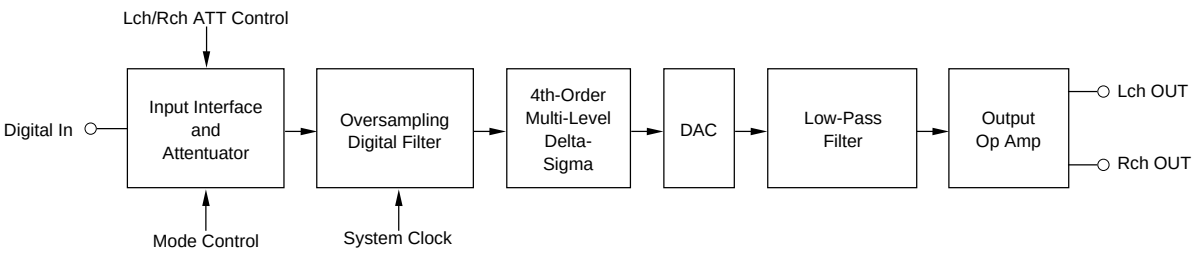
DESCRIPTION

The PCM1715 is a low cost, dual voltage output CMOS digital-to-analog converter. Incorporated into the PCM1715 is a unique multi-level 4th-order delta-sigma architecture that eliminates influence from input clock jitter and RF interferance resulting in truly superior performance.

The PCM1715 has individual channel attenuator and analog output mode select function which is suitable for CD-ROM application.

The on-chip digital filter of the PCM1715 has –62dB stop band attenuation and ±0.008dB ripple in the pass band.

The PCM1715 can be used in a wide variety of consumer audio applications. Its low cost, small size, and single +5V operation make it ideal for portable, automotive, CD players, CD-I, CD-ROM, VIDEO-CD, tuners, music instruments, and other digital audio applications.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATIONS

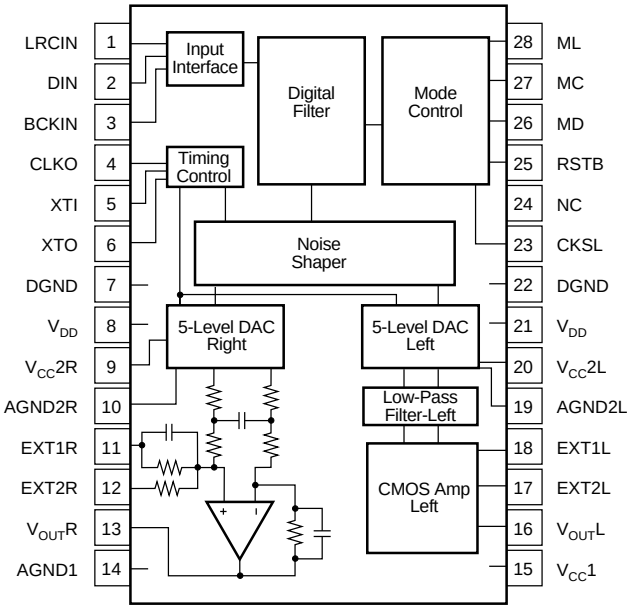
ELECTRICAL

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, fs = 44.1kHz, SYSCLK = 384fs/256fs, and 16-bit data, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1715U MIN	PCM1715U TYP	PCM1715U MAX	UNITS
RESOLUTION			16		Bits
DIGITAL INPUT					
Logic Family					
Input Logic Level (except XTi)					
V_{IH}		2.0			VDC
V_{IL}				0.8	VDC
Input Logic Current (except XTi)				–200	µA
Input Logic Level (XTi)					
V_{IH}		3.2			VDC
V_{IL}				1.4	VDC
Input Logic Current (XTi)				±50	µA
Output Logic Level (CLKO):					
V_{OH}		4.5			VDC
V_{OL}				0.5	VDC
Output Logic Current (CLKO)		±10			mA
Data Format			MSB First, Two's Complement		
Sampling Frequency			44.1		kHz
System Clock Frequency	384fs		16.934		MHz
System Clock Frequency	256fs		11.2894		MHz
DC ACCURACY					
Gain Error			±1.0	±5.0	% of FSR
Gain Mis-Match Channel-To-Channel			±1.0	±5.0	% of FSR
Bipolar Zero Error	V_O = 1/2V_{CC} at Bipolar Zero		±20.0		mV
Gain Drift			±50		ppm of FSR/°C
Bipolar Gain Drift			±20		ppm of FSR/°C
DYNAMIC PERFORMANCE					
THD+N at F/S (0dB)[1]	f_{IN} = 991Hz		–92	–88	dB
THD+N at –60dB[1]	f_{IN} = 991Hz		–36	–32	dB
Dynamic Range	EIAJ A-weighted		98		dB
S/N Ratio	EIAJ A-weighted	104	110		dB
Channel Separation	f_{IN} = 991Hz	90	94		dB
DIGITAL FILTER PERFORMANCE					
Pass Band Ripple				±0.008	dB
Stop Band Attenuation		–62			dB
Pass Band			0.4535		fs
Stop Band			0.5465		fs
De-emphasis Error	(fs = 44.1kHz)			+0.03	dB
ANALOG OUTPUT					
Voltage Range	fs (0dB) OUT		3.2		Vp-p
Load Impedance		5			kΩ
Center Voltage			+1/2V_{CC}		V
POWER SUPPLY REQUIREMENTS					
Voltage Range: $+V_{CC}$		+4.5	+5.0	+5.5	VDC
$+V_{DD}$		+4.5	+5.0	+5.5	VDC
Supply Current $+I_{CC}$ $+I_{DD}$	$+V_{CC}$ = $+V_{DD}$ = +5.0V		45	70	mA
Power Dissipation	$+V_{CC}$ = $+V_{DD}$ = +5.0V		225	350	mW
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+100	°C

NOTE: (1) 30kHz LPF, 400Hz HPF, Average Mode.

PIN CONFIGURATION



PIN ASSIGNMENTS

PIN	NAME	FUNCTION
1	LRCIN	Sample Rate Clock Input (fs)
2	DIN	Data Input
3	BCKIN	Bit Clock Input
4	CLKO	Buffered Output of Oscillator
5	XTI	Oscillator Input (External Clock Input)
6	XTO	Oscillator Output
7	DGND	Digital Ground
8	V_{DD}	Digital Power Supply (+5V)
9	$V_{CC}2R$	Analog (DAC) $+V_{CC}$, Rch
10	AGND2R	Analog (DAC) Ground, Rch
11	EXT1R	Output Amp Common, Rch
12	EXT2R	Output Amp Bias, Rch
13	$V_{OUT}R$	Rch Analog Output
14	AGND	Analog Ground
15	$V_{CC}1$	Analog Power Supply (+5V)
16	$V_{OUT}L$	Lch Analog Output
17	EXT2L	Output Amp Bias, Lch
18	EXT1L	Output Amp Common, Lch
19	AGND2L	Analog (DAC) Ground, Lch
20	$V_{CC}2L$	Analog (DAC) $+V_{CC}$, Lch
21	V_{DD}	Digital Power Supply, (+5V)
22	DGND	Digital Ground
23	CKSL	System Clock Select (H:384fs, L:256fs)
24	NC	No Connection
25	RSTB	Reset
26	MD	Mode Control
27	MC	Mode Control, BCK
28	ML	Mode Control, WDCK

NOTE: All input pins require pull up resistors.

ABSOLUTE MAXIMUM RATINGS

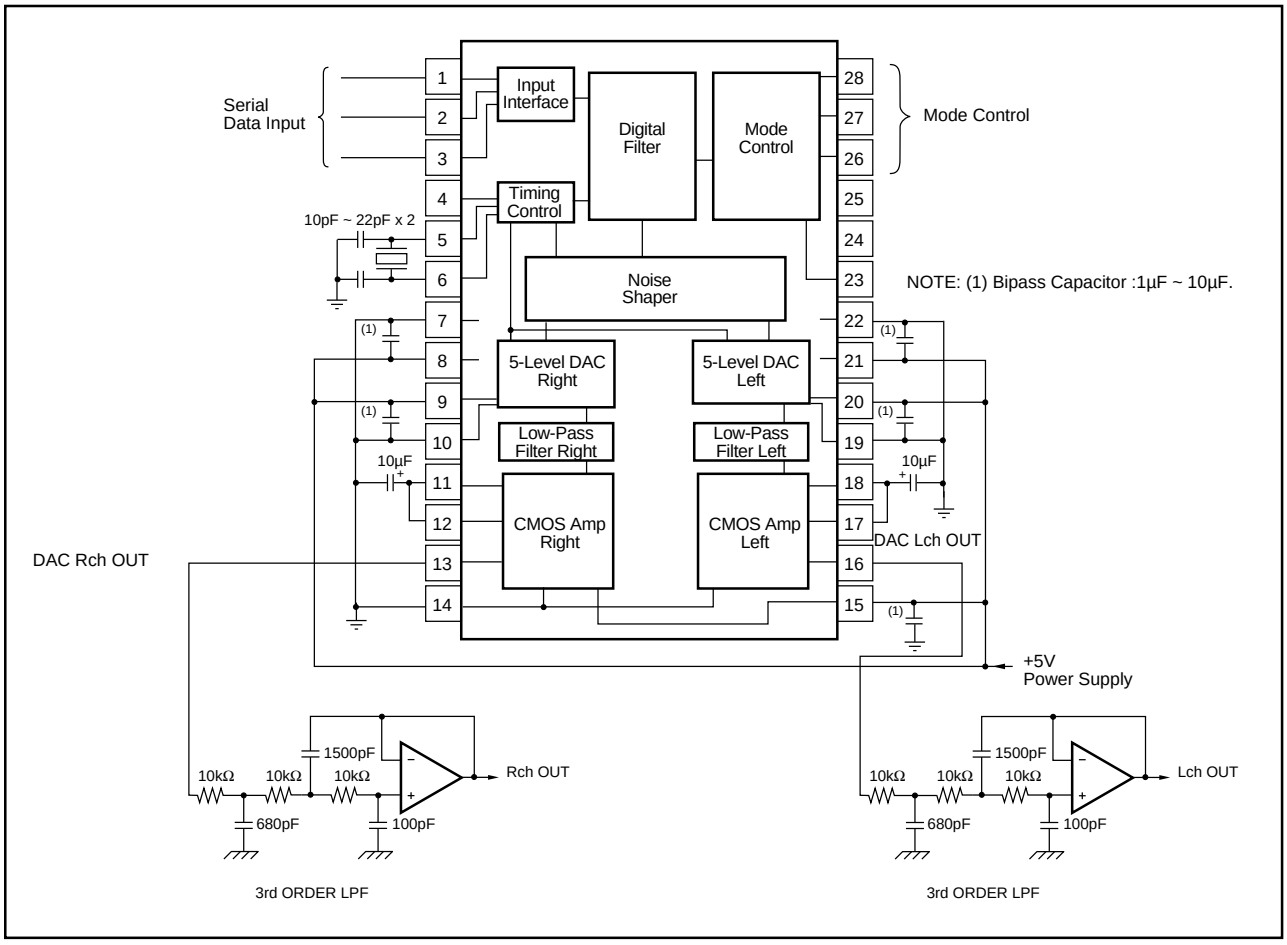
Power Supply Voltage	±6.5VDC
$+V_{CC}$ to V_{DD} Voltage	±0.1V
Input Logic Voltage	–0.3V ~ V_{DD} +0.3V
Power Dissipation	400mW
Operating Temperature	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PCM1715U	28-Pin SOIC	217-4J

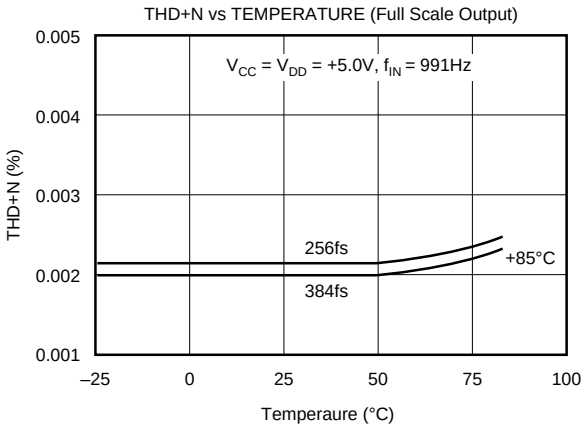
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

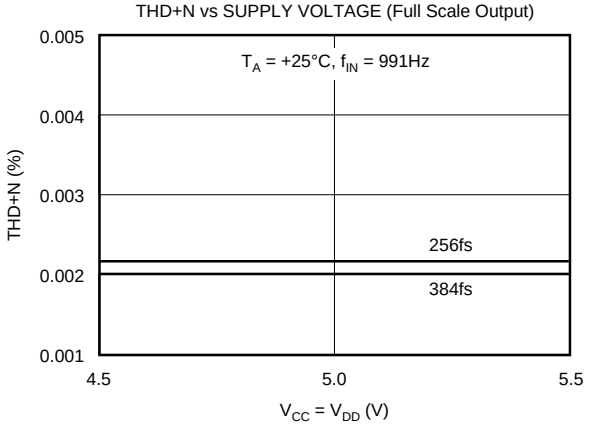
CONNECTION DIAGRAM



TYPICAL PERFORMANCE CURVES

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, fs = 44.1kHz, SYSCLK = 384fs/256fs, and 16-bit data, unless otherwise noted.

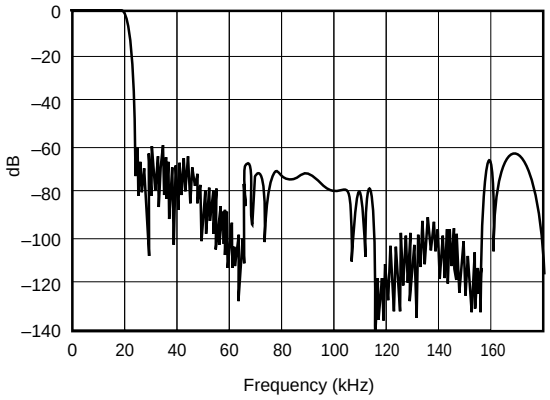




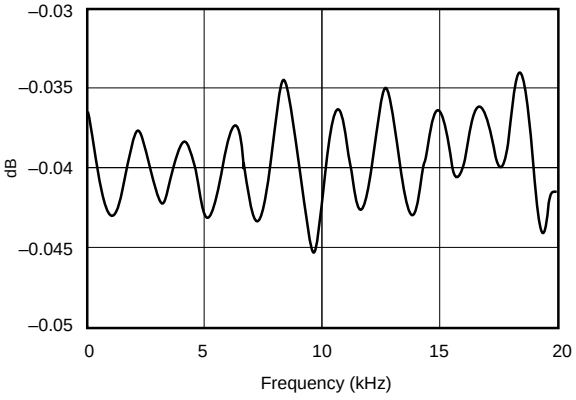
TYPICAL PERFORMANCE CURVES (CONT)

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, fs = 44.1kHz, SYSCLK = 384fs/256fs, and 16-bit data, unless otherwise noted.

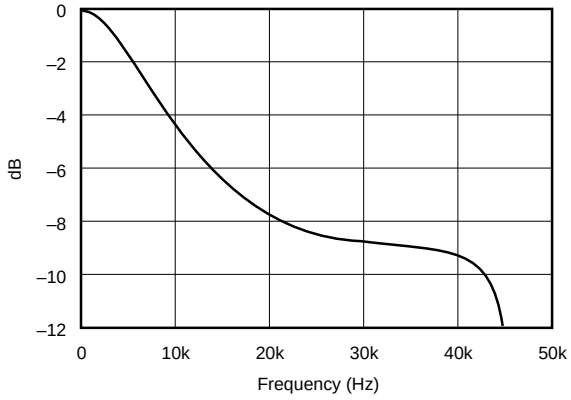
OVERALL FREQUENCY CHARACTERISTIC
(De-Emphasis: OFF)



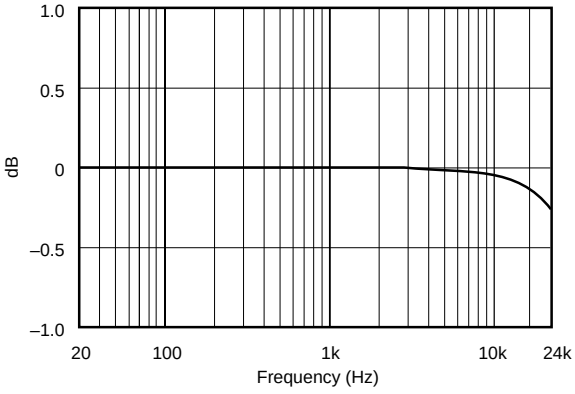
PASSBAND RIPPLE FREQUENCY CHARACTERISTIC
(De-Emphasis: OFF)



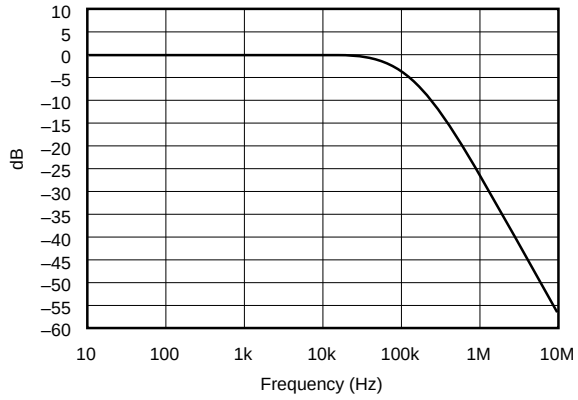
DE-EMPHASIS CHARACTERISTIC



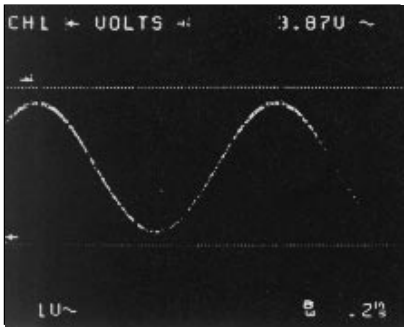
SIMULATED ANALOG FILTER
FREQUENCY RESPONSE
(20Hz~24kHz, Expanded Scale)



SIMULATED ANALOG FILTER
FREQUENCY RESPONSE
(10Hz~10MHz)



OUTPUT WAVE FORM FULL SCALE SIGNAL
(Without External Filter)



NOTES: (1) Measured at V_{OUT} Pin (Pin 13 or 16). (2) The PCM1715 has internal analog low pass filter to reduce high frequency noise-shaped spectrum. Application of the PCM1715 requires external post analog low pass filter which has 2nd-Order or 3rd-Order attenuation performance to get low noise analog output.

THEORY OF DELTA-SIGMA OPERATION

The delta-sigma section of the PCM1715 is based on a 5-level amplitude quantizer and a 4th-order filter. This converts the oversampled 16-bit input data to 5-level delta-sigma form. A block diagram of the 5-level modulator is shown in Figure 1.

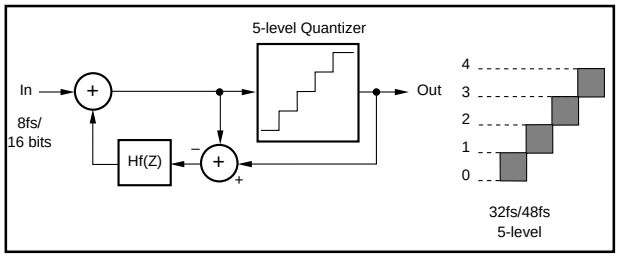


FIGURE 1. Block Diagram of 5-Level Delta-Sigma Quantizer.

This 5-level delta-sigma modulator has the advantage of stability of delta-sigma loop and jitter sensitivity over the typical 1-bit (2-level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal 8x oversampling digital filter is 48fs at a system clock speed of 384fs, 32fs at a system clock speed of 256fs.

A block diagram of the 4th-order filter section Hf(z) in the delta-sigma modulator is shown in Figure 2.

In general, high order 1-bit delta-sigma modulators have disadvantages due to loop instability. The 5 level delta-sigma modulator of the PCM1715 uses phase compensation techniques to obtain stable operation. In Figure 2, the coefficients, b1 to b4, give the basic form of the filter and –a1 and –a2 are used for phase compensation of the feedback loop.

The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figures 3 and 4. In the audio band, the quantization noise floor level of the PCM1715 is less than –130dB (384fs).

MODE OF OPERATION

Serial inputs to MD, MC, and ML (Pins 26, 27 and 28) control the following functions:

(1) Digital Attenuator [AL0 ~ AL7, AR0 ~ AR7]

Attenuation data is constructed by 8-bit/Lch, 8-bit/Rch (total 16-bit), can be controlled as 255 step attenuation by individual channel. AL0 and AR0 are LSB, and AL7 and AR7 are MSB. Attenuation Level ATT is given by:

$$ATT = 20LOG_{10} (ATT\ DATA/255)\ [dB]$$

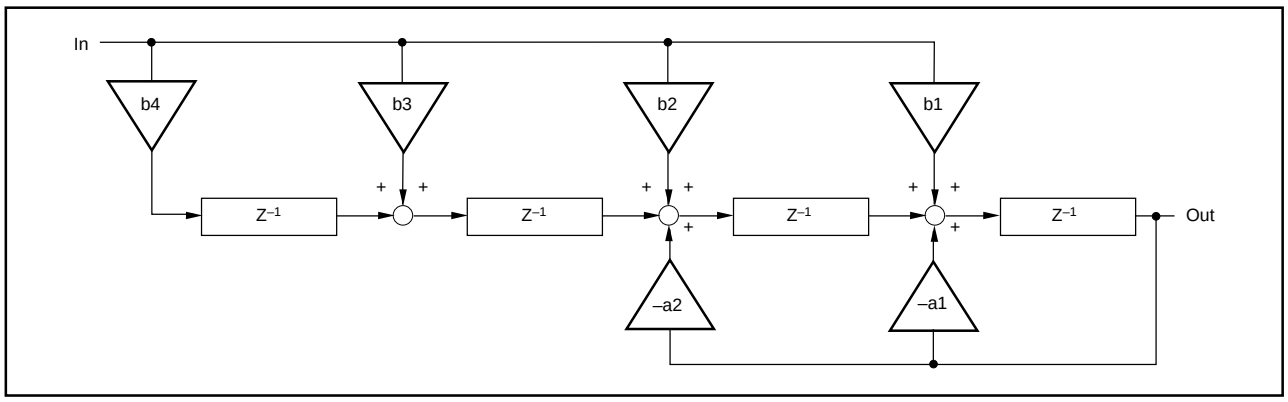


FIGURE 2. Block Diagram of the Hf(z).

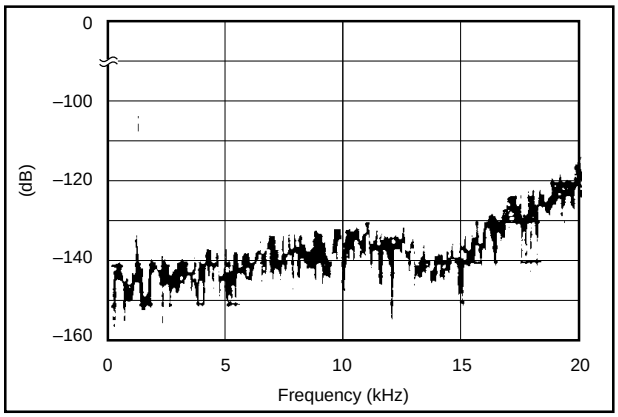


FIGURE 3. Quantization Noise Spectrum (256fs).

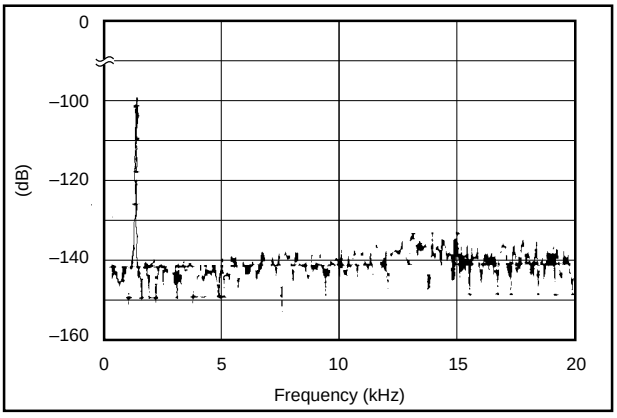


FIGURE 4. Quantization Noise Spectrum (384fs).

At ATT DATA: 0XFF, output is 0dB. At ATT DATA 0X00, output is –∞.

When "Muting" is chosen by output mode control, output goes to –∞ from the present ATT level.

Moving speed from 0dB to –∞ is 1024/f.

Initialized (RESET) ATT level is 0dB.

(2) Versatile Output Mode [PL0 ~ PL3]
By using PL0 ~ PL3 data, up to 16 different output modes (Lch/Rch/L+R/MUTE) can be selected to the output of Lch and Rch, as shown in Table I.

Initialized mode is STEREO mode.

(3) De-emphasis Control (DEM)
De-emphasis function is controlled by DEM flag (H: ON, L: OFF)

De-emphasis is enabled only at 44.1kHzfs. At other fs frequencies, de-emphasis error is not guaranteed. Initialized mode is De-emphasis OFF.

(4) Attenuator Control (ATC)
If common attenuator control of Lch and Rch is needed, use the ATC flag (ATC = "H"). Common attenuation can be controlled by Lch (AL0 ~ AL7) data. Initialized mode is individual.

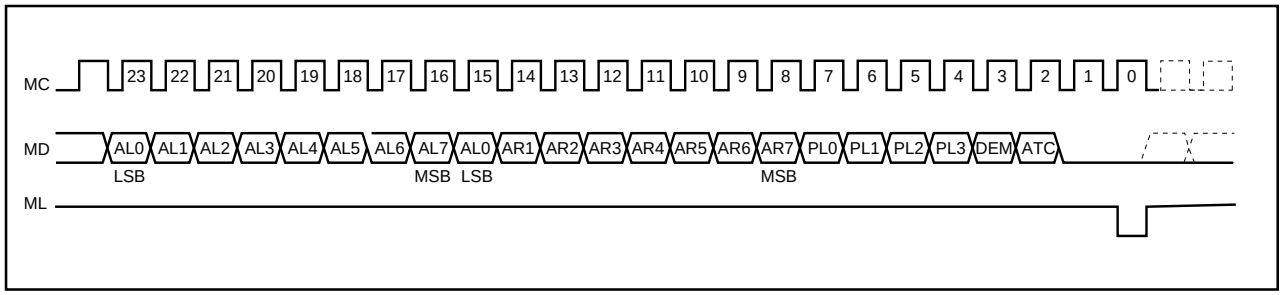
(5) Infinity-Zero Detection
The PCM1715 has an infinity-zero detect function which monitors the input data and bit clock. When the input data is continuously "zero" for 8192 cycles of the bit clock, the infinity zero detect occurs and the DAC outputs are set to bipolar zero ($1/2V_{CC}$).

PL0	PL1	PL2	PL3	Lch OUTPUT	Rch OUTPUT	NOTE
0	0	0	0	MUTE	MUTE	MUTE
0	0	0	1	MUTE	R	
0	0	1	0	MUTE	L	
0	0	1	1	MUTE	(L + R)/2	
0	1	0	0	R	MUTE	
0	1	0	1	R	R	
0	1	1	0	R	L	REVERSE
0	1	1	1	R	(L + R)/2	
1	0	0	0	L	MUTE	
1	0	0	1	L	R	STEREO
1	0	1	0	L	L	
1	0	1	1	L	(L + R)/2	
1	1	0	0	(L + R)/2	MUTE	
1	1	0	1	(L + R)/2	R	
1	1	1	0	(L + R)/2	L	
1	1	1	1	(L + R)/2	(L + R)/2	MONO

TABLE I. PCM1715 Output Mode Control.

(6) Reset
Normally, internal initialize (reset) is done automatically at power on (V_{DD} > 3.5V). The RSTB-pin (Pin 25) accepts external forced reset by RSTB=L. During RSTB=L, the output of the DAC is invalid, set to $1/2V_{CC}$ after internal initialize (1024XTI clock count after RSTB=H).

MODE CONTROL FORMAT



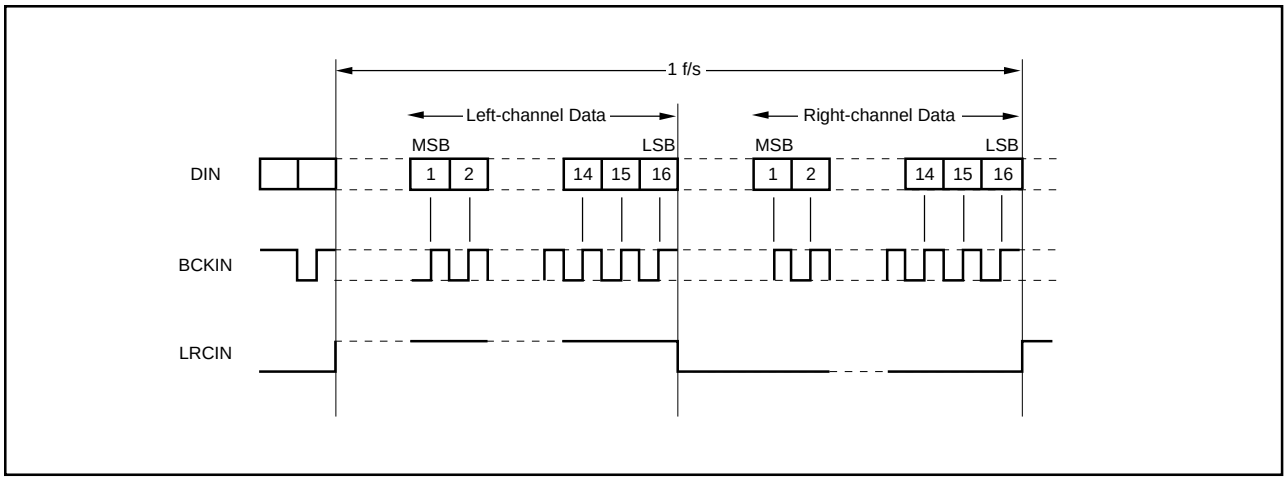


FIGURE 5. Data Input Timing, 16-Bit.

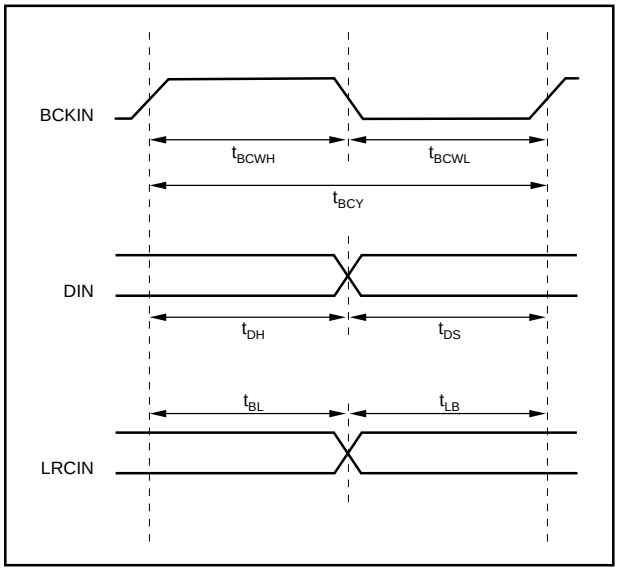


FIGURE 6. Data Input Timing.

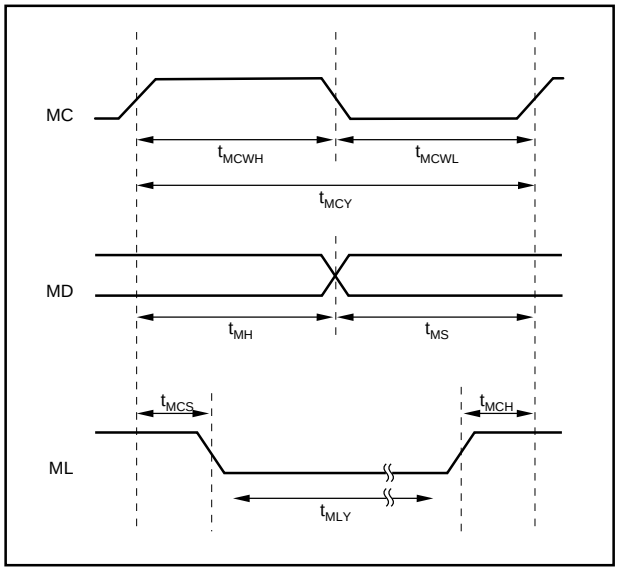


FIGURE 7. Serial Mode Control Timing.

BCK Pulsewidth (H Level)	t_{BCWH}	70ns (min)
BCK Pulsewidth (L Level	t_{BCWL}	70ns (min)
BCK Pulse Cycle Time	t_{BCY}	140ns (min)
DIN Setup Time	t_{DS}	30ns (min)
DIN Hold Time	t_{DH}	30ns (min)
BCK Rising Edge → LRCI Edge	t_{BL}	30ns (min)
LRCI Edge → BCK Rising Edge	t_{LB}	30ns (min)

TABLE II. Data Input Timing Specifications.

MC Pulsewidth (H Level)	t_{MCWH}	50ns (min)
MC Pulsewidth (L Level)	t_{MCWL}	50ns (min)
MC Pulse Cycle Time	t_{MCY}	100ns (min)
MD Setup Time	t_{MS}	30ns (min)
MD Hold Time	t_{MH}	30ns (min)
ML Setup Time	t_{MCS}	30ns (min)
ML Hold Time	t_{MCH}	30ns (min)
ML Low-Level Time	t_{MLY}	1/sysclk + 20ns (min)

TABLE III. Serial Mode Control Timing Specifications.

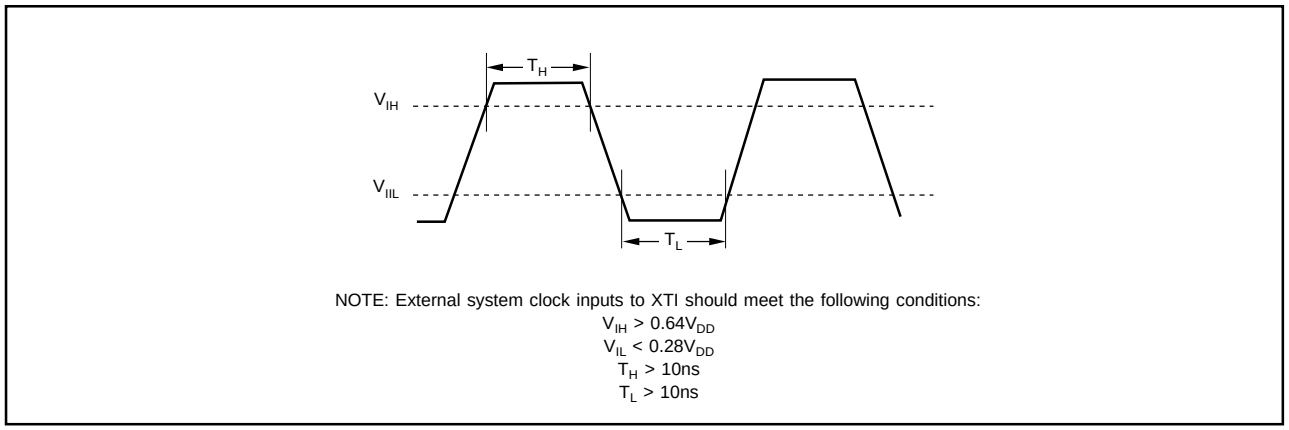


FIGURE 8. Operation Instruction For System Clock.

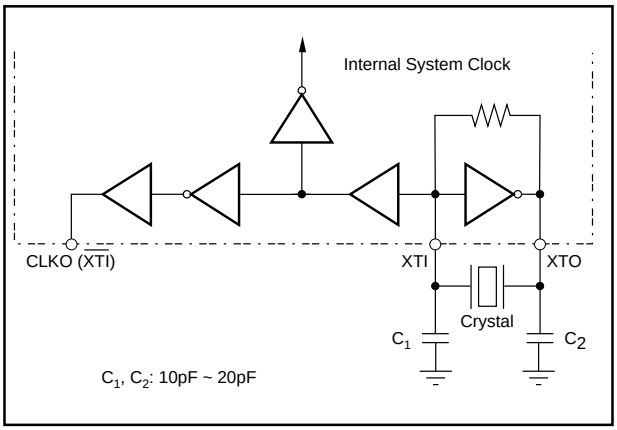


FIGURE 9. Oscillator Circuit Connection Diagram. Optional external crystal oscillator.

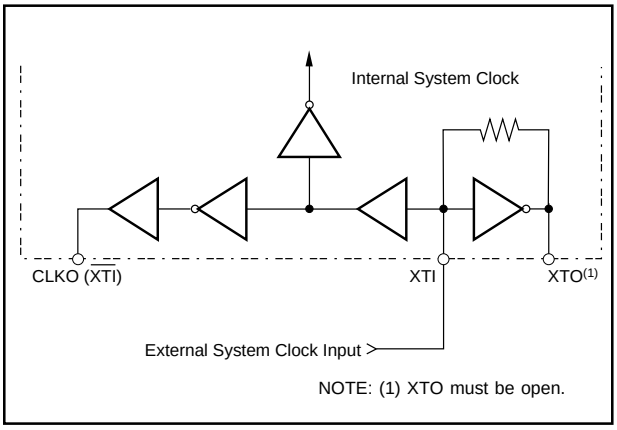


FIGURE 10. Oscillator Circuit Connection Diagram. External system clock.

EVALUATION BOARD

Burr-Brown's DEM-PCM1710 evaluation board for the PCM1710 is capable of evalution of the PCM1715 and PCM1710. Digital input signals for the evaluation board are LRCK, BCK, DATA, and system clock (256fs or 384fs). Power supply requirement is only +5V.

The DEM-PCM1710 has a pattern layout for an optional crystal oscillator. However, the crystal is not installed.