



24-Bit ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 24 BITS NO MISSING CODES
- 0.0015% INL
- 21 BITS EFFECTIVE RESOLUTION (PGA = 1), 19 BITS (PGA = 128)
- PGA FROM 1 TO 128
- SINGLE CYCLE SETTLING
- PROGRAMMABLE DATA OUTPUT RATES
- EXTERNAL DIFFERENTIAL REFERENCE OF 0.1V TO 5V
- ON-CHIP CALIBRATION
- SPI™ COMPATIBLE
- 2.7V TO 5.25V
- < 1mW POWER CONSUMPTION
- UP TO EIGHT INPUT CHANNELS
- UP TO EIGHT DATA I/O

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- LIQUID/GAS CHROMATOGRAPHY
- BLOOD ANALYSIS
- SMART TRANSMITTERS
- PORTABLE INSTRUMENTATION
- WEIGHT SCALES
- PRESSURE TRANSDUCERS

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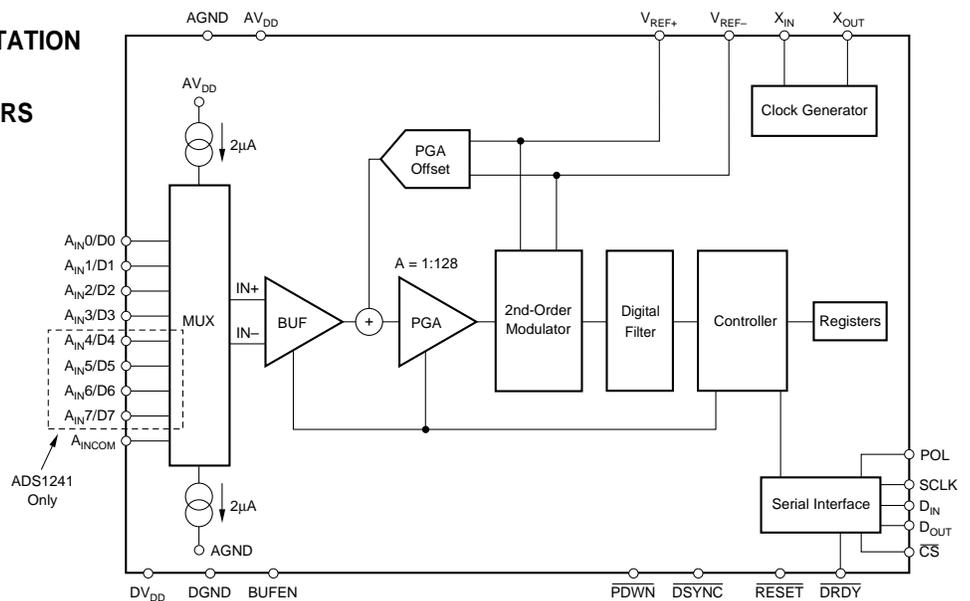
DESCRIPTION

The ADS1240 and ADS1241 are precision, wide dynamic range, delta-sigma, Analog-to-Digital (A/D) converters with 24-bit resolution operating from 2.7V to 5.25V supplies. The delta-sigma, A/D converter provides up to 24 bits of no missing code performance and effective resolution of 21 bits.

The eight input channels are multiplexed. Internal buffering can be selected to provide a very high input impedance for direct connection to transducers or low-level voltage signals. Burn out current sources are provided that allow for the detection of an open or shorted sensor. An 8-bit Digital-to-Analog (D/A) converter provides an offset correction with a range of 50% of the FSR (Full-Scale Range).

The PGA (Programmable Gain Amplifier) provides selectable gains of 1 to 128 with effective resolution of 19 bits at a gain of 128. The A/D conversion is accomplished with a second-order delta-sigma modulator and programmable sinc filter. The reference input is differential and can be used for ratiometric conversion.

The serial interface is SPI compatible. Up to eight bits of data I/O is also provided that can be used for output or input. The ADS1240 and ADS1241 are designed for high-resolution measurement applications in smart transmitters, industrial process control, weight scales, chromatography, and portable instrumentation.



SPECIFICATIONS: $AV_{DD} = 5V$

All specifications T_{MIN} to T_{MAX} , $AV_{DD} = +5V$, $DV_{DD} = +2.7V$ to $5.25V$, $f_{MOD} = 19.2kHz$, $PGA = 1$, Buffer ON, $f_{DATA} = 15Hz$, $V_{REF} \equiv (REF\ IN+) - (REF\ IN-) = +2.5V$, unless otherwise specified.

PARAMETER	CONDITIONS	ADS1240 ADS1241			UNITS
		MIN	TYP	MAX	
ANALOG INPUT ($A_{IN0} - A_{IN7}$, A_{INCOM})					
Analog Input Range	Buffer OFF	-0.1		$AV_{DD} + 0.1$	V
Full-Scale Input Range	Buffer ON	AGND + 0.05		$AV_{DD} - 1.5$	V
Differential Input Impedance	(I_{IN+}) - (I_{IN-}), See Block Diagram, RANGE = 0			$\pm V_{REF}/PGA$	V
Input Current	RANGE = 1		5/PGA	$\pm V_{REF}/(2 \cdot PGA)$	V
Bandwidth	Buffer OFF		0.5		M Ω
$f_{DATA} = 3.75Hz$	Buffer ON		1.65		nA
$f_{DATA} = 7.50Hz$			3.44		Hz
$f_{DATA} = 15.00Hz$			14.6		Hz
Programmable Gain Amplifier	User Selectable Gain Ranges	1		128	
Input Capacitance			9		pF
Input Leakage Current	Modulator OFF, T = 25°C		5		pA
Burnout Current Sources			2		μA
OFFSET DAC					
Offset DAC Range	RANGE = 0		$\pm V_{REF}/(2 \cdot PGA)$		V
	RANGE = 1		$\pm V_{REF}/(4 \cdot PGA)$		V
Offset DAC Monotonicity		8	± 10		Bits
Offset DAC Gain Error			1		%
Offset DAC Gain Error Drift					ppm/°C
SYSTEM PERFORMANCE					
Resolution		24		24	Bits
No Missing Codes	End Point Fit			± 0.0015	Bits
Integral Non-Linearity			7.5		% of FS
Offset Error ⁽¹⁾			0.02		ppm of FS
Offset Drift ⁽¹⁾			0.005		ppm of FS/°C
Gain Error ⁽¹⁾			0.5		%
Gain Error Drift ⁽¹⁾					ppm/°C
Common-Mode Rejection	at DC	100	130		dB
	$f_{CM} = 60Hz$, $f_{DATA} = 15Hz$		120		dB
Normal-Mode Rejection	$f_{CM} = 50Hz$, $f_{DATA} = 15Hz$		100		dB
	$f_{SIG} = 50Hz$, $f_{DATA} = 15Hz$		100		dB
	$f_{SIG} = 60Hz$, $f_{DATA} = 15Hz$				dB
Output Noise			See Typical Performance Curves		
Power-Supply Rejection	at DC, dB = $-20 \log(\Delta V_{OUT}/\Delta V_{DD})^{(2)}$	80	95		dB
VOLTAGE REFERENCE INPUT					
Reference Input Range	REF IN+, REF IN-	0		AV_{DD}	V
V_{REF}	$V_{REF} \equiv (REF\ IN+) - (REF\ IN-)$, RANGE = 0	0.1		2.5	V
	RANGE = 1			5.0	V
Common-Mode Rejection	at DC		120		dB
Common-Mode Rejection	$f_{VREFCM} = 60Hz$, $f_{DATA} = 15Hz$		120		dB
Bias Current ⁽³⁾	$V_{REF} = 2.5V$		1.3		μA
POWER-SUPPLY REQUIREMENTS					
Power-Supply Voltage	AV_{DD}	4.75		5.25	V
Analog Current	$\overline{PDWN} = 0$, or SLEEP		1		nA
	PGA = 1, Buffer OFF		160	250	μA
	PGA = 128, Buffer OFF		470	675	μA
	PGA = 1, Buffer ON		210	300	μA
	PGA = 128, Buffer ON		880	1275	μA
Digital Current	Normal Mode, $DV_{DD} = 5V$		80	125	μA
	SLEEP Mode, $DV_{DD} = 5V$		60		μA
	Read Data Continuous Mode, $DV_{DD} = 5V$		230		μA
	\overline{PDWN}		0.5		nA
Power Dissipation	PGA = 1, Buffer OFF, $DV_{DD} = 5V$		1.2	1.9	mW
TEMPERATURE RANGE					
Operating		-40		+85	°C
Storage		-60		+100	°C

NOTES: (1) Calibration can minimize these errors. (2) ΔV_{OUT} is change in digital result. (3) 12pF switched capacitor at f_{SAMP} clock frequency.

SPECIFICATIONS: $AV_{DD} = 3V$

All specifications T_{MIN} to T_{MAX} , $AV_{DD} = +3V$, $DV_{DD} = +2.7V$ to $5.25V$, $f_{MOD} = 19.2kHz$, $PGA = 1$, Buffer ON, $f_{DATA} = 15Hz$, $V_{REF} \equiv (REF\ IN+) - (REF\ IN-) = +1.25V$ unless otherwise specified.

PARAMETER	CONDITIONS	ADS1240 ADS1241			UNITS
		MIN	TYP	MAX	
ANALOG INPUT ($A_{IN0} - A_{IN7}$, A_{INCOM}) Analog Input Range Full-Scale Input Voltage Range Input Impedance Input Current Bandwidth $f_{DATA} = 3.75Hz$ $f_{DATA} = 7.50Hz$ $f_{DATA} = 15.00Hz$ Programmable Gain Amplifier Input Capacitance Input Leakage Current Burnout Current Sources	Buffer OFF Buffer ON (In+) - (In-) See Block Diagram, RANGE = 0 RANGE = 1 Buffer OFF Buffer ON -3dB -3dB -3dB User Selectable Gain Ranges Modulator OFF, T = 25°C	-0.1 AGND + 0.05 1	 5/PGA 0.5 1.65 3.44 14.6 9 5 2	 128	V V V V MΩ nA Hz Hz Hz pF pA μA
OFFSET DAC Offset DAC Range Offset DAC Monotonicity Offset DAC Gain Error Offset DAC Gain Error Drift	RANGE = 0 RANGE = 1		$\pm V_{REF}/(2 \cdot PGA)$ $\pm V_{REF}/(4 \cdot PGA)$ ± 10 2	V V bits % ppm/°C	
SYSTEM PERFORMANCE Resolution No Missing Codes Integral Non-Linearity Offset Error ⁽¹⁾ Offset Drift ⁽¹⁾ Gain Error ⁽¹⁾ Gain Error Drift ⁽¹⁾ Common-Mode Rejection Normal-Mode Rejection Output Noise Power-Supply Rejection	End Point Fit at DC $f_{CM} = 60Hz$, $f_{DATA} = 15Hz$ $f_{CM} = 50Hz$, $f_{DATA} = 15Hz$ $f_{SIG} = 50Hz$, $f_{DATA} = 15Hz$ $f_{SIG} = 60Hz$, $f_{DATA} = 15Hz$	24 100 75	 15 0.04 0.01 1.0 130 120 100 100 See Typical Performance Curves 90	24 ± 0.0015 dB dB dB dB dB	Bits Bits % of FS ppm of FS ppm of FS/°C ppm ppm/°C dB dB dB dB
VOLTAGE REFERENCE INPUT Reference Input Range V_{REF} Common-Mode Rejection Common-Mode Rejection Bias Current ⁽³⁾	REF IN+, REF IN- $V_{REF} \equiv (REF\ IN+) - (REF\ IN-)$, RANGE = 0 RANGE = 1 at DC $f_{VREFCM} = 60Hz$, $f_{DATA} = 15Hz$ $V_{REF} = 1.25$	0 0.1	 120 120 0.65	AV_{DD} 1.25 2.5 dB dB μA	
POWER-SUPPLY REQUIREMENTS Power-Supply Voltage Analog Current Digital Current Power Dissipation	AV_{DD} PDWN = 0, or SLEEP PGA = 1, Buffer OFF PGA = 128, Buffer OFF PGA = 1, Buffer ON PGA = 128, Buffer ON Normal Mode, $DV_{DD} = 3V$ SLEEP Mode, $DV_{DD} = 3V$ Read Data Continuous Mode, $DV_{DD} = 3V$ PDWN = 0 PGA = 1, Buffer OFF, $DV_{DD} = 3V$	2.7	 1 140 410 190 820 50 75 113 0.5 0.6	3.3 1225 100 1.2	V nA μA μA μA μA μA μA μA nA mW
TEMPERATURE RANGE Operating Storage		-40 -60		+85 +100	°C °C

NOTES: (1) Calibration can minimize these errors. (2) ΔV_{OUT} is change in digital result. (3) 12pF switched capacitor at f_{SAMP} clock frequency.

DIGITAL SPECIFICATIONS: T_{MIN} to T_{MAX}, DV_{DD} 2.7V to 5.25V

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Input/Output					
Logic Family			CMOS		
Logic Level: V _{IH}		0.8 • DV _{DD}		DV _{DD}	V
V _{IL}		0		0.2 • DV _{DD}	V
V _{OH}	I _{OH} = 1mA	DV _{DD} - 0.4			V
V _{OL}	I _{OL} = 1mA	0		0.4	V
Input Leakage: I _{IH}	V _I = DV _{DD}			10	μA
I _{IL}	V _I = 0				μA
Master Clock Rate: f _{OSC}		-10		5	MHz
Master Clock Period: t _{OSC}	1/f _{OSC}	1		1000	ns
		200			

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

V _{DD} to GND	-0.3V to +6V
Input Current	100mA, Momentary
Input Current	10mA, Continuous
A _{IN}	GND -0.5V to AV _{DD} + 0.5V
Digital Input Voltage to GND	-0.3V to DV _{DD} + 0.3V
Digital Output Voltage to GND	-0.3V to DV _{DD} + 0.3V
Maximum Junction Temperature	+150°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-60°C to +100°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

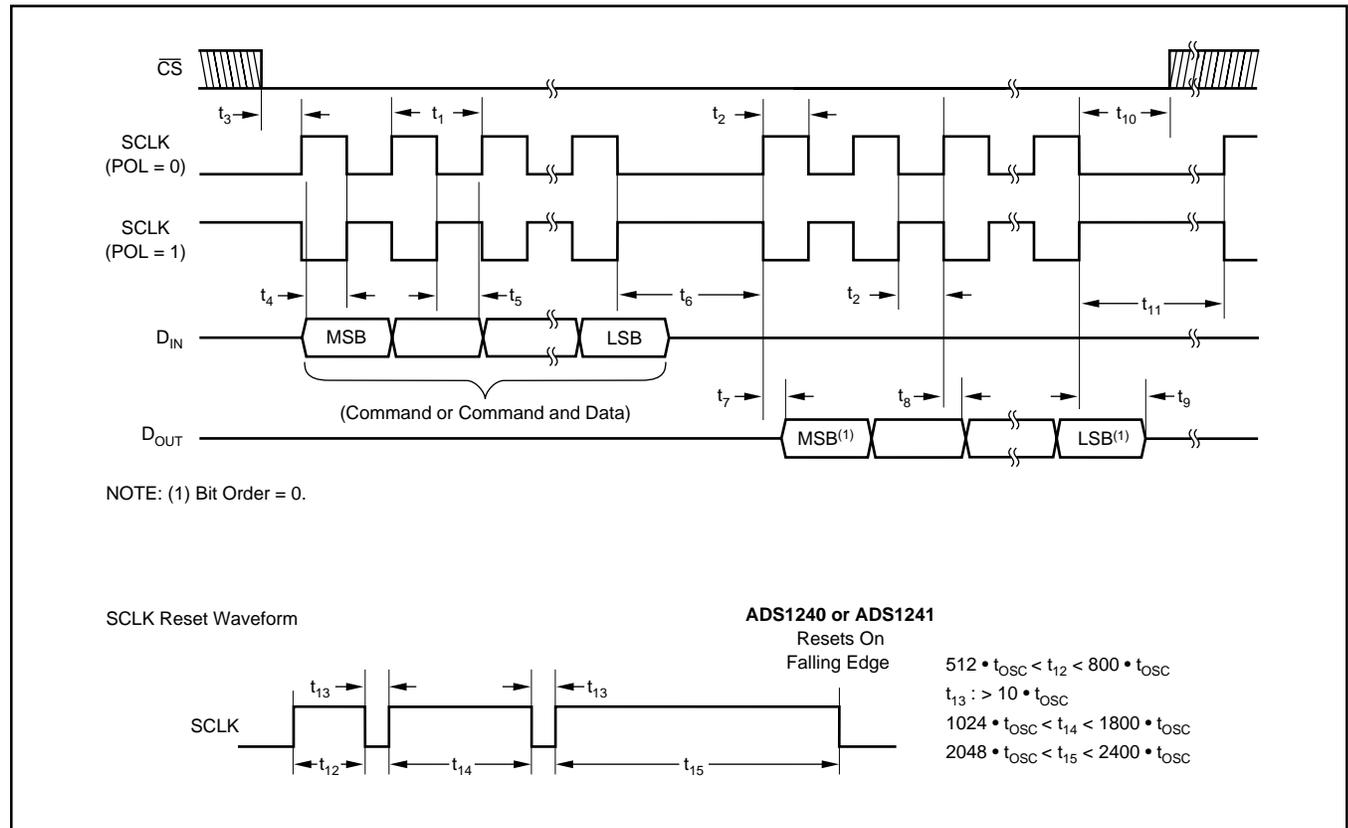
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER ⁽¹⁾	TRANSPORT MEDIA
ADS1240E	SSOP-24	338	-40 to +85	ADS1240E	ADS1240E	Rails
"	"	"	"	"	ADS1240E/1K	Tape and Reel
ADS1241E	SSOP-28	324	-40 to +85	ADS1241E	ADS1241E	Rails
"	"	"	"	"	ADS1241E/1K	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "ADS1240E/1K" will get a single 1000-piece Tape and Reel.

TIMING SPECIFICATIONS

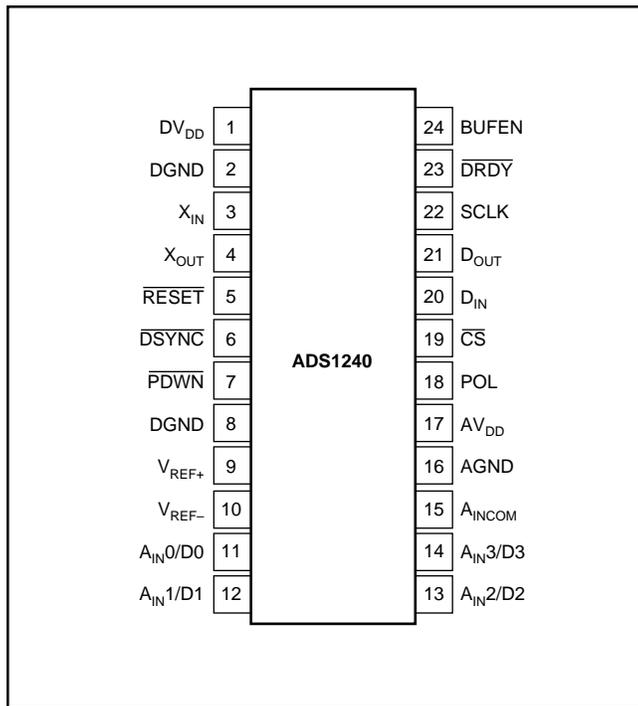


TIMING SPECIFICATION TABLES

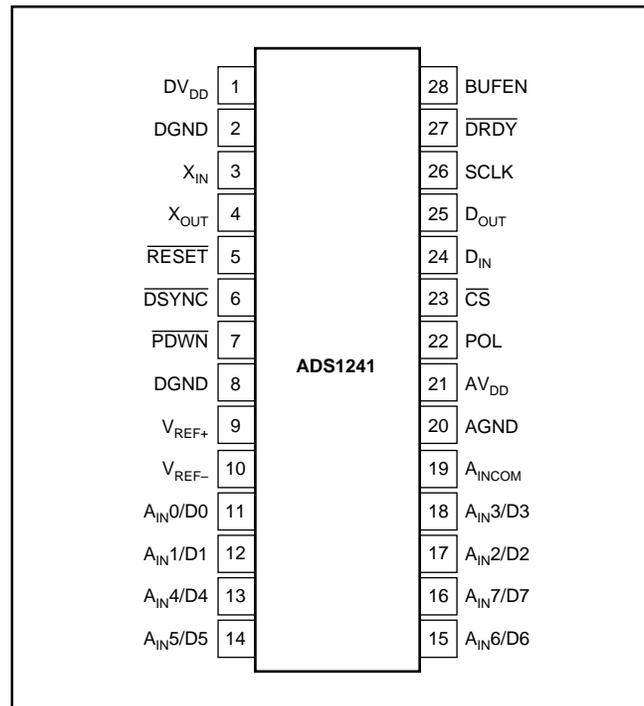
SPEC	DESCRIPTION	MIN	MAX	UNITS
t_1	SCLK Period	4	3	t_{osc} Periods DRDY Periods
t_2	SCLK Pulse Width, HIGH and LOW	200		ns
t_3	\overline{CS} low to first SCLK Edge; Setup Time	0		ns
t_4	D_{IN} Valid to SCLK Edge; Setup Time	50		ns
t_5	Valid D_{IN} to SCLK Edge; Hold Time	50		ns
t_6	Delay between last SCLK edge for D_{IN} and first SCLK edge for D_{OUT} :			
	RDATA, RDATA_C, RREG, WREG	50		t_{osc} Periods
$t_7^{(1)}$	SCLK Edge to Valid New D_{OUT}		50	ns
$t_8^{(1)}$	SCLK Edge to D_{OUT} , Hold Time	0		ns
t_9	Last SCLK Edge to D_{OUT} Tri-State	6	10	t_{osc} Periods
	NOTE: D_{OUT} goes tri-state immediately when \overline{CS} goes HI.			
t_{10}	\overline{CS} Low time after final SCLK edge	0		ns
t_{11}	Final SCLK edge of one op code until first edge SCLK of next command:			
	RREG, WREG, DSYNC, SLEEP, RESET, RDATA, RDATA_C, STOPC	4		t_{osc} Periods
	SELF_GCAL, SELF_FCAL, SYSOCAL, SYS_GCAL	2		DRDY Periods
	SELF_CAL	4		DRDY Periods

NOTE: (1) Load = 20pF || 10kΩ to DGND.

PIN CONFIGURATION (ADS1240)



PIN CONFIGURATION (ADS1241)



PIN DESCRIPTIONS (ADS1240)

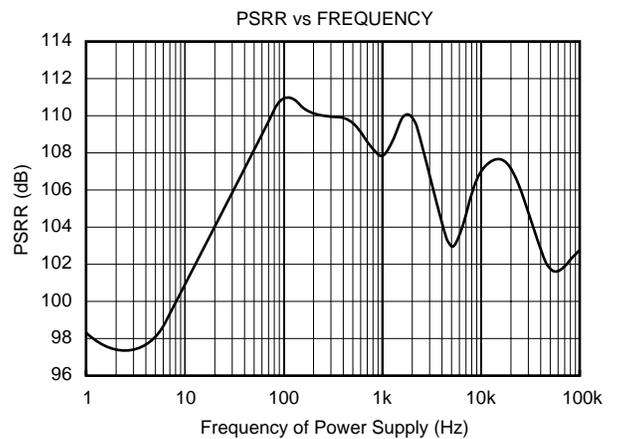
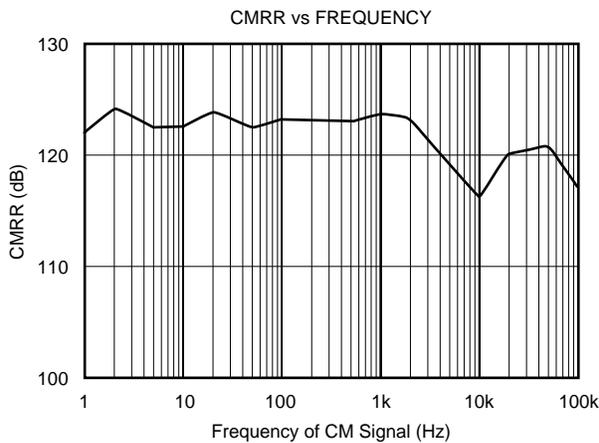
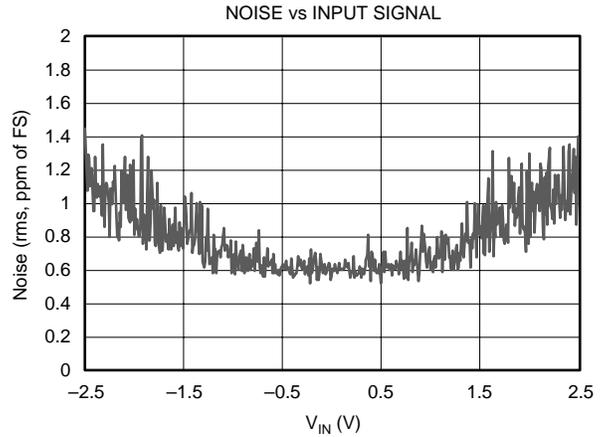
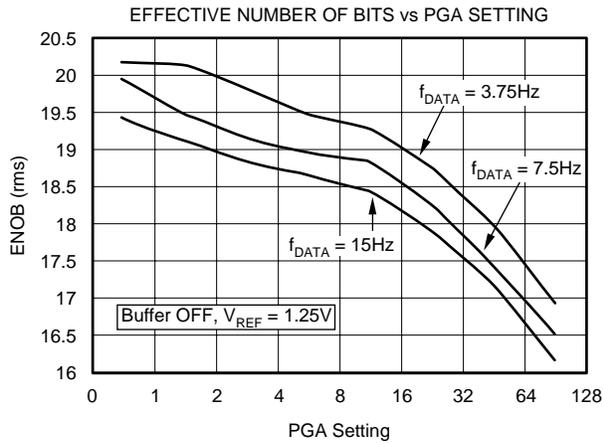
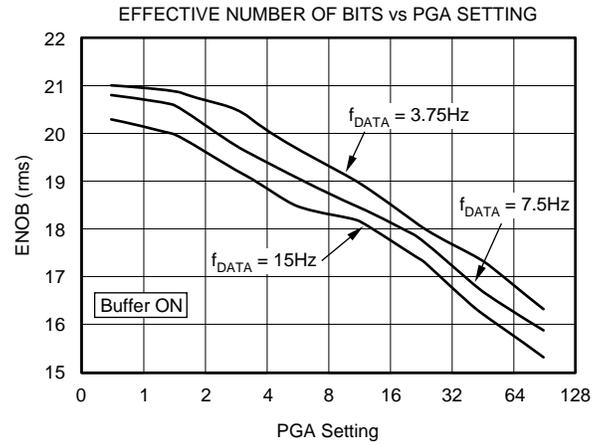
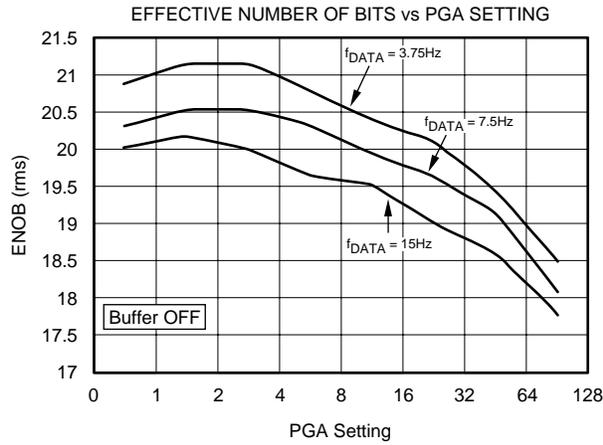
PIN NUMBER	NAME	DESCRIPTION
1	DV _{DD}	Digital Power Supply
2	DGND	Digital Ground
3	X _{IN}	Clock Input
4	X _{OUT}	Clock Output, used with crystal or ceramic resonator.
5	$\overline{\text{RESET}}$	Active LOW, resets the entire device.
6	$\overline{\text{DSYNC}}$	Synchronization Control.
7	$\overline{\text{PDWN}}$	Active LOW. Power Down. The power down function shuts down the analog and digital circuits.
8	DGND	Digital Ground
9	V _{REF+}	Positive Differential Reference Input
10	V _{REF-}	Negative Differential Reference Input
11	A _{IN0/D0}	Analog Input 0/Data I/O 0
12	A _{IN1/D1}	Analog Input 1/Data I/O 1
13	A _{IN2/D2}	Analog Input 2/Data I/O 2
14	A _{IN3/D3}	Analog Input 3/Data I/O 3
15	A _{INCOM}	Analog Input Common
16	AGND	Analog Ground
17	AV _{DD}	Analog Power Supply
18	POL	Serial Clock Polarity
19	$\overline{\text{CS}}$	Active LOW, Chip Select
20	D _{IN}	Serial Data Input, Schmitt Trigger
21	D _{OUT}	Serial Data Output
22	SCLK	Serial Clock, Schmitt Trigger
23	$\overline{\text{DRDY}}$	Active LOW, Data Ready
24	BUFEN	Buffer Enable

PIN DESCRIPTIONS (ADS1241)

PIN NUMBER	NAME	DESCRIPTION
1	DV _{DD}	Digital Power Supply
2	DGND	Digital Ground
3	X _{IN}	Clock Input
4	X _{OUT}	Clock Output, used with crystal or ceramic resonator.
5	$\overline{\text{RESET}}$	Active LOW, entire device.
6	$\overline{\text{DSYNC}}$	Synchronization Control.
7	$\overline{\text{PDWN}}$	Active LOW. Power Down. The power down function shuts down the analog and digital circuits.
8	DGND	Digital Ground
9	V _{REF+}	Positive Differential Reference Input
10	V _{REF-}	Negative Differential Reference Input
11	A _{IN0/D0}	Analog Input 0/Data I/O 0
12	A _{IN1/D1}	Analog Input 1/Data I/O 1
13	A _{IN4/D4}	Analog Input 4/Data I/O 4
14	A _{IN5/D5}	Analog Input 5/Data I/O 5
15	A _{IN6/D6}	Analog Input 6/Data I/O 6
16	A _{IN7/D7}	Analog Input 7/Data I/O 7
17	A _{IN2/D2}	Analog Input 2/Data I/O 2
18	A _{IN3/D3}	Analog Input 3/Data I/O 3
19	A _{INCOM}	Analog Input Common
20	AGND	Analog Ground
21	AV _{DD}	Analog Power Supply
22	POL	Serial Clock Polarity
23	$\overline{\text{CS}}$	Active LOW, Chip Select
24	D _{IN}	Serial Data Input, Schmitt Trigger
25	D _{OUT}	Serial Data Output
26	SCLK	Serial Clock, Schmitt Trigger
27	$\overline{\text{DRDY}}$	Active LOW, Data Ready
28	BUFEN	Buffer Enable

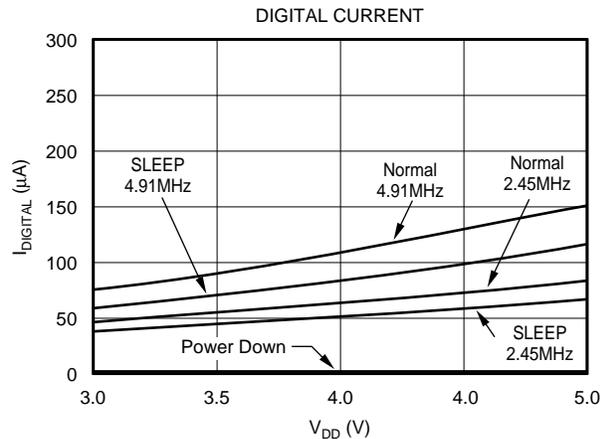
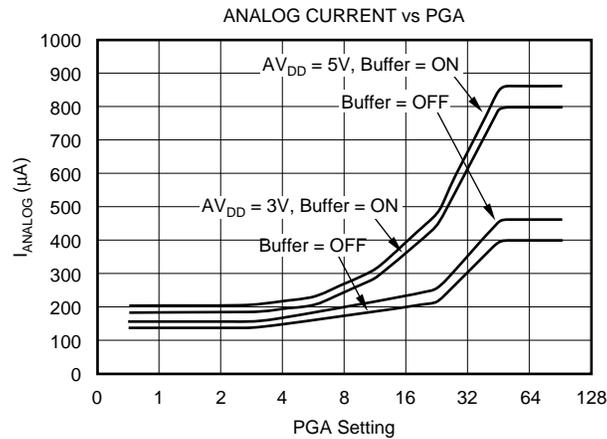
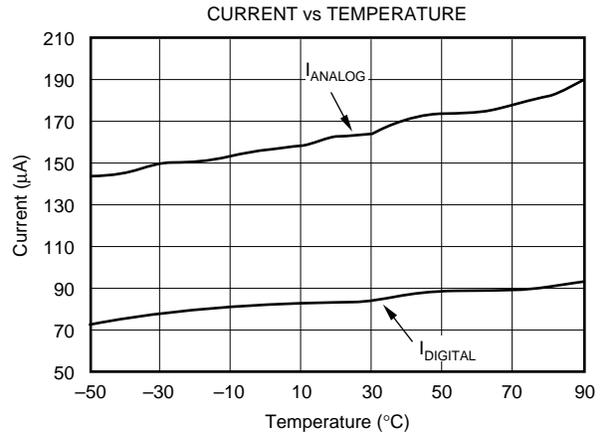
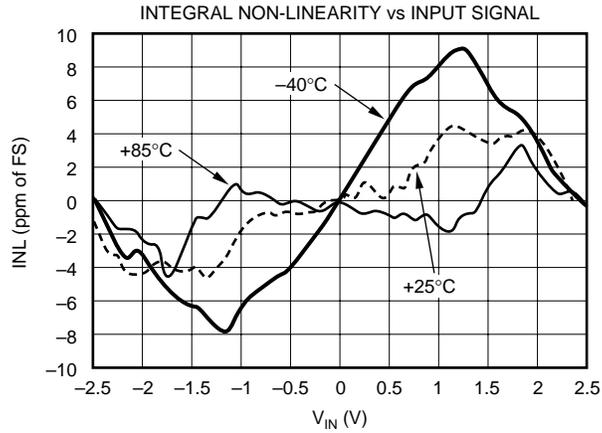
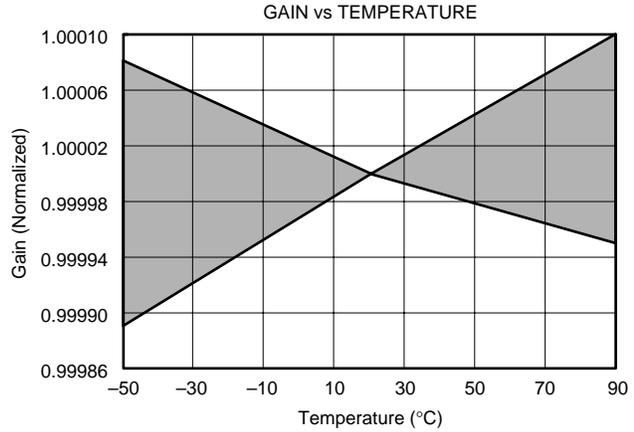
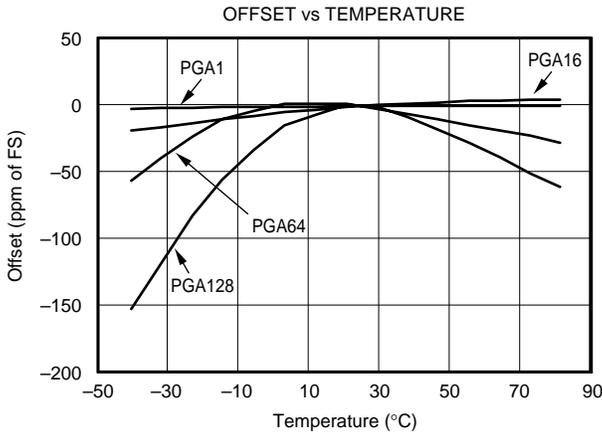
TYPICAL PERFORMANCE CURVES

All specifications, $AV_{DD} = +5V$, $DV_{DD} = +5V$, $f_{OSC} = 2.4576MHz$, $PGA = 1$, $f_{DATA} = 15Hz$, $V_{REF} \equiv (REF IN+) - (REF IN-) = +2.5V$, unless otherwise specified.



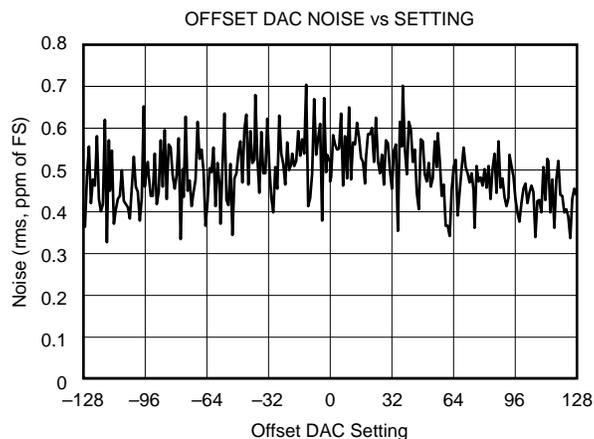
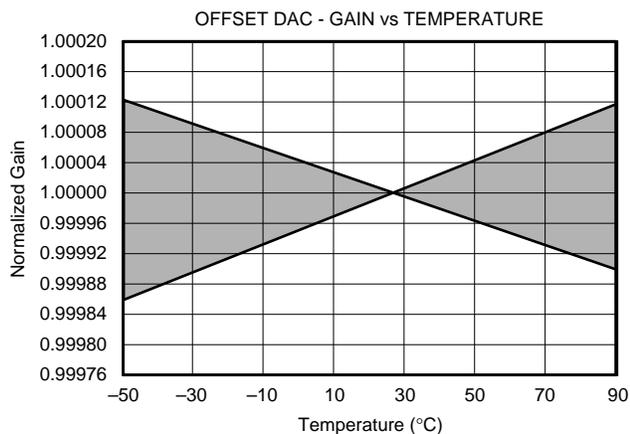
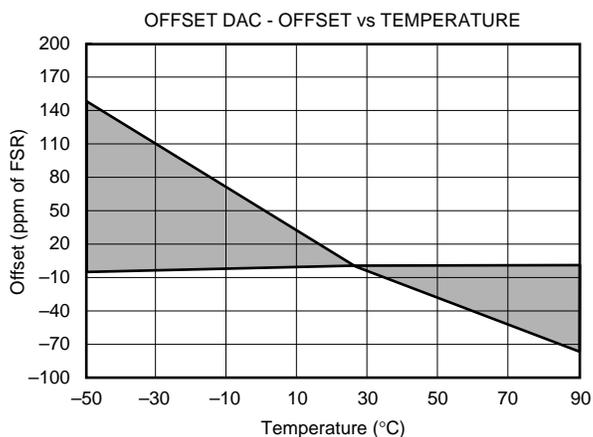
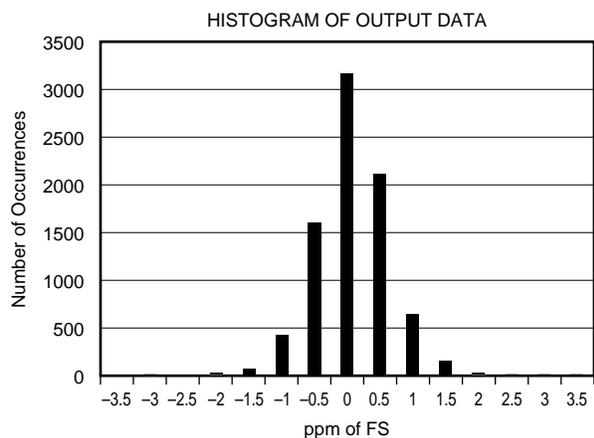
TYPICAL PERFORMANCE CURVES (Cont.)

All specifications, $AV_{DD} = +5V$, $DV_{DD} = +5V$, $f_{OSC} = 2.4576MHz$, $PGA = 1$, $f_{DATA} = 15Hz$, $V_{REF} \equiv (REF IN+) - (REF IN-) = +2.5V$, unless otherwise specified.



TYPICAL PERFORMANCE CURVES (Cont.)

All specifications, $AV_{DD} = +5V$, $DV_{DD} = +5V$, $f_{OSC} = 2.4576MHz$, $PGA = 1$, $f_{DATA} = 15Hz$, $V_{REF} \equiv (REF\ IN+) - (REF\ IN-) = +2.5V$, unless otherwise specified.



OVERVIEW

INPUT MULTIPLEXER

The input multiplexer provides for any combination of differential inputs to be selected on any of the input channels, as shown in Figure 1. In the ADS1240 and ADS1241, if channel 1 is selected as the positive differential input channel, any other channel can be selected as the negative differential input channel. Under this method, it is possible to have up to eight fully differential input channels.

In addition, current sources are supplied that will source or sink current to detect open or short circuits on the multiplexer pins.

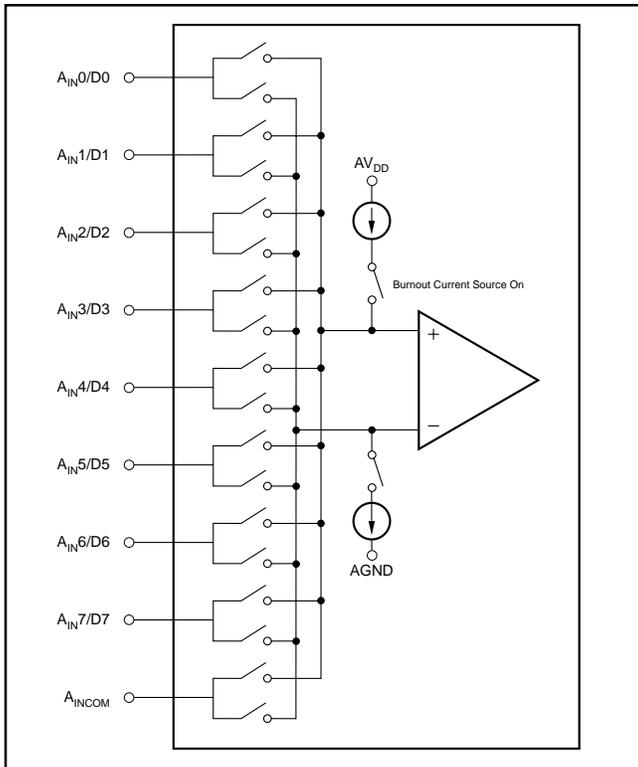


FIGURE 1. Input Multiplexer Configuration.

BURNOUT CURRENT SOURCES

When the Burnout bit is set in the ACR configuration register, two current sources inside the mux are enabled. The current source on the positive input channel sources approximately $2\mu\text{A}$ of current. The current source on the negative input channel sinks approximately $2\mu\text{A}$. This allows for the detection of an open circuit (full-scale reading) or short circuit (0V differential reading) on the input differential pair.

INPUT BUFFER

The input impedance of the ADS1240 and ADS1241 without the buffer is $5\text{M}\Omega/\text{PGA}$. With the buffer enabled the input voltage range is reduced, and the power-supply current is higher. The Buffer bit in the ACR register controls the state of

the buffer, but only if the BUFEN pin is enabled. The BUFEN pin must be tied HIGH to enable the input buffer. If the buffer enable pin is LOW, the software control bit has no effect.

PGA

The Programmable Gain Amplifier (PGA) can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128. Using the PGA can actually improve the effective resolution of the A/D converter. For instance, with a gain of 1, the effective bit resolution of the A/D converter is about $1\mu\text{V}$. Using the highest gain setting, it is possible to achieve an effective bit resolution of about 75nV . Without the PGA, this would require a 26-bit A/D converter. AV_{DD} current increases with higher PGA settings.

PGA OFFSET DAC

The input to the PGA can be shifted by half the full-scale input range of the PGA. The ODAC (Offset DAC) register is an 8-bit value; the MSB is the sign and the seven LSBs provide the magnitude of the offset.

MODULATOR

The modulator is a single-loop second-order system. The modulator runs at a clock speed (f_{MOD}) that is derived from the external clock (f_{OSC}). The frequency division is determined by the SPEED bit in the SETUP register.

CALIBRATION

SPEED BIT	f_{MOD}
0	$f_{\text{OSC}}/128$
1	$f_{\text{OSC}}/256$

The offset and gain errors in the ADS1240 and ADS1241, or the complete system, can be minimized with calibration. Internal calibration of the ADS1240 and ADS1241 is called self calibration. This is handled with three commands. One command does both offset and gain calibration. There is also a gain calibration command and an offset calibration command. Each calibration process takes $2 t_{\text{DATA}}$ periods to complete. Therefore, it takes $4 t_{\text{DATA}}$ periods to complete both an offset and gain calibration.

For system calibration, the appropriate signal must be applied to the inputs. The system offset command requires a “zero” input signal. It then computes an offset that will nullify offset in the system. The system gain command requires a “full-scale” input signal. It then computes a value to nullify gain errors in the system. Each of these calibrations will take $2 t_{\text{DATA}}$ periods to complete.

Calibration should be performed after power on, or a change in temperature.

DIGITAL FILTER

The ADS1240 and ADS1241 have a 1279 taps modified linear phase digital filter on board which a user can configure various output data rates. When 2.4576MHz crystal is used, the device can be programmed to an output data rate of 15Hz, 7.5Hz, or 3.75Hz. Under these conditions, the digital filter rejects both 50Hz and 60Hz interference down to at least -90dB of full-scale input. Table I shows the various conditions that user can configure ADS1240 and ADS1241 on-board digital filter to perform various data output rate to get different line rejection frequencies.

DATA OUTPUT RATE	-3dB BANDWIDTH	50Hz	60Hz	100Hz	120Hz
15Hz	14.6Hz	-95dB	-93dB	-107dB	-109dB
7.5Hz	3.44Hz	-109dB	-99dB	-109dB	-108dB
3.75	1.65Hz	-108dB	-111dB	-112dB	-109dB

TABLE I. Data Output Rate and their Typical Rejection Performance.

If a different data output rate is desired, a different crystal frequency. However, the rejection frequencies will shift accordingly. For example, 3.6864MHz crystal with default register condition will have:

$$(3.6864\text{MHz}/2.4576\text{MHz}) \cdot 15\text{Hz} = 22.5\text{Hz of data output rate}$$

and the first and second notch will be:

$$1.5 \cdot (50\text{Hz and } 60\text{Hz}) = 75\text{Hz and } 90\text{Hz}$$

EXTERNAL VOLTAGE REFERENCE

The voltage reference used for the ADS1240 and ADS1241 is external. The selection for the voltage reference, value is made through the ACR register.

The external voltage reference is differential and is represented by the voltage difference between the pins: $+V_{REF}$ and $-V_{REF}$. The absolute voltage on either pin $+V_{REF}$ or $-V_{REF}$ can range from AGND to AV_{DD} . However, the following limitations apply:

For $AV_{DD} = 5.0\text{V}$ and $RANGE = 0$ in the ACR, the differential V_{REF} must not exceed 2.5V.

For $AV_{DD} = 5.0\text{V}$ and $RANGE = 1$ in the ACR, the differential V_{REF} must not exceed 5V.

For $AV_{DD} = 3.0\text{V}$ and $RANGE = 0$ or 1 in the ACR, the differential V_{REF} must not exceed 1.25V.

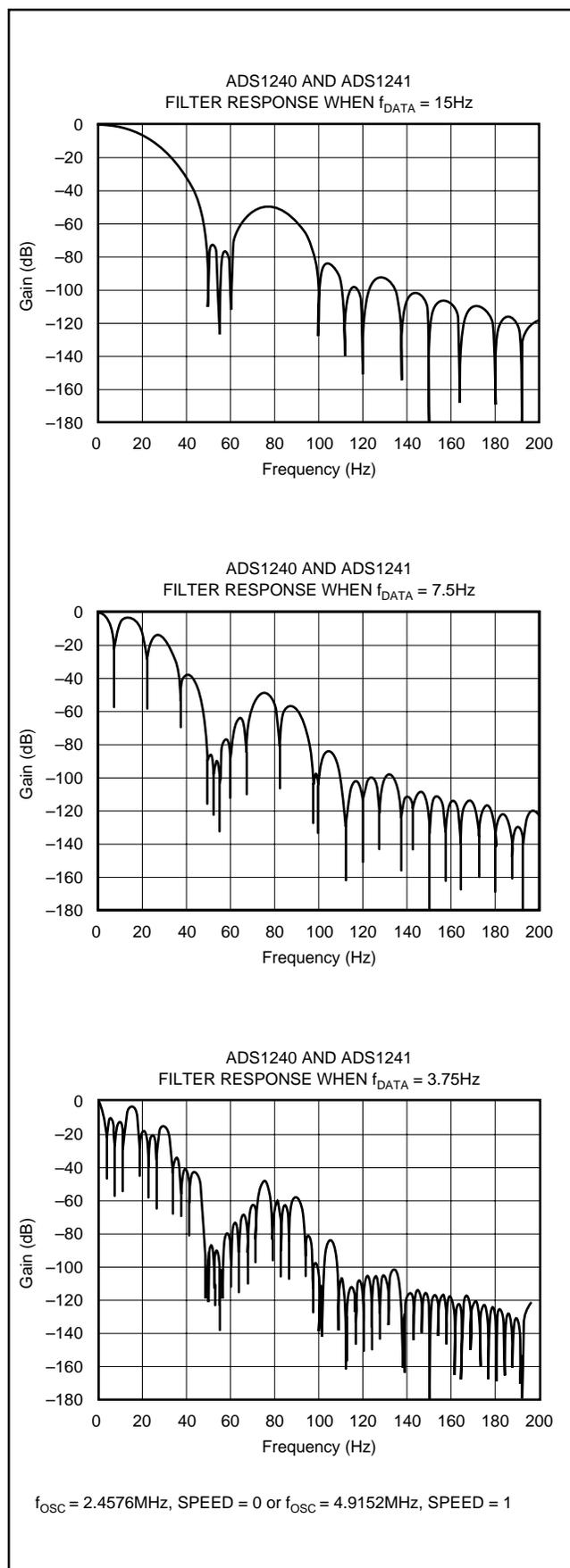


FIGURE 2. Filter Frequency Responses.

CLOCK GENERATOR

The clock source for the ADS1240 and ADS1241 can be provided from a crystal, ceramic resonator, oscillator, or external clock. When the clock source is a crystal or ceramic resonator, external capacitors must be provided to ensure start-up and stable clock frequency. This is shown in Figure 3 and Table II.

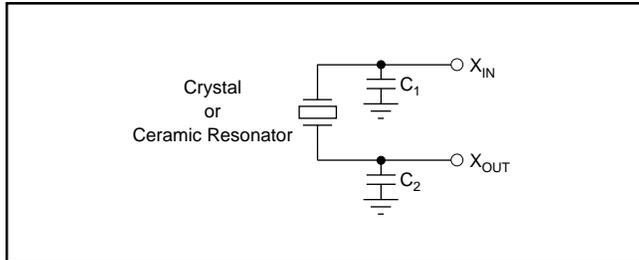


FIGURE 3. Crystal or Ceramic Resonator Connection.

CLOCK SOURCE	FREQUENCY	C ₁	C ₂	PART NUMBER
Crystal	2.4576	0-20pF	0-20pF	ECS, ECSD 2.45 - 32
Crystal	4.9152	0-20pF	0-20pF	ECS, ECSD 4.91
Crystal	4.9152	0-20pF	0-20pF	ECS, ECSD 4.91
Crystal	4.9152	0-20pF	0-20pF	CTS, MP 042 4M9182

TABLE II. Typical Clock Sources.

DATA I/O INTERFACE

The ADS1240 has four pins and the ADS1241 has eight pins which serve a dual purpose as both analog inputs and data I/O. These pins are powered from AV_{DD} and are configured through the IOCON, DIR, and DIO registers. These pins can be individually configured as either analog inputs or data I/O.

The IOCON register defines the pin as either an analog input or data I/O. The default power-up state is an analog input. If the pin is configured as an analog input in the IOCON register, the DIR and DIO registers have no effect on the state of the pin.

If the pin is configured as data I/O in the IOCON register, then DIR and DIO are used to control the state of the pin. The DIR register controls the direction of the data pin, either as an input or output. If the pin is configured as an input in the DIR register, then the corresponding DIO register bit reflects the state of the pin. If the pin is configured as an output in the DIR register, then the corresponding DIO register bit value determines the state of the output pin (0 = AGND, 1 = AV_{DD}).

It is still possible to perform A/D conversions on a pin configured as data I/O. This may be useful as a test mode, where the data I/O pin is driven and an A/D conversion is done on the pin.

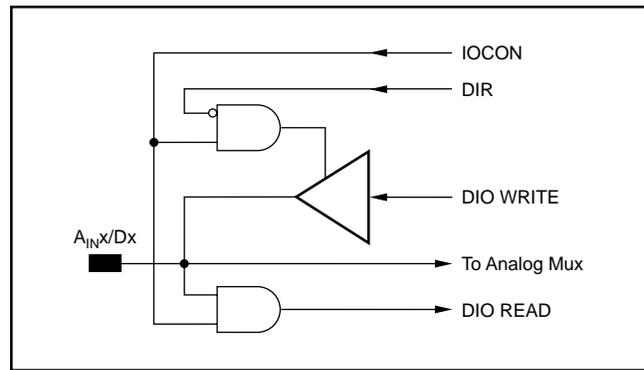


FIGURE 4. Analog/Data Interface Pin.

SERIAL INTERFACE

The serial interface is standard four-wire SPI compatible (D_{IN} , D_{OUT} , SCLK, and \overline{CS}). The ADS1240 and ADS1241 also offers the flexibility to select the polarity of the serial clock through the POL pin. The serial interface can be clocked up to $f_{osc}/4$.

DSYNC OPERATION

\overline{DSYNC} is used to provide for precise synchronization of the A/D conversion with an external event. Synchronization can be achieved either through the \overline{DSYNC} pin or the \overline{DSYNC} command. When the \overline{DSYNC} pin is used, the filter counter is reset on the falling edge of \overline{DSYNC} . The filter values are useless, they should be treated as if the input channel was changed. The modulator is held in reset until \overline{DSYNC} is taken HIGH. Synchronization occurs on the next rising edge of the system clock after \overline{DSYNC} is taken HIGH.

When the \overline{DSYNC} command is sent, the filter counter is reset on the edge of the last SCLK on the \overline{DSYNC} command. The modulator is held in RESET until the next edge of SCLK is detected. Synchronization occurs on the next rising edge of the system clock after the first SCLK after the \overline{DSYNC} command.

POWER-UP—SUPPLY VOLTAGE RAMP RATE

The power-on reset circuitry was designed to accommodate digital supply ramp rates as slow as 1V/10ms. To ensure proper operation, the power supply should ramp monotonically.

MEMORY

Sixteen registers directly control the various functions of the ADS1240 and ADS1241 can be directly read or written to. Collectively, the registers contain all the information needed to configure the part, such as data format, MUX settings, cal settings, data rate, etc.

ADS1240 AND ADS1241 REGISTER BANKS

The operation of the device is set up through individual registers. Collectively, the registers contain all the information needed to configure the part, such as data format, mux

settings, cal settings, data rate, etc. The set of the 16 registers are shown in Table III.

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00 _H	SETUP	ID	ID	ID	ID	BOCS	PGA2	PGA1	PGA0
01 _H	MUX	PSEL3	PSEL2	PSEL1	PSEL0	NSEL3	NSEL2	NSEL1	NSEL0
02 _H	ACR	DRDY	U/B	SPEED	BUFEN	BIT ORDER	RANGE	DR1	DR0
03 _H	ODAC	SIGN	OSET6	OSET5	OSET4	OSET3	OSET2	OSET1	OSET0
04 _H	DIO	DIO_7	DIO_6	DIO_5	DIO_4	DIO_3	DIO_2	DIO_1	DIO_0
05 _H	DIR	DIR_7	DIR_6	DIR_5	DIR_4	DIR_3	DIR_2	DIR_1	DIR_0
06 _H	IOCON	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
07 _H	OCR0	OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00
08 _H	OCR1	OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08
09 _H	OCR2	OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16
0A _H	FSR0	FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00
0B _H	FSR1	FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08
0C _H	FSR2	FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16
0D _H	DOR2	DOR23	DOR22	DOR21	DOR20	DOR19	DOR18	DOR17	DOR16
0E _H	DOR1	DOR15	DOR14	DOR13	DOR12	DOR11	DOR10	DOR09	DOR08
0F _H	DOR0	DOR07	DOR16	FSR21	DOR04	DOR03	DOR02	DOR01	DOR00

TABLE III. Registers.

DETAILED REGISTER DEFINITIONS

SETUP (Address 00_H) Setup Register

Reset Value = iiiii0000

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ID	ID	ID	ID	BOCS	PGA2	PGA1	PGA0

bit 7-4 Factory Programmed Bits

bit 3 BOCS: Burnout Current Source
0 = Disabled (default)
1 = Enabled

bit 2-0 PGA2: PGA1: PGA0: Programmable Gain Amplifier Gain Selection
000 = 1 (default)
001 = 2
010 = 4
011 = 8
100 = 16
101 = 32
110 = 64
111 = 128

MUX (Address 01_H) Multiplexer Control Register

Reset Value = 01_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PSEL3	PSEL2	PSEL1	PSEL0	NSEL3	NSEL2	NSEL1	NSEL0

bit 7-4 PSEL3: PSEL2: PSEL1: PSEL0: Positive Channel Select

0000 = AIN0 (default)
0001 = AIN1
0010 = AIN2
0011 = AIN3
0100 = AIN4
0101 = AIN5
0110 = AIN6
0111 = AIN7
1xxx = AINCOM (except when all bits are 1's)
1111 = Reserved

bit 3-0 NSEL3: NSEL2: NSEL1: NSEL0: Negative Channel Select

0000 = AIN0
0001 = AIN1 (default)
0010 = AIN2
0011 = AIN3
0100 = AIN4
0101 = AIN5
0110 = AIN6
0111 = AIN7
1xxx = AINCOM (except when all bits are 1's)
1111 = Reserved

ACR (Address 02_H) Analog Control Register

Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DRDY	U/B	SPEED	BUFEN	BIT ORDER	RANGE	DR1	DR0

- bit 7 **DRDY**: Data Ready (Read Only)
This bit duplicates the state of the $\overline{\text{DRDY}}$ signal.
- bit 6 **U/B**: Data Format
0 = Bipolar (default)
1 = Unipolar

U/B	ANALOG INPUT	DIGITAL OUTPUT
0	+FSR	0x7FFFFFFF
	Zero	0x000000
	-FSR	0x800000
1	+FSR	0xFFFFFFFF
	Zero	0x000000
	-FSR	0x000000

- bit 5 **SPEED**: Modulator Clock Speed
0 = $f_{\text{MOD}} = f_{\text{OSC}}/128$ (default)
1 = $f_{\text{MOD}} = f_{\text{OSC}}/256$
- bit 4 **BUFEN**: Buffen Enable
0 = Buffer Disabled (default)
1 = Buffered Enabled
- bit 3 **BIT ORDER**: Set Order Bits are Transmitted
0 = Most Significant Bit Transmitted First (default)
1 = Most Significant bit Transmitted First
Data is always shifted into the part most significant bit first. Data is always shifted out of the part most significant byte first. This configuration bit only controls the bit order within the byte of data that is shifted out.
- bit 2 **RANGE**: Range Select
0 = Full-Scale Output Range Equal to $\pm V_{\text{REF}}$ (default).
1 = Full-Scale Output Range Equal to $\pm 1/2 V_{\text{REF}}$
- bit 1-0 **DR1: DR0**: Data Rate ($f_{\text{OSC}} = 2.4576\text{MHz}$, $\text{SPEED} = 0$)
00 = 15Hz (default)
01 = 7.5Hz
10 = 3.75Hz
11 = Reserved

ODAC (Address 03_H) Offset DAC

Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SIGN	OSET6	OSET5	OSET4	OSET3	OSET2	OSET1	OSET0

- bit 7 **Offset Sign**
0 = Positive
1 = Negative
- bit 6 **Offset** = $\frac{V_{\text{REF}}}{2 \cdot \text{PGA}} \cdot \left(\frac{\text{Code}}{127} \right)$ RANGE = 0

Offset = $\frac{V_{\text{REF}}}{4 \cdot \text{PGA}} \cdot \left(\frac{\text{Code}}{127} \right)$ RANGE = 1

DIO (Address 04_H) Data I/O

Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0

If the IOCON register is configured for data, a value written to this register will appear on the data I/O pins if the pin is configured as an output in the DIR register. Reading this register will return the value of the data I/O pins.

DIR (Address 05_H) Direction Control for Data I/O

Reset Value = FF_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0

Each bit controls whether the data I/O pin is an output (= 0) or input (= 1). The default power-up state is as inputs.

IOCON (Address 06_H) I/O Configuration Register

Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0

- bit 7-0 **IO7: IO0**: Data I/O Configuration
0 = Analog (default)
1 = Data

Configuring the pin as a data I/O pin allows it to be controlled through the DIO and DIR registers.

OCR0 (Address 07_H) Offset Calibration Coefficient (Least Significant Byte)

Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00

OCR1 (Address 08_H) Offset Calibration Coefficient (Middle Byte)

Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08

OCR2 (Address 09_H) Offset Calibration Coefficient (Most Significant Byte)

Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16

FSR0 (Address 0A_H) Full-Scale Register
(Least Significant Byte)
Reset Value = 59_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00

FSR1 (Address 0B_H) Full-Scale Register
(Middle Byte)
Reset Value = 55_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08

FSR2 (Address 0C_H) Full-Scale Register
(Most Significant Byte)
Reset Value = 55_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16

DOR2 (Address 0D_H) Data Output Register
(Most Significant Byte) (Read Only)
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DOR23	DOR22	DOR21	DOR20	DOR19	DOR18	DOR17	DOR16

DOR1 (Address 0E_H) Data Output Register
(Middle Byte) (Read Only)
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DOR15	DOR14	DOR13	DOR12	DOR11	DOR10	DOR09	DOR08

DOR0 (Address 0F_H) Data Output Register
(Least Significant Byte) (Read Only)
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DOR07	DOR06	DOR05	DOR04	DOR03	DOR02	DOR01	DOR00

ADS1240 AND ADS1241 CONTROL

COMMAND DEFINITIONS

The commands listed in Table IV control the operations of the ADS1240 and ADS1241. Some of the commands are stand-alone commands (e.g., RESET) while others require additional bytes (e.g., WREG requires count, and the data bytes).

Operands:

n = count (0 to 127)

r = register (0 to 15)

x = don't care

COMMANDS	DESCRIPTION	OP CODE	2ND COMMAND BYTE
RDATA	Read Data	0000 0001 (01 _H)	—
RDATA C	Read Data Continuously	0000 0011 (03 _H)	—
STOPC	Stop Read Data Continuously	0000 1111 (0F _H)	—
RREG	Read from REG "rrrr"	0001 rrrr (1x _H)	xxxx_nnnn (# of regs-1)
WREG	Write to REG "rrrr"	0101 rrrr (5x _H)	xxxx_nnnn (# of regs-1)
SELF CAL	Self Cal Offset and Gain	1111 0000 (F0 _H)	—
SELF OCAL	Self Cal Offset	1111 0001 (F1 _H)	—
SELF GCAL	Self Cal Gain	1111 0010 (F2 _H)	—
SYSOCAL	Sys Cal Offset	1111 0011 (F3 _H)	—
SYSGCAL	Sys Cal Gain	1111 0100 (F4 _H)	—
DSYNC	Sync \overline{DRDY}	1111 1100 (FC _H)	—
SLEEP	Put in SLEEP Mode	1111 1101 (FD _H)	—
RESET	Reset to Power-Up Values	1111 1110 (FE _H)	—

NOTE: (1) The received data in format is always MSB First, the data out format is set by the BIT ORDER bit in ACR reg.

TABLE IV. Command Summary.

RDATA Read Data

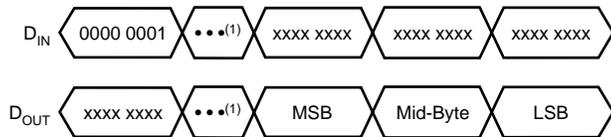
Description: Read a single data value from the Data Output Register (DOR) which is the most recent conversion result. This is a 24-bit value.

Operands: None

Bytes: 1

Encoding: 0000 0001

Data Transfer Sequence:



NOTE: (1) For wait time, refer to timing specification.

RDATA_C Read Data Continuous

Description: Read Data Continuous mode enables the continuous output of new data on each $\overline{\text{DRDY}}$. This command eliminates the need to send the Read Data Command on each $\overline{\text{DRDY}}$. This mode may be terminated by either the STOP Read Continuous command or the RESET command.

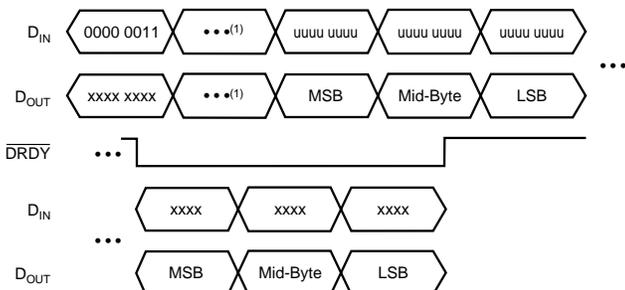
Operands: None

Bytes: 1

Encoding: 0000 0011

Data Transfer Sequence:

Command terminated when “uuuu uuuu” equals STOPC or RESET.



NOTE: (1) For wait time, refer to timing specification.

STOPC Stop Continuous

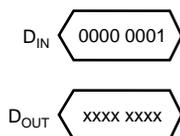
Description: Ends the continuous data output mode.

Operands: None

Bytes: 1

Encoding: 0000 1111

Data Transfer Sequence:



RREG Read from Registers

Description: Output the data from up to 16 registers starting with the register address specified as part of the instruction. The number of registers read will be one plus the second byte. If the count exceeds the remaining registers, the addresses will wrap back to the beginning.

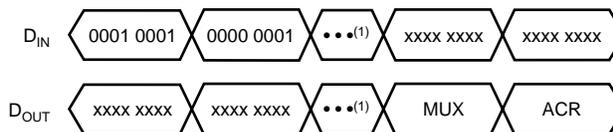
Operands: r, n

Bytes: 2

Encoding: 0001 rrrr xxxx nnnn

Data Transfer Sequence:

Read Two Registers Starting from Register 01_H (MUX)



NOTE: (1) For wait time, refer to timing specification.

WREG Write to Register

Description: Write to the registers starting with the register specified as part of the instruction. The number of registers that will be written is one plus the value of the second byte.

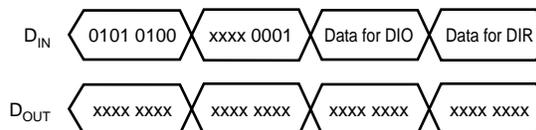
Operands: r, n

Bytes: 2

Encoding: 0101 rrrr xxxx nnnn

Data Transfer Sequence:

Write Two Registers Starting from 04_H (DIO)



SELFCAL Offset and Gain Self Calibration

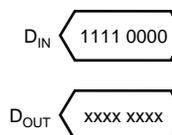
Description: Starts the process of self calibration. The Offset Control Register (OCR) and the Full-Scale Register (FSR) are updated with new values after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0000

Data Transfer Sequence:



SELFOCAL Offset Self Calibration

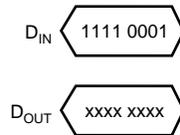
Description: Starts the process of self-calibration for offset. The Offset Control Register (OCR) is updated after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0001

Data Transfer Sequence:



SELFGCAL Gain Self Calibration

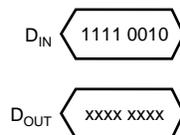
Description: Starts the process of self-calibration for gain. The Full-Scale Register (FSR) is updated with new values after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0010

Data Transfer Sequence:



SYSOCAL System Offset Calibration

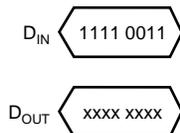
Description: Starts the system offset calibration process. For a system offset calibration the input should be set to 0V, and the ADS1240 and ADS1241 computes the OCR register value that will compensate for offset errors. The Offset Control Register (OCR) is updated after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0011

Data Transfer Sequence:



SYSGCAL System Gain Calibration

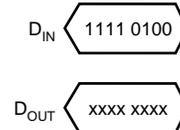
Description: Starts the system gain calibration process. For a system gain calibration, the input should be set to the reference voltage and the ADS1240 and ADS1241 computes the FSR register value that will compensate for gain errors. The FSR is updated after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0100

Data Transfer Sequence:



DSYNC Sync \overline{DRDY}

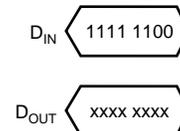
Description: Synchronizes the ADS1240 and ADS1241 to an external event.

Operands: None

Bytes: 1

Encoding: 1111 1100

Data Transfer Sequence:



SLEEP Sleep Mode

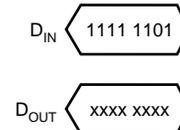
Description: Puts the ADS1240 and ADS1241 into a low power sleep mode. To exit sleep mode strobe SCLK.

Operands: None

Bytes: 1

Encoding: 1111 1101

Data Transfer Sequence:



RESET Reset to Powerup Values

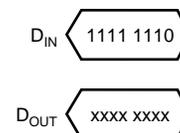
Description: Restore the registers to their power-up values. This command will also stop the Read Continuous mode.

Operands: None

Bytes: 1

Encoding: 1111 1110

Data Transfer Sequence:



MSB	LSB															
	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	x	rdata	x	rdatac	x	x	x	x	x	x	x	x	x	x	x	stopc
0001	rreg 0	rreg 1	rreg 2	rreg 3	rreg 4	rreg 5	rreg 6	rreg 7	rreg 8	rreg 9	rreg A	rreg B	rreg C	rreg D	rreg E	rreg F
0010	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0011	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0100	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0101	wreg 0	wreg 1	wreg 2	wreg 3	wreg 4	wreg 5	wreg 6	wreg 7	wreg 8	wreg 9	wreg A	wreg B	wreg C	wreg D	wreg E	wreg F
0110	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0111	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1000	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1001	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1010	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1011	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1100	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1101	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
1110	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1111	self cal	self ocal	self gcal	sys ocal	sys gcal	x	x	x	x	x	x	x	dsync	sleep	reset	x

x = Reserved

TABLE V. Command Map.

SERIAL PERIPHERAL INTERFACE

The Serial Peripheral Interface (SPI), allows a controller to communicate synchronously with the ADS1240 and ADS1241. The ADS1240 and ADS1241 operates in slave only mode.

SPI Transfer Formats

During an SPI transfer, data is simultaneously transmitted and received. The SCLK signal synchronizes shifting and sampling of the information on the two serial data lines: D_{IN} and D_{OUT} . The \overline{CS} signal allows individual selection of the ADS1240 or ADS1241 device; an ADS1240 or ADS1241 with \overline{CS} HIGH is not active on the bus.

Clock Phase and Polarity Controls (POL)

The clock polarity is specified by the POL pin, which selects an active HIGH or active LOW clock, and has no effect on the transfer format.

Serial Clock (SCLK)

SCLK, a Schmitt trigger input to the ADS1240 or ADS1241, is generated by the master device and synchronizes data transfer on the D_{IN} and D_{OUT} lines. When transferring data to or from the ADS1240 or ADS1241, burst mode may be used i.e., multiple bits of data may be transferred back-to-back with no delay in SCLKs or toggling of \overline{CS} .

Chip Select (\overline{CS})

The chip select (\overline{CS}) input of the ADS1240 or ADS1241 must be externally asserted before a master device can exchange data with the ADS1240 or ADS1241. \overline{CS} must be LOW before data transactions and must stay LOW for the duration of the transaction.

DIGITAL INTERFACE

The ADS1240 and ADS1241's programmable functions are controlled using a set of on-chip registers, as outlined previously. Data is written to these registers via the part's serial interface and read access to the on-chip registers is also provided by this interface.

The ADS1240 and ADS1241's serial interface consists of four signals: \overline{CS} , SCLK, D_{IN} , and D_{OUT} . The D_{IN} line is used for transferring data into the on-chip registers while the D_{OUT} line is used for accessing data from the on-chip registers. SCLK is the serial clock input for the device and all data transfers (either on D_{IN} or D_{OUT}) take place with respect to this SCLK signal.

The \overline{DRDY} line is used as a status signal to indicate when data is ready to be read from the ADS1240 and ADS1241's data register. \overline{DRDY} goes LOW when a new data word is available in the DOR register. It is reset HIGH when a read operation from the data register is complete. It also goes HIGH prior to the updating of the output register to indicate when not to read from the device to ensure that a data read is not attempted while the register is being updated.

\overline{CS} is used to select the device. It can be used to decode the ADS1240 and ADS1241 in systems where a number of parts are connected to the serial bus.

The timing specifications shows the timing diagram for interfacing to the ADS1240 or ADS1241 with \overline{CS} used to decode the part.

The ADS1240 or ADS1241 serial interface can operate in three-wire mode by tying the \overline{CS} input LOW. In this case, the SCLK, D_{IN} , and D_{OUT} lines are used to communicate with the ADS1240 and ADS1241, the status of \overline{DRDY} can be obtained by interrogating bit 7 of the M/DEC1 register (address 9_H). This scheme is suitable for interfacing to microcontrollers. If \overline{CS} is required as a decoding signal, it can be generated from a port bit.

DEFINITION OF TERMS

An attempt has been made to be consistent with the terminology used in this data sheet. In that regard, the definition of each term is given as follows:

Analog Input Voltage—the voltage at any one analog input relative to AGND.

Analog Input Differential Voltage—given by the following equation: $IN+ - IN-$. Thus, a positive digital output is produced whenever the analog input differential voltage is positive, while a negative digital output is produced whenever the differential is negative.

For example, when the converter is configured with a 2.5V reference and placed in a gain setting of 1, the positive full-scale output is produced when the analog input differential is 2.5V. The negative full-scale output is produced when the differential is $-2.5V$. In each case, the actual input voltages must remain within the AGND to AV_{DD} range.

Conversion Cycle—the term “conversion cycle” usually refers to a discrete A/D conversion operation, such as that performed by a successive approximation converter. As used here, a conversion cycle refers to the t_{DATA} time period. However, each digital output is actually based on the modulator results from several t_{DATA} time periods.

Data Rate—The rate at which conversions are completed. See definition for f_{DATA} .

Effective Resolution—the effective resolution of the ADS1240 and ADS1241 in a particular configuration can be expressed in two different units: bits rms (referenced to output) and V_{rms} (referenced to input). Computed directly from the converter’s output data, each is a statistical calculation. The conversion from one to the other is shown below.

BITS rms	BIPOLAR V_{rms}	UNIPOLAR V_{rms}
	RANGE = 0	RANGE = 0
	$\frac{\left(\frac{2 \cdot V_{REF}}{PGA}\right)}{10^{\left(\frac{6.02 \cdot ER}{20}\right)}}$	$\frac{\left(\frac{V_{REF}}{PGA}\right)}{10^{\left(\frac{6.02 \cdot ER}{20}\right)}}$
24	298nV	149nV
22	1.19 μ V	597nV
20	4.77 μ V	2.39 μ V
18	19.1 μ V	9.55 μ V
16	76.4 μ V	38.2 μ V
14	505 μ V	152.7 μ V
12	1.22mV	610 μ V

f_{OSC} —the frequency of the crystal oscillator or CMOS compatible input signal at the X_{IN} input of the ADS1240 and ADS1241.

f_{MOD} —the frequency or speed at which the modulator of the ADS1240 and ADS1241 is running. This depends on the SPEED bit as given by the following equation:

	SPEED = 0	SPEED = 1
mfactor	128	256

$$f_{MOD} = \frac{f_{OSC}}{\text{mfactor}}$$

f_{SAMP} —the frequency, or switching speed, of the input sampling capacitor. The value is given by one of the following equations:

PGA SETTING	SAMPLING FREQUENCY
1, 2, 4, 8	$f_{SAMP} = \frac{f_{OSC}}{\text{mfactor}}$
16	$f_{SAMP} = \frac{f_{OSC} \cdot 2}{\text{mfactor}}$
32	$f_{SAMP} = \frac{f_{OSC} \cdot 4}{\text{mfactor}}$
64, 128	$f_{SAMP} = \frac{f_{OSC} \cdot 8}{\text{mfactor}}$

f_{DATA} —the frequency of the digital output data produced by the ADS1240 and ADS1241, f_{DATA} is also referred to as the Data Rate.

Full-Scale Range (FSR)—as with most A/D converters, the full-scale range of the ADS1240 and ADS1241 is defined as the “input”, which produces the positive full-scale digital output minus the “input”, which produces the negative full-scale digital output.

For example, when the converter is configured with a 2.5V reference and is placed in a gain setting of 2, the full-scale range is: [1.25V (positive full-scale) minus -1.25V (negative full-scale)] = 2.5V.

Least Significant Bit (LSB) Weight—this is the theoretical amount of voltage that the differential voltage at the analog input would have to change in order to observe a change in the output data of one least significant bit. It is computed as follows:

$$\text{LSB Weight} = \frac{\text{Full-Scale Range}}{2^N}$$

where N is the number of bits in the digital output.

t_{DATA} —the inverse of f_{DATA} , or the period between each data output.

GAIN SETTING	5V SUPPLY ANALOG INPUT ⁽¹⁾			GENERAL EQUATIONS		
	FULL-SCALE RANGE	DIFFERENTIAL INPUT VOLTAGES ⁽²⁾	PGA OFFSET RANGE	FULL-SCALE RANGE	DIFFERENTIAL INPUT VOLTAGES ⁽²⁾	PGA SHIFT RANGE
1	5V	±2.5V	±1.25V	$\frac{2 \cdot V_{\text{REF}}}{\text{PGA}}$	$\frac{\pm V_{\text{REF}}}{\text{PGA}}$	$\frac{\pm V_{\text{REF}}}{2 \cdot \text{PGA}}$
2	2.5V	±1.25V	±0.625V			
4	1.25V	±0.625V	±312.5mV			
8	0.625V	±312.5mV	±156.25mV			
16	312.5mV	±156.25mV	±78.125mV	RANGE = 0		
32	156.25mV	±78.125mV	±39.0625mV	$\frac{V_{\text{REF}}}{\text{PGA}}$	$\frac{\pm V_{\text{REF}}}{2 \cdot \text{PGA}}$	$\frac{\pm V_{\text{REF}}}{4 \cdot \text{PGA}}$
64	78.125mV	±39.0625mV	±19.531mV			
128	39.0625mV	±19.531mV	±9.766mV			

NOTES: (1) With a 2.5V reference. (2) Refer to electrical specification for analog input voltage range.

TABLE VI. Full-Scale Range versus PGA Setting.

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