

## Precision, Low Drift 4-20mA TWO-WIRE TRANSMITTER

### FEATURES

- **INSTRUMENTATION AMPLIFIER INPUT:**
  - Low Offset Voltage,  $30\mu\text{V}$  max
  - Low Voltage Drift,  $0.75\mu\text{V}/^\circ\text{C}$  max
  - Low Nonlinearity, 0.01% max
- **TRUE TWO-WIRE OPERATION:**
  - Power and Signal on One Wire Pair
  - Current Mode Signal Transmission
  - High Noise Immunity
- **DUAL MATCHED CURRENT SOURCES**
- **WIDE SUPPLY RANGE: 11.6V to 40V**
- **SPECIFICATION RANGE:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$**
- **SMALL DIP-14 PACKAGE, CERAMIC AND PLASTIC**

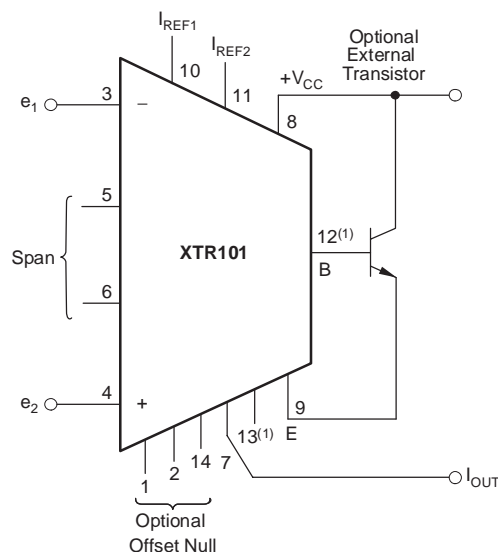
### APPLICATIONS

- **INDUSTRIAL PROCESS CONTROL:**
  - Pressure Transmitters
  - Temperature Transmitters
  - Millivolt Transmitters
- **RESISTANCE BRIDGE INPUTS**
- **THERMOCOUPLE INPUTS**
- **RTD INPUTS**
- **CURRENT SHUNT (mV) INPUTS**
- **PRECISION DUAL CURRENT SOURCES**
- **AUTOMATED MANUFACTURING**
- **POWER/PLANT ENERGY SYSTEM MONITORING**

### DESCRIPTION

The XTR101 is a microcircuit, 4-20mA, two-wire transmitter containing a high accuracy instrumentation amplifier (IA), a voltage-controlled output current source, and dual-matched precision current reference. This combination is ideally suited for remote signal conditioning of a wide variety of transducers such as thermocouples, RTDs, thermistors, and strain gauge bridges. State-of-the-art design and laser-trimming, wide temperature range operation, and small size make it very suitable for industrial process control applications. In addition, the optional external transistor allows even higher precision.

The two-wire transmitter allows signal and power to be supplied on a single wire pair by modulating the power-supply current with the input signal source. The transmitter is immune to voltage drops from long runs and noise from motors, relays, actuators, switches, transformers, and industrial equipment. It can be used by OEMs producing transmitter modules or by data acquisition system manufacturers.



NOTE: (1) Pins 12 and 13 are used for optional BW control.



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**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Power Supply, +V <sub>CC</sub>	40V
Input Voltage, e <sub>1</sub> or e <sub>2</sub>	$\geq V_{OUT}, \leq +V_{CC}$
Storage Temperature Range, Ceramic	–55°C to +165°C
Plastic	–55°C to +125°C
Lead Temperature (soldering, 10s) G, P	+300°C
(wave soldering, 3s) U	+260°C
Output Short-Circuit Duration	Continuous +V <sub>CC</sub> to I <sub>OUT</sub>
Junction Temperature	+165°C

<sup>(1)</sup> Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

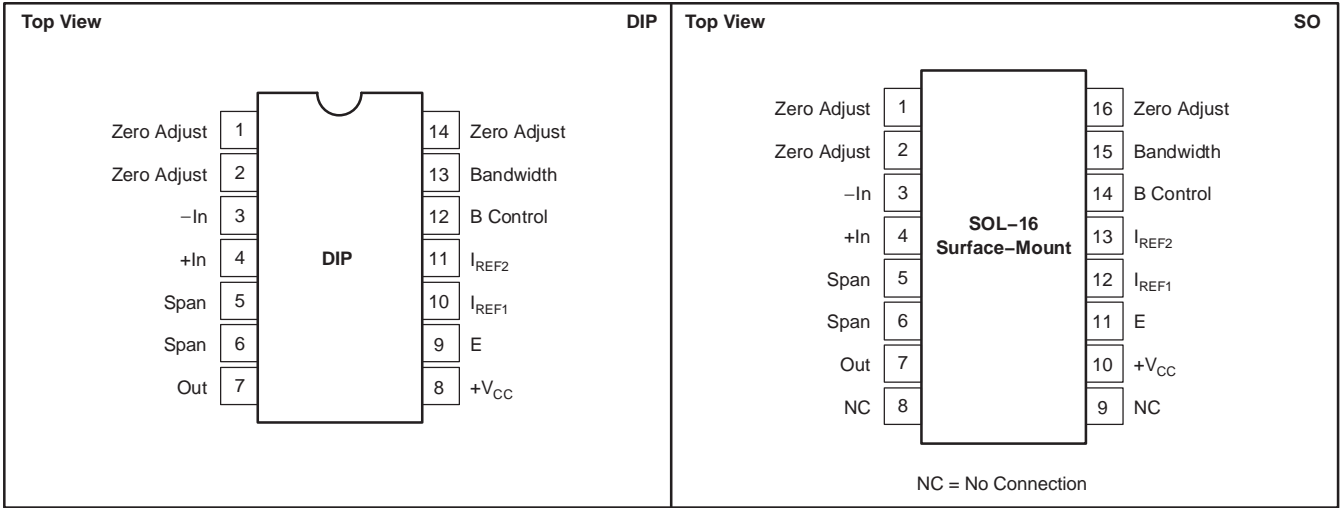
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**ORDERING INFORMATION**

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR <sup>(1)</sup>	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING
XTR101	Ceramic DIP-14	JD	–40°C to +85°C	XTR101AG
				XTR101BG
	Plastic DIP-14	N		XTR101AP
	SO-16	DW		XTR101AU

<sup>(1)</sup> For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

**PIN CONFIGURATION**



## ELECTRICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $+V_{CC} = 24\text{VDC}$ , and  $R_L = 100\Omega$  with external transistor connected, unless otherwise noted.

PARAMETER		CONDITIONS			XTR101AG			XTR101BG			XTR101AP			XTR101AU			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT AND LOAD CHARACTERISTICS																	
Current	Linear Operating Region	4		20	*		*	*		*	*		*		mA		
	Derated Performance	3.8		22	*		*	*		*	*		*		mA		
Current Limit			28	38		*	*		31	*		31	*	mA			
Offset Current Error vs Temperature	I <sub>OS</sub> , I <sub>O</sub> = 4mA ΔI <sub>OS</sub> /ΔT		±3.9 ±10.5	±10 ±20		±2.5 ±8	±6 ±15		±8.5 ±10.5	±19 ±20		±8.5 *	±19	μA ppm, FS/°C			
Full-Scale Output Current Error	Full-Scale = 20mA		±20	±40		±15	±30		±30	±60		±30	±60	μA			
Power-Supply Voltage	V <sub>CC</sub> , Pins 7 and 8, Compliance <sup>(1)</sup>	+11.6		±40	*		*	*		*	*		*	VDC			
Load Resistance	At V <sub>CC</sub> = +24V, I <sub>O</sub> = 20mA			600			*			*			*	Ω			
	At V <sub>CC</sub> = +40V, I <sub>O</sub> = 20mA			1400			*			*			*	Ω			
SPAN																	
Output Current Equation	R <sub>S</sub> in Ω, e <sub>1</sub> and e <sub>2</sub> in V				I <sub>O</sub> = 4mA + $\left[ 0.016\text{amps/volt} + \left( 40/R_S \right) \right] (e_2 - e_1)$												
Span Equation	R <sub>S</sub> in Ω				S = $\left[ 0.016\text{amps/volt} + \left( 40/R_S \right) \right]$										A/V		
vs Temperature	Excluding TCR of R <sub>S</sub>		±30	±100		*	*	*	*	*	*	*	*	ppm/°C			
Untrimmed Error <sup>(2)</sup>	ε <sub>SPAN</sub>	-5	-2.5	0	*	*	*	*	*	*	*	*	*	%			
Nonlinearity	ε <sub>NONLINEARITY</sub>			0.01		*	*		*	*		*	*	%			
Hysteresis			0			*			*			*		%			
Dead Band			0			*			*			*		%			
INPUT CHARACTERISTICS																	
Impedance: Differential			0.4    3			*			*			*		GΩ    pF			
Common-Mode			10    3			*			*			*		GΩ    pF			
Voltage Range, Full-Scale	Δe = (e <sub>2</sub> - e <sub>1</sub> ) <sup>(3)</sup>	0		1	*		*	*	*	*	*	*	*	V			
Offset Voltage	V <sub>OS</sub>		±30	±60		±20	±30		*	±100		*	±100	μV			
vs Temperature	ΔV <sub>OS</sub> /ΔT		±0.75	±1.5		±0.35	±0.75		*	*		*	*	μV/°C			
Power-Supply Rejection	ΔV <sub>CC</sub> /PSRR = V <sub>OS</sub> Error	110	125		*	*	*	*	122	*	*	122	*	dB			
Bias Current	I <sub>B</sub>		60	150		*	*		*	*		*	*	nA			
vs Temperature	ΔI <sub>B</sub> /ΔT		0.30	1		*	*		*	*		*	*	nA/°C			
Offset Current	I <sub>OSI</sub>		10	±30		*	±20		*	*		*	*	nA			
vs Temperature	ΔI <sub>OSI</sub> /ΔT		0.1	0.3		*	*		*	*		*	*	nA/°C			
Common-Mode Rejection <sup>(4)</sup>	DC	90	100		*	*		*	*		*	*		dB			
Common-Mode Range	e <sub>1</sub> and e <sub>2</sub> with Respect to Pin 7	4		6	*		*	*	*	*	*	*	*	V			
CURRENT SOURCES																	
Magnitude			1			*			*			*		mA			
Accuracy	V <sub>CC</sub> = 24V, V <sub>PIN 8</sub> - V <sub>PIN 10, 11</sub> = 19V, R <sub>2</sub> = 5kΩ, see Figure 5		±0.06	±0.1 7		±0.02 5	±0.075		±0.2	±0.37		±0.2	±0.37	%			
vs Temperature			±50	±80		±30	±50		*	*		*	*	ppm/°C			
vs V <sub>CC</sub>			±3			*			*			*		ppm/V			
vs Time			±8			*			*			*		ppm/month			
Compliance Voltage Ratio Match	With Respect to Pin 7 Tracking	0	V <sub>CC</sub> - 3.5		*		*	*	*	*	*	*	*	V			
Accuracy	(1 - I <sub>REF1</sub> /I <sub>REF2</sub> ) × 100%		±0.01 4	±0.0 6		±0.00 9	±0.04		±0.031	±0.088		±0.031	±0.088	%			
vs Temperature				±15		*	10		*	*		*	*	ppm/°C			
vs V <sub>CC</sub>			±10			*			*			*		ppm/V			
vs Time			±1			*			*			*		ppm/month			
Output Impedance		10	20		*	*		*	15		*	15		MΩ			
TEMPERATURE RANGE																	
Specification		-40		+85	*		*	*		*	*		*	°C			
Operating		-55		+125	*		*	-40		+85	-40		+85	°C			
Storage		-55		+165	*		*	-55		+125	-55		+125	°C			

\* Same as XTR101AG.

(1) See the Typical Characteristics.

(2) Span error shown is untrimmed and may be adjusted to zero.

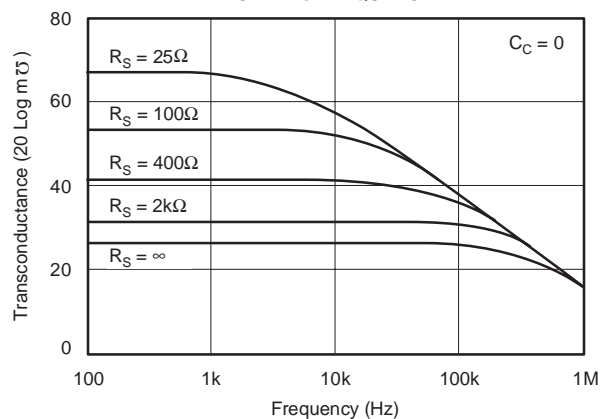
(3)  $e_1$  and  $e_2$  are signals on the -In and +In terminals with respect to the output, pin 7. While the maximum permissible  $\Delta e$  is 1V, it is primarily intended for much lower signal levels, for instance, 10mV or 50mV full-scale for the XTR101A and XTR101B grades, respectively. 2mV FS is also possible with the B grade, but accuracy will degrade due to possible errors in the low value span resistance and very high amplification of offset, drift, and noise.

(4) Offset voltage is trimmed with the application of a 5V common-mode voltage. Thus, the associated common-mode error is removed. See the *Application Information* section.

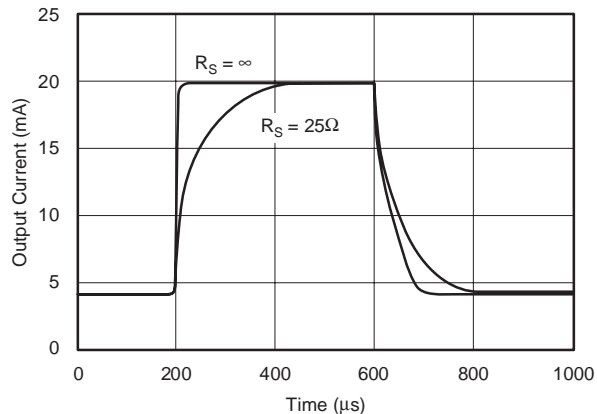
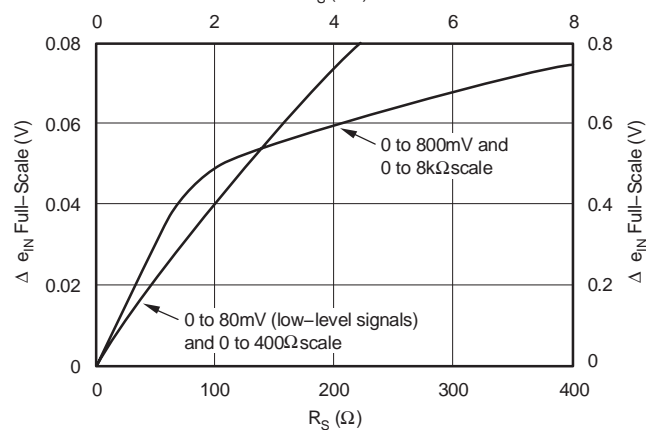
## TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$  and  $V_{CC} = 24\text{VDC}$ , unless otherwise noted.

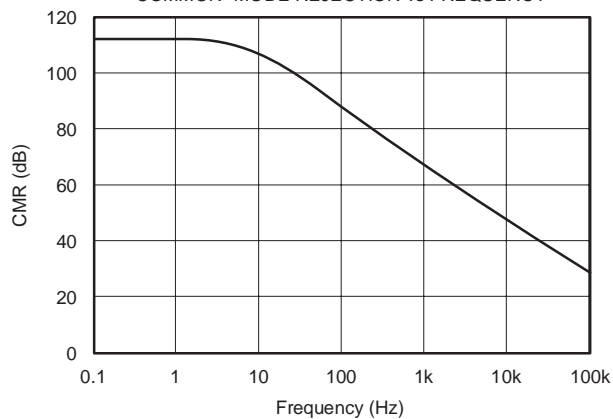
SPAN vs FREQUENCY



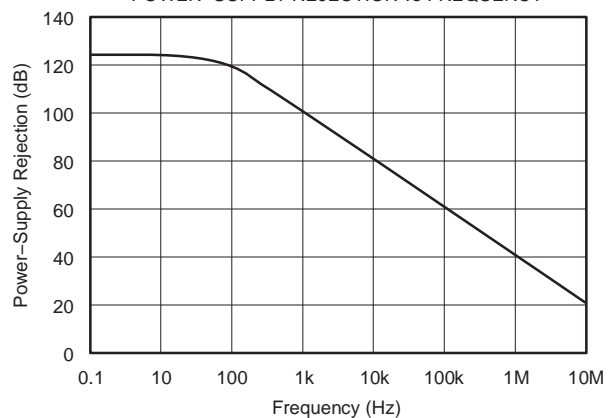
STEP RESPONSE

FULL-SCALE INPUT VOLTAGE vs  $R_S$ 

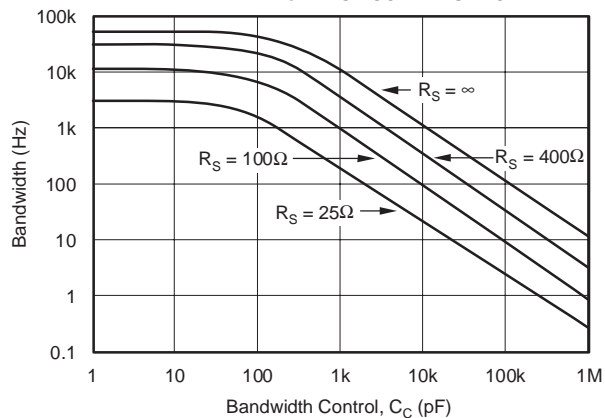
COMMON-MODE REJECTION vs FREQUENCY



POWER-SUPPLY REJECTION vs FREQUENCY

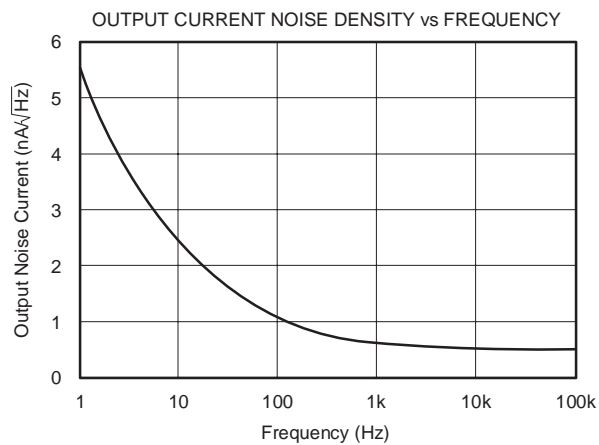
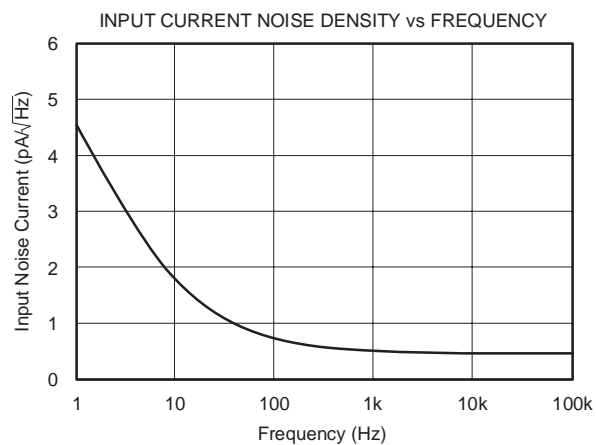
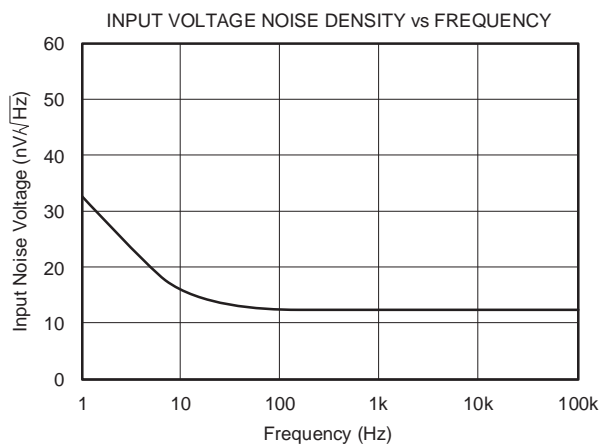


BANDWIDTH vs PHASE COMPENSATION



## TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +3.3\text{V}$ , and  $V_{IO} = +3.3\text{V}$ , unless otherwise noted.



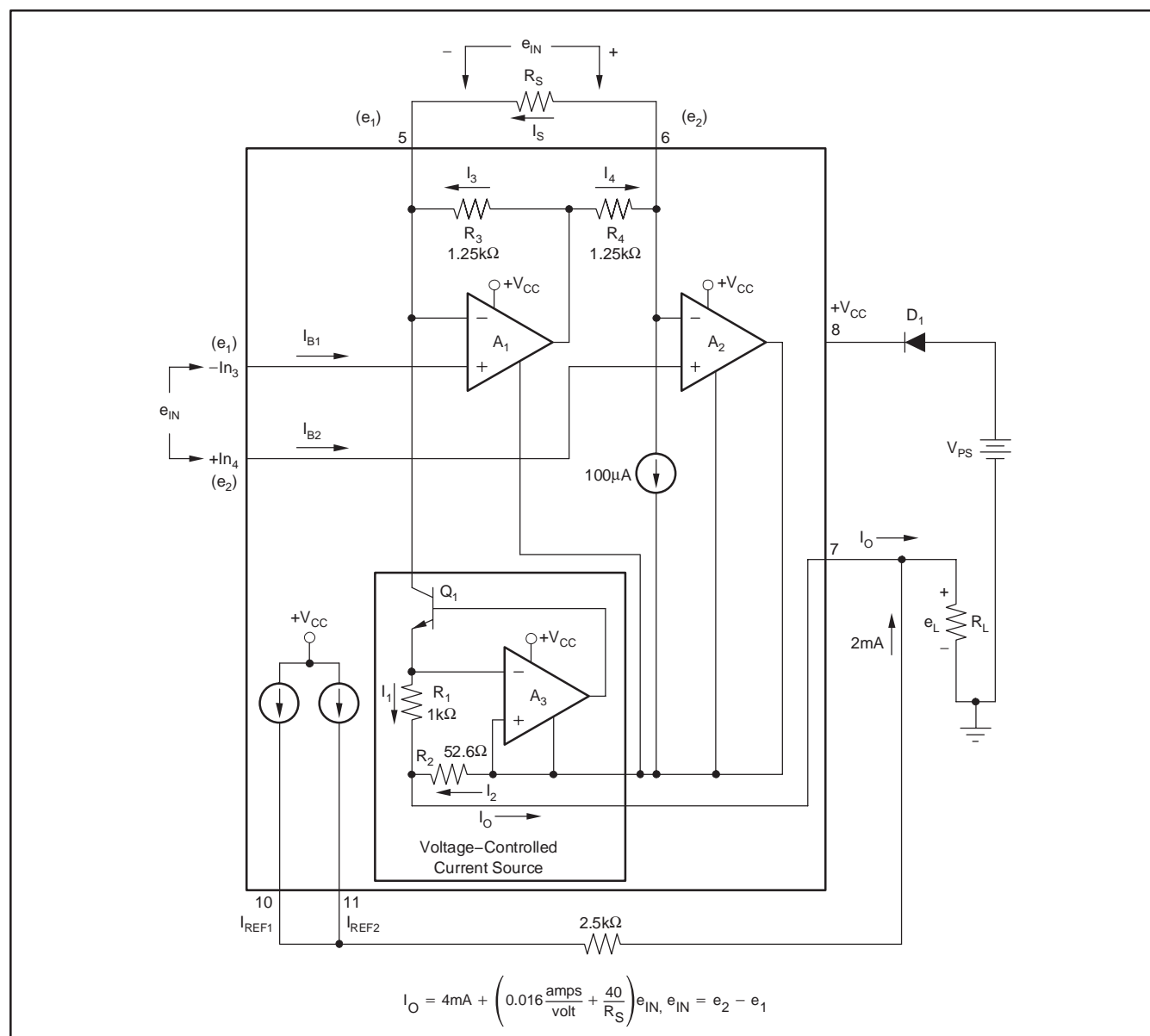
## THEORY OF OPERATION

A simplified schematic of the XTR101 is shown in Figure 1. Basically, the amplifiers  $A_1$  and  $A_2$  act as a single power-supply instrumentation amplifier controlling a current source,  $A_3$  and  $Q_1$ . Operation is determined by an internal feedback loop.  $e_1$  applied to pin 3 will also appear at pin 5, and similarly,  $e_2$  will appear at pin 6. Therefore, the current in  $R_S$  (the span setting resistor) will be  $I_S = (e_2 - e_1)/R_S = e_{IN}/R_S$ . This current combines with the current  $I_3$  to form  $I_1$ . The circuit is configured such that  $I_2$  is 19 times  $I_1$ . From this point, the derivation of the transfer function is straightforward but lengthy. The result is shown in Figure 1.

Examination of the transfer function shows that  $I_O$  has a lower range-limit of 4mA when  $e_{IN} = e_2 - e_1 = 0V$ . This 4mA is composed of 2mA quiescent current exiting pin 7 plus 2mA from the current sources. The upper range limit of  $I_O$  is set to 20mA by the proper selection of  $R_S$  based on the upper range limit of  $e_{IN}$ . Specifically,  $R_S$  is chosen for a 16mA output current span for the given full-scale input voltage span.

For example,  $\left(0.016 \frac{\text{amps}}{\text{volt}} + \frac{40}{R_S}\right)(e_{IN} \text{ full-scale}) = 16\text{mA}$ .

Note that since  $I_O$  is unipolar,  $e_2$  must be kept larger than  $e_1$  (that is,  $e_2 \geq e_1$  or  $e_{IN} \geq 0$ ). Also note that in order not to exceed the output upper range limit of 20mA,  $e_{IN}$  must be kept less than 1V when  $R_S = \infty$  and proportionately less as  $R_S$  is reduced.



### Figure 1. Simplified Schematic of the XTR101

## INSTALLATION AND OPERATING INSTRUCTIONS

### BASIC CONNECTION

See Figure 1 for the basic connection of the XTR101. A difference voltage applied between input pins 3 and 4 will cause a current of 4-20mA to circulate in the two-wire output loop (through  $R_L$ ,  $V_{PS}$ , and  $D_1$ ). For applications requiring moderate accuracy, the XTR101 operates very cost-effectively with just its internal drive transistor. For more demanding applications (high accuracy in high gain), an external NPN transistor can be added in parallel with the internal one. This keeps the heat out of the XTR101 package and minimizes thermal feedback to the input stage. Also, in such applications where the  $e_N$  full-scale is small ( $< 50\text{mV}$ ) and  $R_{SPAN}$  is small ( $< 150\Omega$ ), caution should be taken to consider errors from the external span circuit plus high amplification of offset drift and noise.

### OPTIONAL EXTERNAL TRANSISTOR

The optional external transistor, when used, is connected in parallel with the XTR101 internal transistor. The purpose is to increase accuracy by reducing heat change inside the XTR101 package as the output current spans from 4-20mA. Under normal operating conditions, the internal transistor is never completely turned off, as shown in Figure 2. This maintains frequency stability with varying external transistor characteristics and wiring capacitance. The actual current sharing between internal and external transistors is dependent on two factors:

1. relative geometry of emitter areas, and
2. relative package dissipation (case size and thermal conductivity).

For best results, the external device should have a larger base-emitter area and smaller package. It will, upon turn-on, take about  $[0.95(I_O - 3.3\text{mA})]\text{mA}$ . However, it will heat faster and take a greater share after a few seconds.

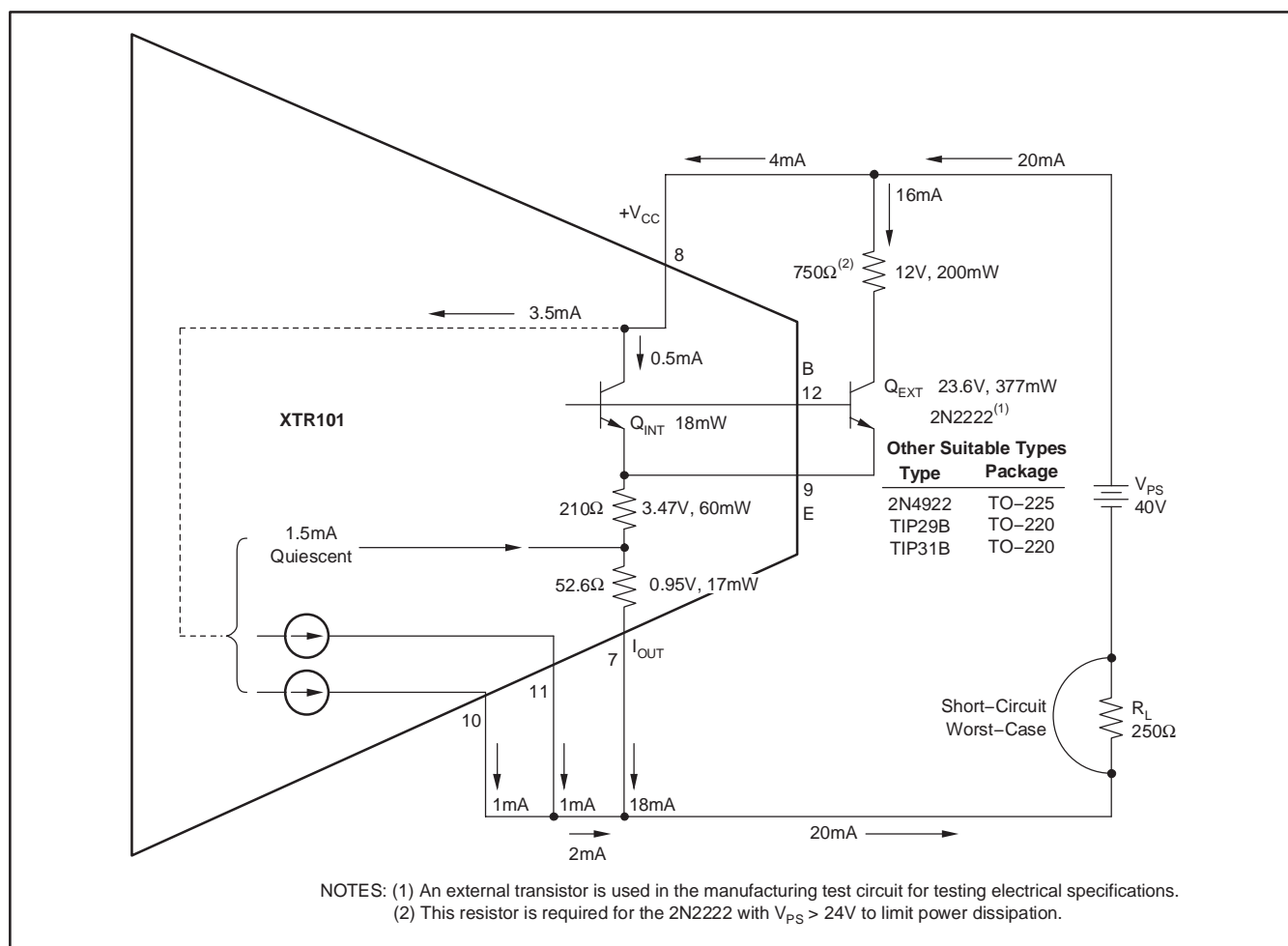


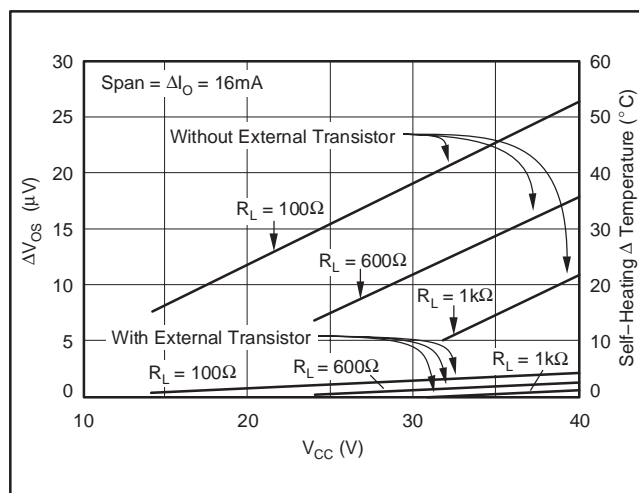
Figure 2. Power Calculation of the XTR101 with an External Transistor

Although any NPN of suitable power rating will operate with the XTR101, two readily available transistors are recommended:

1. 2N2222 in the TO-18 package. For power-supply voltages above 24V, a 750Ω, 1/2W resistor should be connected in series with the collector. This will limit the power dissipation to 377mW under the worst-case conditions; see Figure 2. Thus, the 2N2222 will safely operate below its 400mW rating at the upper temperature of +85°C. Heat sinking the 2N2222 will result in greatly reduced accuracy improvement and is not recommended.
2. TIP29B in the TO-220 package. This transistor will operate over the specified temperature and output voltage range without a series collector resistor. Heat sinking the TIP29B will result in slightly less accuracy improvement. It can be done, however, when mechanical constraints require it.

### ACCURACY WITH AND WITHOUT AN EXTERNAL TRANSISTOR

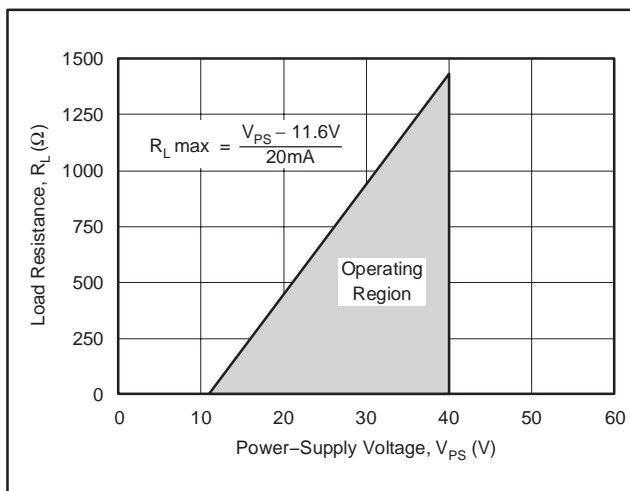
The XTR101 has been tested in a circuit using an external transistor. The relative difference in accuracy with and without an external transistor is shown in Figure 3. Notice that a dramatic improvement in offset voltage change with supply voltage is evident for any value of load resistor.



**Figure 3. Thermal Feedback Due to Change in Output Current**

### MAJOR POINTS TO CONSIDER WHEN USING THE XTR101

1. The leads to  $R_S$  should be kept as short as possible to reduce noise pick-up and parasitic resistance.
2.  $+V_{CC}$  should be bypassed with a 0.01μF capacitor as close to the unit as possible (pin 8 to pin 7).
3. Always keep the input voltages within their range of linear operation, +4V to +6V ( $e_1$  and  $e_2$  measured with respect to pin 7).
4. The maximum input signal level ( $e_{INFS}$ ) is 1V with  $R_S = \infty$  and proportionally less as  $R_S$  decreases.
5. Always return the current references (pins 10 and 11) to the output (pin 7) through an appropriate resistor. If the references are not used for biasing or excitation, connect them together to pin 7. Each reference must have between 0V and  $+(V_{CC} - 4V)$  with respect to pin 7.
6. Always choose  $R_L$  (including line resistance) so that the voltage between pins 7 and 8 ( $+V_{CC}$ ) remains within the 11.6V to 40V range as the output changes between the 4-20mA range (as shown in Figure 4).
7. It is recommended that a reverse polarity protection diode ( $D_1$  in Figure 1) be used. This will prevent damage to the XTR101 caused by a momentary (such as a transient) or long-term application of the wrong polarity of voltage between pins 7 and 8.
8. Consider PC board layout which minimizes parasitic capacitance, especially in high gain.



**Figure 4. Power-Supply Operating Range**



## SELECTING THE $R_S$

$R_{SPAN}$  is chosen so that a given full-scale input span ( $e_{INFS}$ ) will result in the desired full-scale output span of  $\Delta I_{OFS}$ :

$$\left[ \left( 0.016 \frac{\text{amps}}{\text{volt}} \right) + \left( \frac{40}{R_S} \right) \right] \Delta e_{IN} = \Delta I_O = 16\text{mA}.$$

Solving for  $R_S$ :

$$R_S = \frac{40}{\Delta I_O / \Delta e_{IN} - 0.016 \frac{\text{amps}}{\text{volt}}} \quad (1)$$

For example, if  $\Delta e_{INFS} = 100\text{mV}$  for  $\Delta I_{OFS} = 16\text{mA}$ ,

$$\begin{aligned} R_S &= \frac{40}{(16\text{mA}/100\text{mV}) - 0.016} = \frac{40}{0.16 - 0.016} \\ &= \frac{40}{0.144} = 278\Omega \end{aligned}$$

See the Typical Characteristics for a plot of  $R_S$  vs  $\Delta e_{INFS}$ . Note that in order not to exceed the 20mA upper range limit,  $e_{IN}$  must be less than 1V when  $R_S = \infty$  and proportionately smaller as  $R_S$  decreases.

## BIASING THE INPUTS

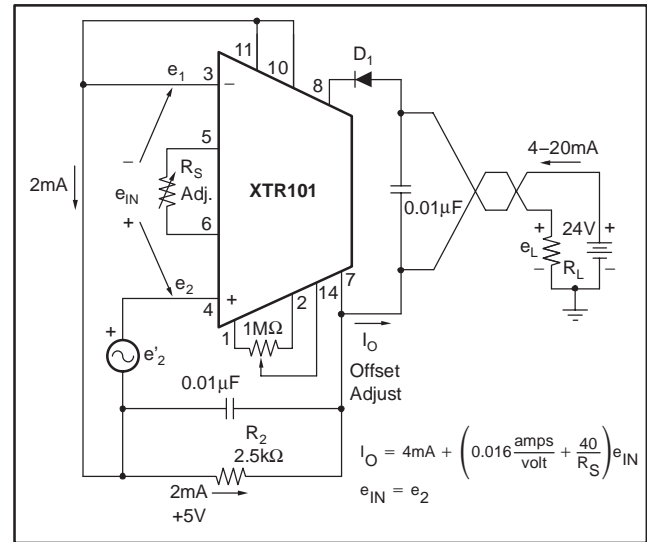
Because the XTR operates from a single supply, both  $e_1$  and  $e_2$  must be biased approximately 5V above the voltage at pin 7 to assure linear response. This is easily done by using one or both current sources and an external resistor,  $R_2$ . Figure 5 shows the simplest case—a floating voltage source  $e'_2$ . The 2mA from the current sources flows through the 2.5k $\Omega$  value of  $R_2$  and both  $e_1$  and  $e_2$  are raised by the required 5V with respect to pin 7. For linear operation the constraint is:

$$+4\text{V} \leq e_1 \leq +6\text{V}$$

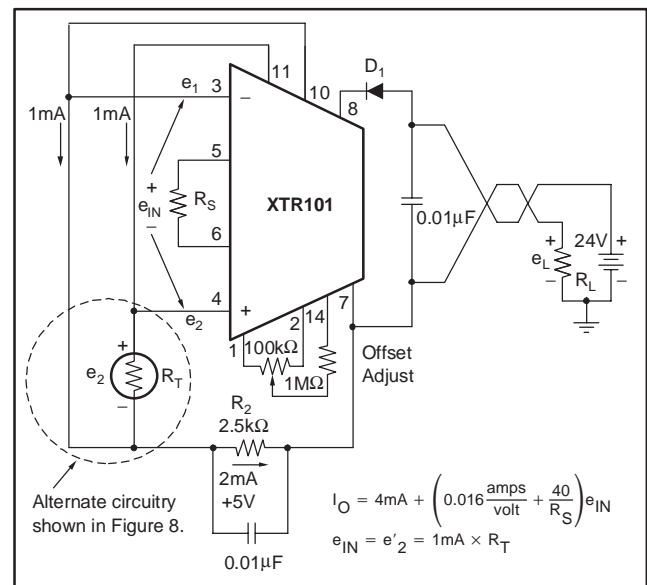
$$+4\text{V} \leq e_2 \leq +6\text{V}$$

The offset adjustment is used to remove the offset voltage of the input amplifier. When the input differential voltage ( $e_{IN}$ ) equals zero, adjust for 4mA output.

Figure 6 shows a similar connection for a resistive transducer. The transducer could be excited either by one (as shown) or both current sources. Also, the offset adjustment has higher resolution compared to Figure 5.



**Figure 5. Basic Connection for Floating Voltage Source**



**Figure 6. Basic Connection for Resistive Source**

## CMV AND CMR

The XTR101 is designed to operate with a nominal 5V common-mode voltage at the input and will function properly with either input operating over the range of 4V to 6V with respect to pin 7. The error caused by the 5V CMV is already included in the accuracy specifications.

If the inputs are biased at some other CMV, then an input offset error term is  $(\text{CMV} - 5)/\text{CMRR}$ , where CMR is in dB, and CMRR is in V/V.

## SIGNAL SUPPRESSION AND ELEVATION

In some applications, it is desired to have suppressed zero range (input signal elevation) or elevated zero range (input signal suppression). This is easily accomplished with the XTR101 by using the current sources to create the suppression/elevation voltage. The basic concept is shown in Figure 7 and Figure 8(a). In this example, the sensor voltage is derived from  $R_T$  (a thermistor, RTD, or other variable resistance element) and excited by one of the 1mA current sources. The other current source is used to create the elevated zero range voltage. Figure 8(b), (c), and (d) show some of the possible circuit variations. These circuits have the desirable feature of noninteractive span and suppression/elevation adjustments.

Note: It is not recommended to use the optional offset voltage null (pins 1, 2, and 14) for elevation/suppression. This trim capability is used only to null the amplifier's input offset voltage. In many applications the already low offset voltage (typically 20 $\mu$ V) will not need to be nulled at all. Adjusting the offset voltage to non-zero values will disturb the voltage drift by  $\pm 0.3\mu$ V/ $^{\circ}$ C per 100 $\mu$ V or induced offset.

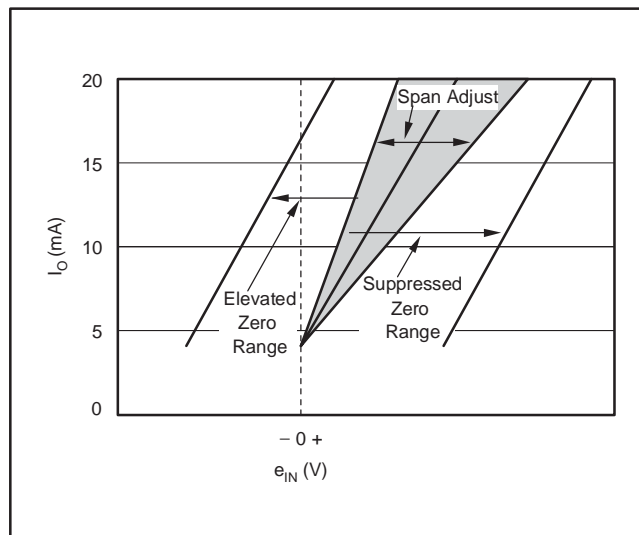


Figure 7. Elevation and Suppression Graph

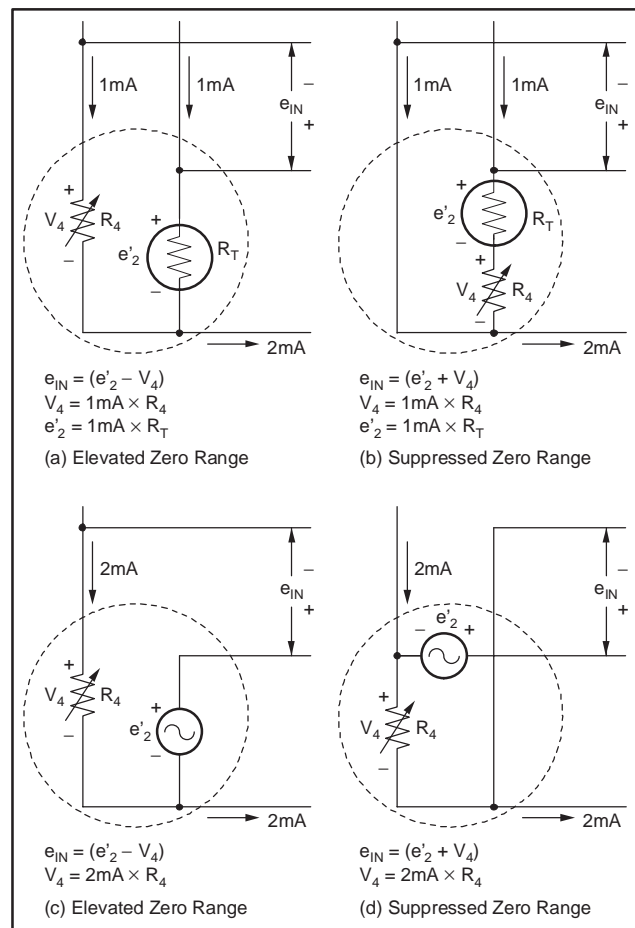


Figure 8. Elevation and Suppression Circuits

## APPLICATION INFORMATION

The small size, low offset voltage and drift, excellent linearity, and internal precision current sources make the XTR101 ideal for a variety of two-wire transmitter applications. It can be used by OEMs producing different types of transducer transmitter modules and by data acquisition systems manufacturers who gather transducer data. Current-mode transmission greatly reduces noise interference. The two-wire nature of the device allows economical signal conditioning at the transducer. Thus the XTR101 is, in general, very suitable for individualized and special-purpose applications.

## EXAMPLE 1

An RTD transducer is shown in Figure 9.

Given a process with temperature limits of +25°C and +150°C, configure the XTR101 to measure the temperature with a platinum RTD which produces 100Ω at 0°C and 200Ω at +266°C (obtained from standard RTD tables). Transmit 4mA for +25°C and 20mA for +150°C.

### COMPUTING $R_S$ :

The sensitivity of the RTD is  $\Delta R/\Delta T = 100\Omega/266^\circ\text{C}$ . When excited with a 1mA current source for a 25°C to 150°C range (a 125°C span), the span of  $e_{IN}$  is  $1\text{mA} \times (100\Omega/266^\circ\text{C}) \times 125^\circ\text{C} = 47\text{mV} = \Delta e_{IN}$ .

From Equation 1,  $R_S = \frac{40}{\Delta I_O/\Delta e_{IN} - 0.016 \frac{\text{amps}}{\text{volt}}}$

$$R_S = \frac{40}{16\text{mA}/47\text{mV} - 0.016\text{A/V}} = \frac{40}{0.3244} = 123.3\Omega$$

Span adjustment (calibration) is accomplished by trimming  $R_S$ .

### COMPUTING $R_4$ :

$$\begin{aligned} \text{At } +25^\circ\text{C}, e'_2 &= 1\text{mA}(R_T + \Delta R_T) \\ &= 1\text{mA} \left[ 100\Omega + \frac{100\Omega}{266^\circ\text{C}} \times 25^\circ\text{C} \right] \\ &= 1\text{mA}(109.4\Omega) = 109.4\text{mV} \end{aligned}$$

In order to make the lower range limit of 25°C correspond to the output lower range limit of 4mA, the input circuitry shown in Figure 9 is used.

$e_{IN}$ , the XTR101 differential input, is made 0 at 25°C or:

$$\begin{aligned} e'_{2 \text{ } 25^\circ\text{C}} - V_4 &= 0 \\ \text{thus, } V_4 &= e'_{2 \text{ } 25^\circ\text{C}} = 109.4\text{mV} \\ R_4 &= \frac{V_4}{1\text{mA}} = \frac{109.4\text{mV}}{1\text{mA}} = 109.4\Omega \end{aligned}$$

### COMPUTING $R_2$ AND CHECKING CMV:

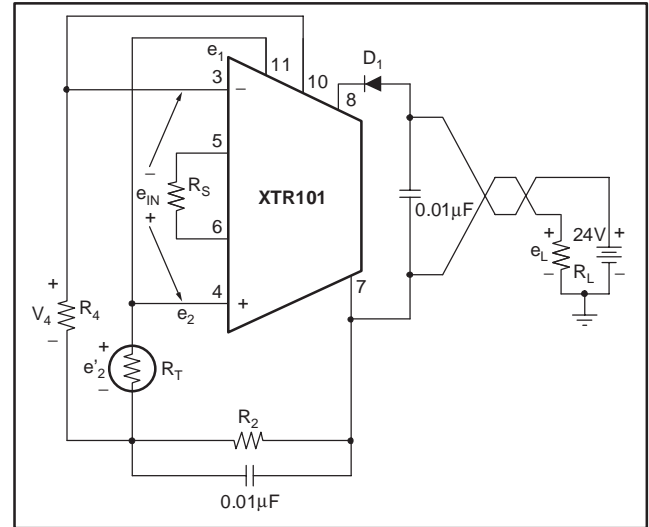
$$\begin{aligned} \text{At } +25^\circ\text{C}, e'_2 &= 109.4\text{mV} \\ \text{At } +150^\circ\text{C}, e'_2 &= 1\text{mA}(R_T + \Delta R_T) \\ &= 1\text{mA} \left[ 100\Omega + \frac{100\Omega}{266^\circ\text{C}} \times 150^\circ\text{C} \right] \\ &= 156.4\text{mV} \end{aligned}$$

Since both  $e'_2$  and  $V_4$  are small relative to the desired 5V common-mode voltage, they may be ignored in computing  $R_2$  as long as the CMV is met.

$$R_2 = \frac{5\text{V}}{2\text{mA}} = 2.5\text{k}\Omega$$

$$\begin{aligned} e_2 \text{ min} &= 5\text{V} + 0.1094\text{V} \\ e_2 \text{ max} &= 5\text{V} + 0.1564\text{V} \\ e_1 &= 5\text{V} + 0.1094\text{V} \end{aligned}$$

The 4V to 6V CMV requirement is met.

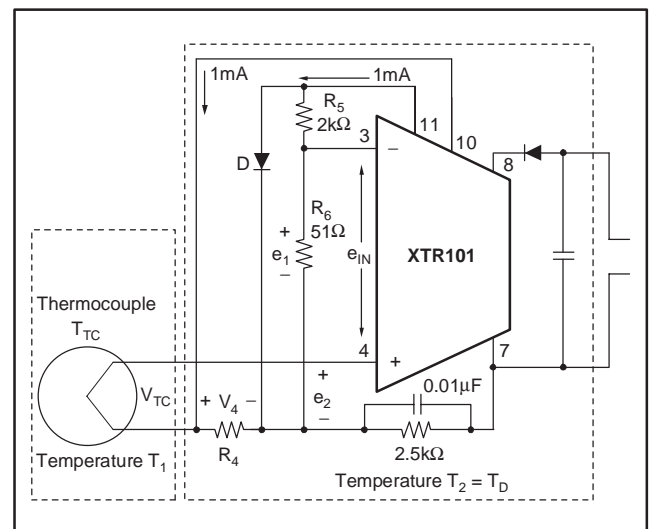


**Figure 9. Circuit for Example 1**

## EXAMPLE 2

A thermocouple transducer is shown in Figure 10.

Given a process with temperature ( $T_1$ ) limits of 0°C and +1000°C, configure the XTR101 to measure the temperature with a type J thermocouple that produces a 58mV change for 1000°C change. Use a semiconductor diode for cold junction compensation to make the measurement relative to 0°C. This is accomplished by supplying a compensating voltage ( $V_{R6}$ ) equal to that normally produced by the thermocouple with its cold junction ( $T_2$ ) at ambient. At a typical ambient of +25°C, this is 1.28mV (obtained from standard thermocouple tables with reference junction of 0°C). Transmit 4mA for  $T_1 = 0^\circ\text{C}$  and 20mA for  $T_1 = +1000^\circ\text{C}$ . Note:  $e_{IN} = e_2 - e_1$  indicates that  $T_1$  is relative to  $T_2$ .



**Figure 10. Thermocouple Input Circuit with Two Temperature Regions and Diode (D) Cold Junction Compensation**

**ESTABLISHING  $R_S$ :**

The input full-scale span is 58mV ( $\Delta e_{INFS} = 58\text{mV}$ ).

$R_S$  is found from Equation 1.

$$R_S = \frac{40}{\Delta I_O / \Delta e_{IN} - 0.016 \frac{\text{amps}}{\text{volt}}} = \frac{40}{16\text{mA}/58\text{mV} - 0.016\text{A/V}} = \frac{40}{0.2599} = 153.9\Omega$$

**SELECTING  $R_4$ :**

$R_4$  is chosen to make the output 4mA at  $T_{TC} = 0^\circ\text{C}$  ( $V_{TC} = -1.28\text{mV}$ ) and  $T_D = +25^\circ\text{C}$  ( $V_D = 0.6\text{V}$ ); see Figure 10.

$V_{TC}$  will be  $-1.28\text{mV}$  when  $T_{TC} = 0^\circ\text{C}$  and the reference junction is at  $+25^\circ\text{C}$ .  $e_1$  must be computed for the condition of  $T_D = +25^\circ\text{C}$  to make  $e_{IN} = 0\text{V}$ .

$$V_{D\ 25^\circ\text{C}} = 600\text{mV}$$

$$e_{1\ 25^\circ\text{C}} = 600\text{mV} \left( \frac{51}{2051} \right) = 14.9\text{mV}$$

$$e_{IN} = e_2 - e_1 = V_{TC} + V_4 - e_1$$

With  $e_{IN} = 0$  and  $V_{TC} = -1.28\text{mV}$ ,

$$V_4 = e_1 + e_{IN} - V_{TC} = 14.9\text{mV} + 0\text{V} - (-1.28\text{mV})$$

$$1\text{mA}(R_4) = 16.18\text{mV}$$

$$R_4 = 16.18\Omega$$

**COLD JUNCTION COMPENSATION:**

A temperature reference circuit is shown in Figure 11.

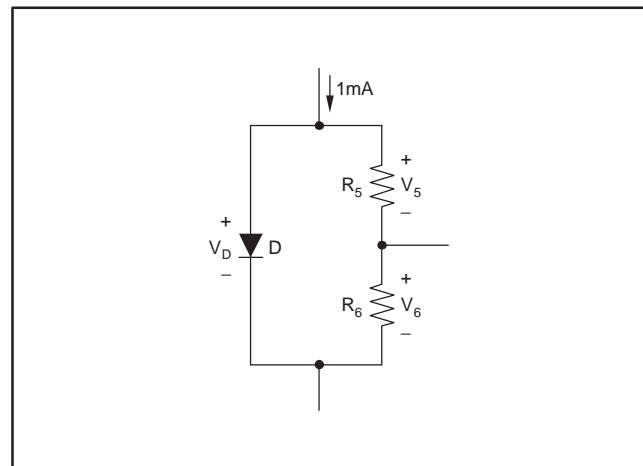
The diode voltage has the form:

$$V_D = \frac{KT}{q} \ln \frac{I_{DIODE}}{I_{SAT}}$$

Typically at  $T_2 = +25^\circ\text{C}$ ,  $V_D = 0.6\text{V}$  and  $\Delta V_D / \Delta T = -2\text{mV}/^\circ\text{C}$ .  $R_5$  and  $R_6$  form a voltage divider for the diode voltage  $V_D$ . The divider values are selected so that the gradient  $\Delta V_D / \Delta T$  equals the gradient of the thermocouple at the reference temperature. At  $+25^\circ\text{C}$  this is approximately  $52\mu\text{V}/^\circ\text{C}$  (obtained from a standard thermocouple table); therefore,

$$\begin{aligned} \frac{\Delta T_C}{\Delta T} &= \frac{\Delta V_D}{\Delta T} \left( \frac{R_6}{R_5 + R_6} \right) \\ \frac{52\mu\text{V}}{^\circ\text{C}} &= \frac{2000\mu\text{V}}{^\circ\text{C}} \left( \frac{R_6}{R_5 + R_6} \right) \end{aligned} \quad (2)$$

$R_5$  is chosen as  $2\text{k}\Omega$  to be much larger than the resistance of the diode. Solving for  $R_6$  yields  $51\Omega$ .



**Figure 11. Cold Junction Compensation Circuit**

**THERMOCOUPLE BURN-OUT INDICATION**

In process control applications it is desirable to detect when a thermocouple has burned out. This is typically done by forcing the two-wire transmitter current to either limit when the thermocouple impedance goes very high. The circuits of Figure 16 and Figure 17 inherently have downscale indication. When the impedance of the thermocouple gets very large (open) the bias current flowing into the + input (large impedance) will cause  $I_O$  to go to its lower range limit value (about 3.8mA). If upscale indication is desired, the circuit of Figure 18 should be used. When  $T_C$  opens, the output will go to its upper range limit value (about 25mA or higher).

**OPTIONAL INPUT OFFSET VOLTAGE TRIM**

The XTR101 has provisions for nulling the input offset voltage associated with the input amplifiers. In many applications the already low offset voltages ( $30\mu\text{V}$  max for the B grade and  $60\mu\text{V}$  max for the A grade) will not need to be nulled at all. The null adjustment can be done with a potentiometer at pins 1, 2, and 14; see Figure 5 and Figure 6. Either of these two circuits may be used. NOTE: It is not recommended to use this input offset voltage nulling capability for elevation or suppression. See the *Signal Suppression and Elevation* section for the proper techniques.

## OPTIONAL BANDWIDTH CONTROL

Low-pass filtering is recommended where possible and can be done by either one of two techniques; see Figure 12.  $C_2$  connected to pins 3 and 4 will reduce the bandwidth with a cutoff frequency given by:

$$f_{CO} = \frac{15.9}{(R_1 + R_2 + R_3 + R_4)(C_2 + 3pF)}$$

This method has the disadvantage of having  $f_{CO}$  vary with  $R_1$ ,  $R_2$ ,  $R_3$ ,  $R_4$ , and it may require large values of  $R_3$  and  $R_4$ . The other method, using  $C_1$ , will use smaller values of capacitance and is not a function of the input resistors. It is, however, more subject to nonlinear distortion caused by slew rate limiting. This is normally not a problem with the slow signals associated with most process control transducers. The relationship between  $C_1$  and  $f_{CO}$  is shown in the Typical Characteristics.

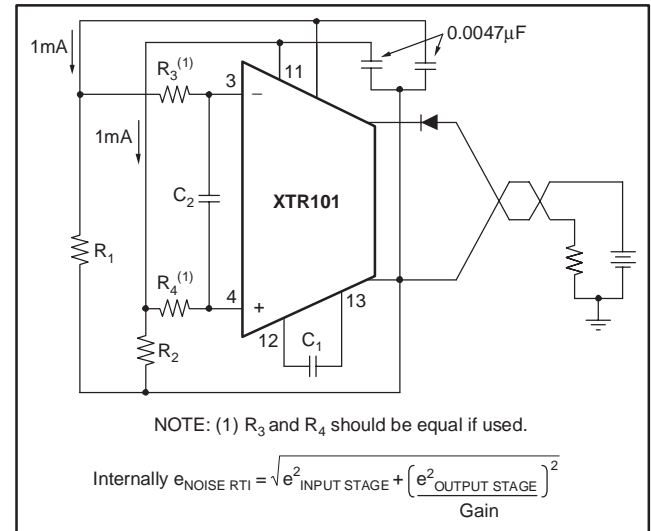


Figure 12. Optional Filtering

## APPLICATION CIRCUITS

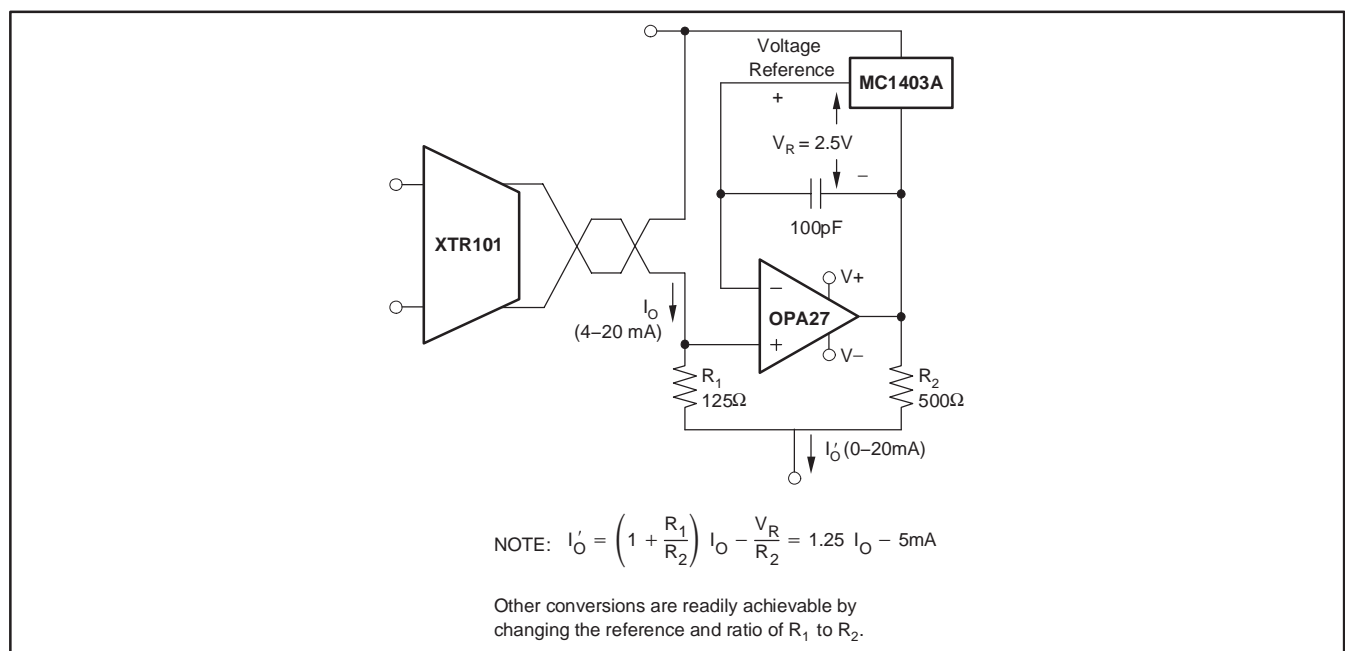


Figure 13. 0-20mA Output Converter

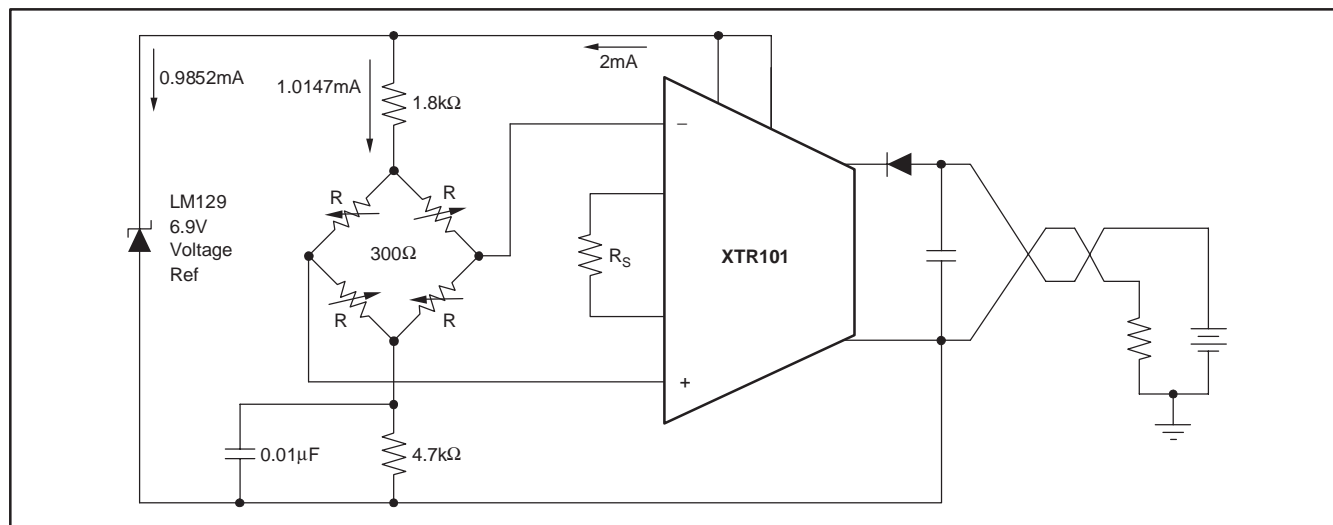


Figure 14. Bridge Input, Voltage Excitation

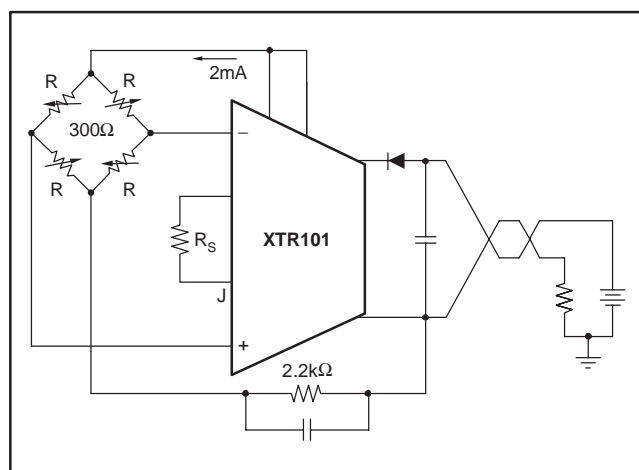


Figure 15. Bridge Input, Current Excitation

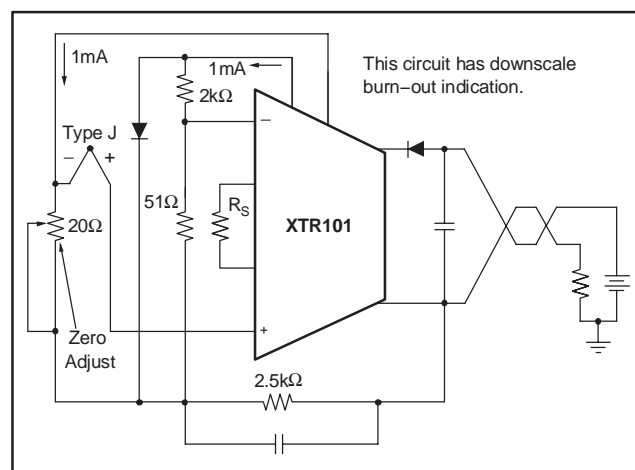


Figure 17. Thermocouple Input with Diode Cold Junction Compensation

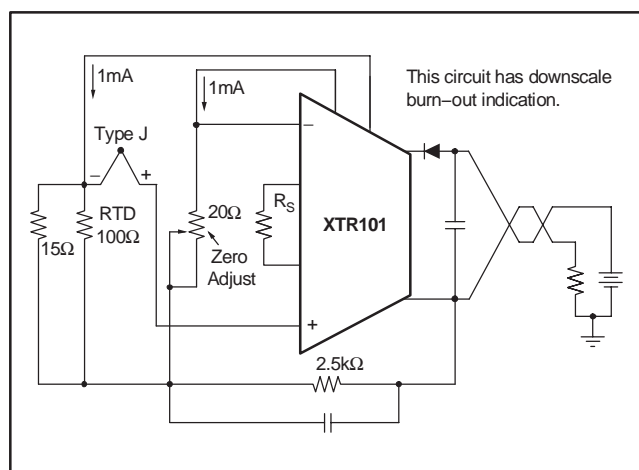


Figure 16. Thermocouple Input with RTD Cold Junction Compensation

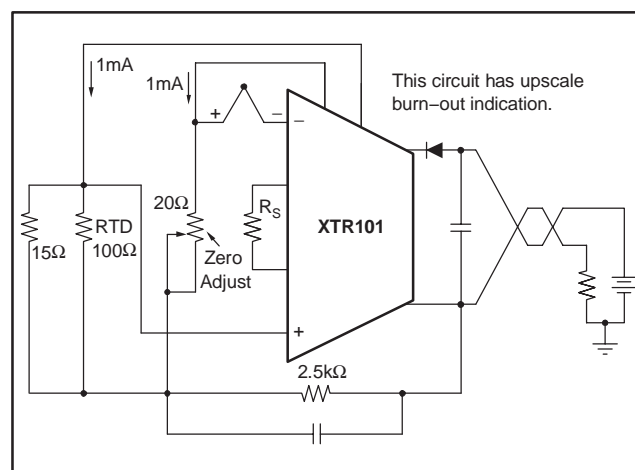


Figure 18. Thermocouple Input with RTD Cold Junction Compensation

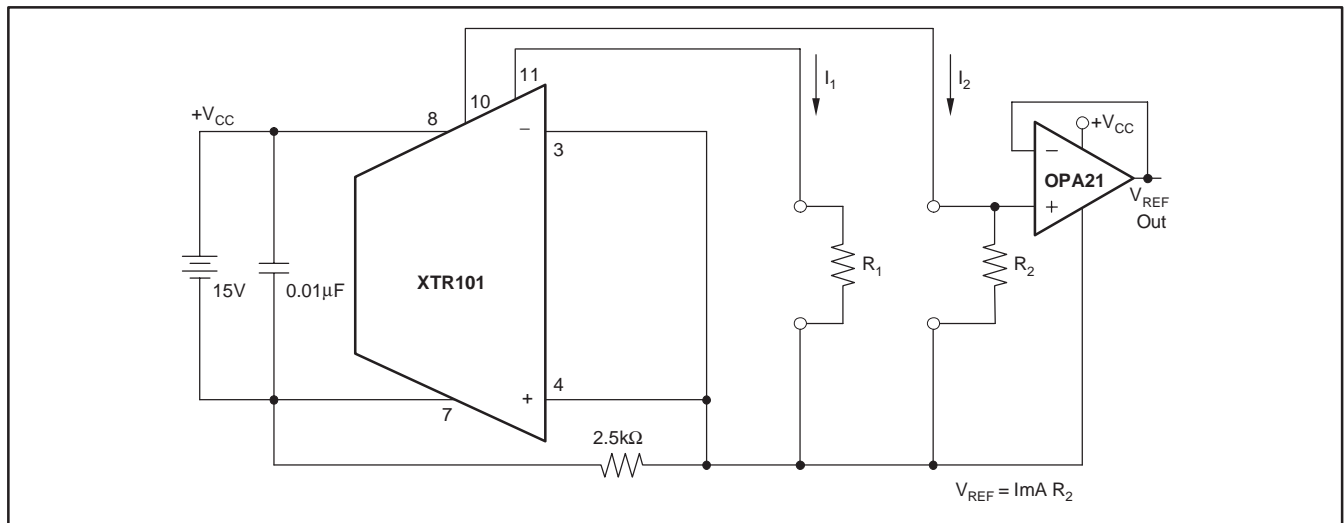


Figure 19. Dual Precision Current Sources Operated from One Supply

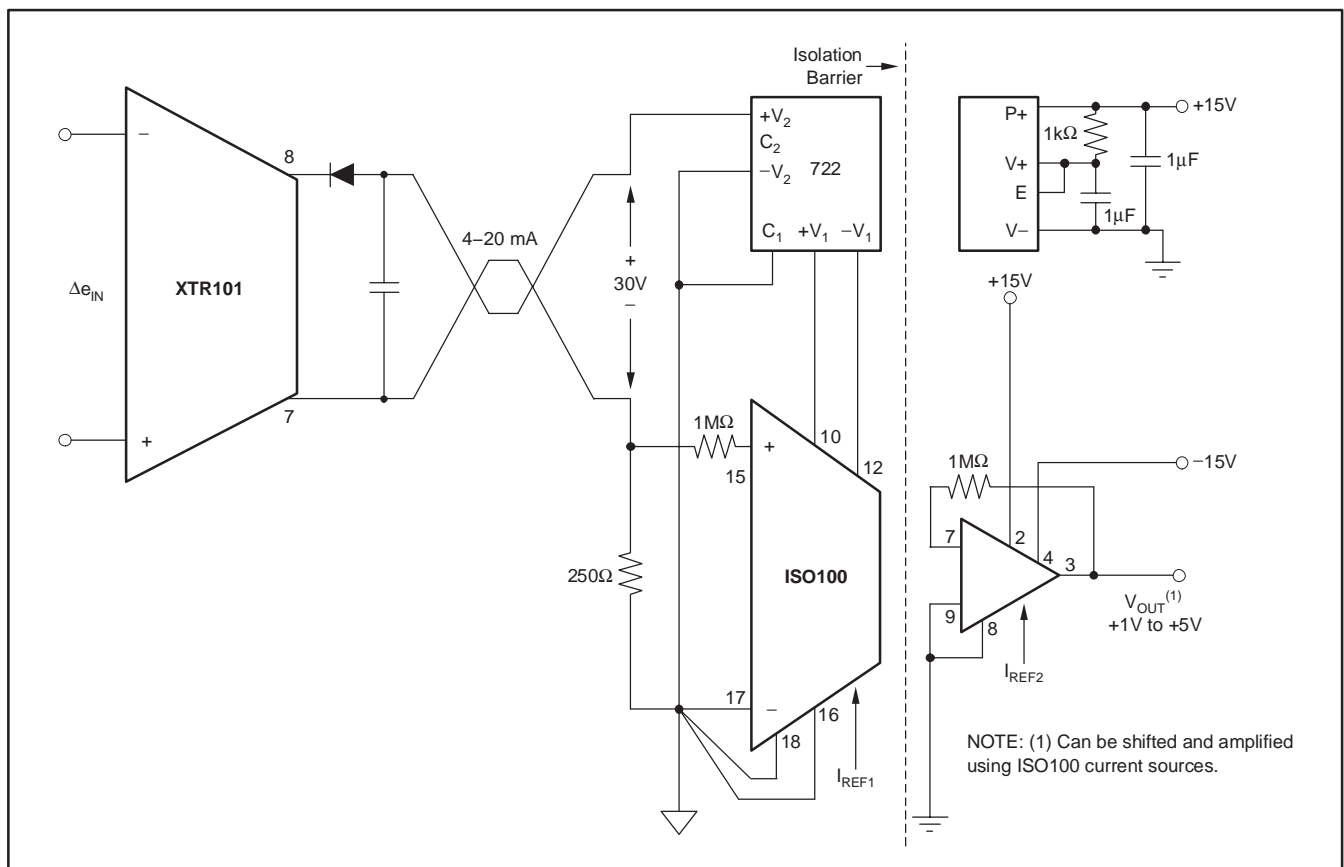


Figure 20. Isolated Two-Wire Current Loop

## DETAILED ERROR ANALYSIS

The ideal output current is:

$$I_{O\text{ IDEAL}} = 4\text{mA} + K e_{\text{IN}} \quad (3)$$

$$\text{where } K \text{ is the span (gain) term, } \left( 0.016 \frac{\text{amps}}{\text{volt}} + \left( \frac{40}{R_S} \right) \right)$$

In the XTR101 there are three major components of error:

1.  $\sigma_O$  = errors associated with the output stage.
2.  $\sigma_S$  = errors associated with span adjustment.
3.  $\sigma_I$  = errors associated with the input stage.

The transfer function including these errors is:

$$I_{O\text{ ACTUAL}} = (4\text{mA} + \sigma_O) + K(1 + \sigma_S)(e_{\text{IN}} + \sigma_I) \quad (4)$$

When this expression is expanded, second-order terms ( $\sigma_S, \sigma_I$ ) dropped, and terms collected, the result is:

$$I_{O\text{ ACTUAL}} = (4\text{mA} + \sigma_O) + K e_{\text{IN}} + K\sigma_I + K\sigma_S e_{\text{IN}} \quad (5)$$

The error in the output current is  $I_{O\text{ ACTUAL}} - I_{O\text{ IDEAL}}$  and can be found by subtracting Equation 3 from Equation 5.

$$I_{O\text{ ERROR}} = \sigma_O + K\sigma_I + K\sigma_S e_{\text{IN}} \quad (6)$$

This is a general error expression. The composition of each component of error depends on the circuitry inside the XTR101 and the particular circuit in which it is applied. The circuit of Figure 9 will be used to illustrate the principles.

$$\sigma_O = I_{OS\text{ RTO}} \quad (7)$$

$$\sigma_S = \epsilon_{\text{NONLINEARITY}} + \epsilon_{\text{SPAN}} \quad (8)$$

$$\sigma_I = V_{OSI} + (I_{B1} + R_4 - I_{B2} R_T) + \frac{\Delta V_{CC}}{\text{PSRR}} + \frac{\left( \frac{e_1 + e_2}{2} \right) - 5V}{\text{CMRR}} \quad (9)$$

The term in parentheses may be written in terms of offset current and resistor mismatches as  $I_{B1} \Delta R + I_{OS'} R_4$ .

$V_{OSI}^{(1)}$  = input offset voltage.

$I_{B1}^{(1)}, I_{B2}^{(1)}$  = input bias current.

$I_{OSI}^{(1)}$  = input offset current.

$I_{OS\text{ RTO}}^{(1)}$  = output offset current error.

$\Delta R = R_T - R_4$  = mismatch in resistor.

$\Delta V_{CC}$  = change supply voltage between pins 7 and 8 away from 24V nominal.

$\text{PSRR}^{(1)}$  = power-supply rejection ratio.

$\text{CMRR}^{(1)}$  = common-mode rejection ratio.

$\epsilon_{\text{NONLIN}}^{(1)}$  = span nonlinearity.

$\epsilon_{\text{SPAN}}^{(1)}$  = span equation error.

Untrimmed error = 5% max. May be trimmed to zero.

(1) These items can be found in the Electrical Characteristics.

## EXAMPLE 3

See the circuit in Figure 9 with the XTR101BG specifications and the following conditions:  $R_T = 109.4\Omega$  at  $25^\circ\text{C}$ ,  $R_T = 156.4\Omega$  at  $150^\circ\text{C}$ ,  $I_O = 4\text{mA}$  at  $25^\circ\text{C}$ ,  $I_O = 20\text{mA}$  at  $150^\circ\text{C}$ ,  $R_S = 123.3\Omega$ ,  $R_4 = 109\Omega$ ,  $R_L = 250\Omega$ ,  $R_{\text{LINE}} = 100\Omega$ ,  $V_{DI} = 0.6V$ , and  $V_{PS} = 24V \pm 0.5\%$ . Determine the % error at the upper and lower range values.

### A. AT THE LOWER RANGE VALUE ( $T = +25^\circ\text{C}$ )

$$\sigma_O = I_{OS\text{ RTO}} = \pm 6\mu\text{A}$$

$$\sigma_I = V_{OSI} + (I_{B1} \Delta R + I_{OSI} R_4) + \frac{\Delta V_{CC}}{\text{PSRR}} + \left[ \frac{\left( \frac{e_1 + e_2}{2} \right) - 5V}{\text{CMRR}} \right]$$

$$\Delta R = R_{T\ 25^\circ\text{C}} - R_4 = 109.4 - 109 \approx 0$$

$$\Delta V_{CC} = (24 \times 0.005) + 4\text{mA}(250\Omega + 100\Omega) + 0.6V \\ = 120\text{mV} + 1400\text{mV} + 600\text{mV} = 2120\text{mV}$$

$$e_1 = (2\text{mA} \times 2.5\text{k}\Omega) + (1\text{mA} \times 109\Omega) \\ = 5.109V$$

$$e_2 = (2\text{mA} \times 2.5\text{k}\Omega) + (1\text{mA} \times 109.4\Omega) \\ = 5.1094V$$

$$\frac{(e_1 + e_2)}{2} - 5V = 0.1092V$$

$$\text{PSRR} = 3.16 \times 10^5 \text{ for } 110\text{dB}$$

$$\text{CMRR} = 31.6 \times 10^3 \text{ for } 90\text{dB}$$

$$\sigma_I = 30\mu\text{V} + (150\text{nA} \times 0 + 20\text{nA} \times 109\Omega) + \\ \frac{2120\text{mV}}{3.16 \times 10^5} + \frac{0.1092V}{3.16 \times 10^3} \quad (10) \\ = 30\mu\text{V} + 2.18\mu\text{V} + 6.7\mu\text{V} + 3.46\mu\text{V} \\ = 42.34\mu\text{V}$$

$$\sigma_S = \epsilon_{\text{NONLIN}} + \epsilon_{\text{SPAN}} \\ = 0.0001 + 0 \text{ (assumes trim of } R_S)$$

$$I_{O\text{ ERROR}} = \sigma_O + K\sigma_I + K\sigma_S e_{\text{IN}}$$

$$K = 0.016 + \frac{40}{R_S} = 0.016 + \frac{40}{123.3\Omega} \\ = 0.340 \frac{\text{amps}}{\text{volts}}$$

$$e_{\text{IN}} = e_2 - V_4 = I_{\text{REF1}} R_{T\ 25^\circ\text{C}} - I_{\text{REF2}} R_4$$

Since  $R_{T\ 25^\circ\text{C}} = R_4$ :

$$e_{\text{IN}} = (I_{\text{REF1}} - I_{\text{REF2}}) R_4 = 0.4\mu\text{A} \times 109\Omega \\ = 43.6\mu\text{V}$$

Since the maximum mismatch of the current references is 0.04% of  $1\text{mA} = 0.4\mu\text{A}$ :

$$I_{O\text{ error}} = 6\mu\text{A} + (0.34\text{A/V} \times 42.34\mu\text{V}) + \\ (0.34\text{A/V} \times 0.0001 \times 43.6\mu\text{V}) \\ = 6\mu\text{A} + 14.40\mu\text{A} + 0.0015\mu\text{A} = 20.40\mu\text{A}$$

$$\% \text{ error} = \frac{20.40\mu\text{A}}{16\text{mA}} \times 100\%$$

0.13% of span at lower range value.



## B. AT THE UPPER RANGE VALUE (T = +150°C)

$$\Delta R = R_{T150^{\circ}\text{C}} - R_4 = 156.4 - 109.4 = 47\Omega$$

$$\Delta V_{\text{CC}} = (24 \times 0.005) + 20\text{mA}(250\Omega + 100\Omega) + 0.6\text{V} = 7720\text{mV}$$

$$e_1 = 5.109\text{V}$$

$$e_2 = (2\text{mA} \times 2.5\text{k}\Omega) + (1\text{mA} \times 156.4\Omega) = 5.156\text{V}$$

$$\frac{(e_1 - e_2)}{2} - 5\text{V} = 0.1325\text{V}$$

$$\sigma_O = 6\mu\text{A}$$

$$\begin{aligned} \sigma_1 &= 30\mu\text{V} + (150\text{nA} \times 47\Omega + 20\text{nA} \times 190\Omega) + \\ &\quad \frac{7720\text{mV}}{3.16 \times 10^5} + \frac{0.1325\text{V}}{3.16 \times 10^3} \\ &= 30\mu\text{V} + 9.23\mu\text{V} + 24\mu\text{V} + 4.19\mu\text{V} \\ &= 67.42\mu\text{V} \end{aligned}$$

$$\sigma_S = 0.0001$$

$$\begin{aligned} e_{\text{IN}} &= e'_2 - V_4 = I_{\text{REF1}} R_{T150^{\circ}\text{C}} - I_{\text{REF2}} R_4 \\ &= (1\text{mA} \times 156.4\Omega) - (1\text{mA} \times 109\Omega) \\ &= 47\text{mV} \end{aligned}$$

$$\begin{aligned} I_O \text{ error} &= \sigma_O + K \sigma_1 + K \sigma_S e_{\text{IN}} \\ &= 6\mu\text{A} + (0.34\text{A/V} \times 67.42\mu\text{V}) + \\ &\quad (0.34\text{A/V} \times 0.0001 \times 47000\mu\text{V}) \\ &= 6\mu\text{A} + 22.92\mu\text{A} + 1.60\mu\text{A} \\ &= 30.52\mu\text{A} \end{aligned} \tag{11}$$

$$\% \text{ error} = \frac{30.52\mu\text{A}}{16\text{mA}} \times 100\%$$

0.19% of span at upper range value.

## CONCLUSIONS

**Lower Range:** From Equation 10, it is observed that the predominant error term is the input offset voltage (30μV for the B grade). This is of little consequence in many applications.  $V_{\text{OS RTI}}$  can, however, be nulled using the plots shown in Figure 5 and Figure 6. The result is an error of 0.06% of span instead of 0.13% of span.

**Upper Range:** From Equation 11, the predominant errors are  $I_{\text{OS RTO}}$  (6μA),  $V_{\text{OS RTI}}$  (30μV), and  $I_B$  (150nA), max, B grade. Both  $I_{\text{OS}}$  and  $V_{\text{OS}}$  can be trimmed to zero; however, the result is an error of 0.09% of span instead of 0.19% of span.

## RECOMMENDED HANDLING PROCEDURES FOR INTEGRATED CIRCUITS

All semiconductor devices are vulnerable, in varying degrees, to damage from the discharge of electrostatic energy. Such damage can cause performance degradation or failure, either immediate or latent. As a general practice, we recommend the following handling procedures to reduce the risk of electrostatic damage:

1. Remove the static-generating materials (such as untreated plastic) from all areas that handle microcircuits.
2. Ground all operators, equipment, and work stations.
3. Transport and ship microcircuits, or products incorporating microcircuits, in static-free, shielded containers.
4. Connect together all leads of each device by means of a conductive material when the device is not connected into a circuit.
5. Control relative humidity to as high a value as practical (50% recommended).

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XTR101AG	NRND	CDIP SB	JD	14	1	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type		XTR101AG	
XTR101AP	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	XTR101AP	<a href="#">Samples</a>
XTR101AU	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	XTR101AU	<a href="#">Samples</a>
XTR101AU/1K	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	XTR101AU	<a href="#">Samples</a>
XTR101BG	NRND	CDIP SB	JD	14	1	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type	-40 to 85	XTR101BG	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XTR101AU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS

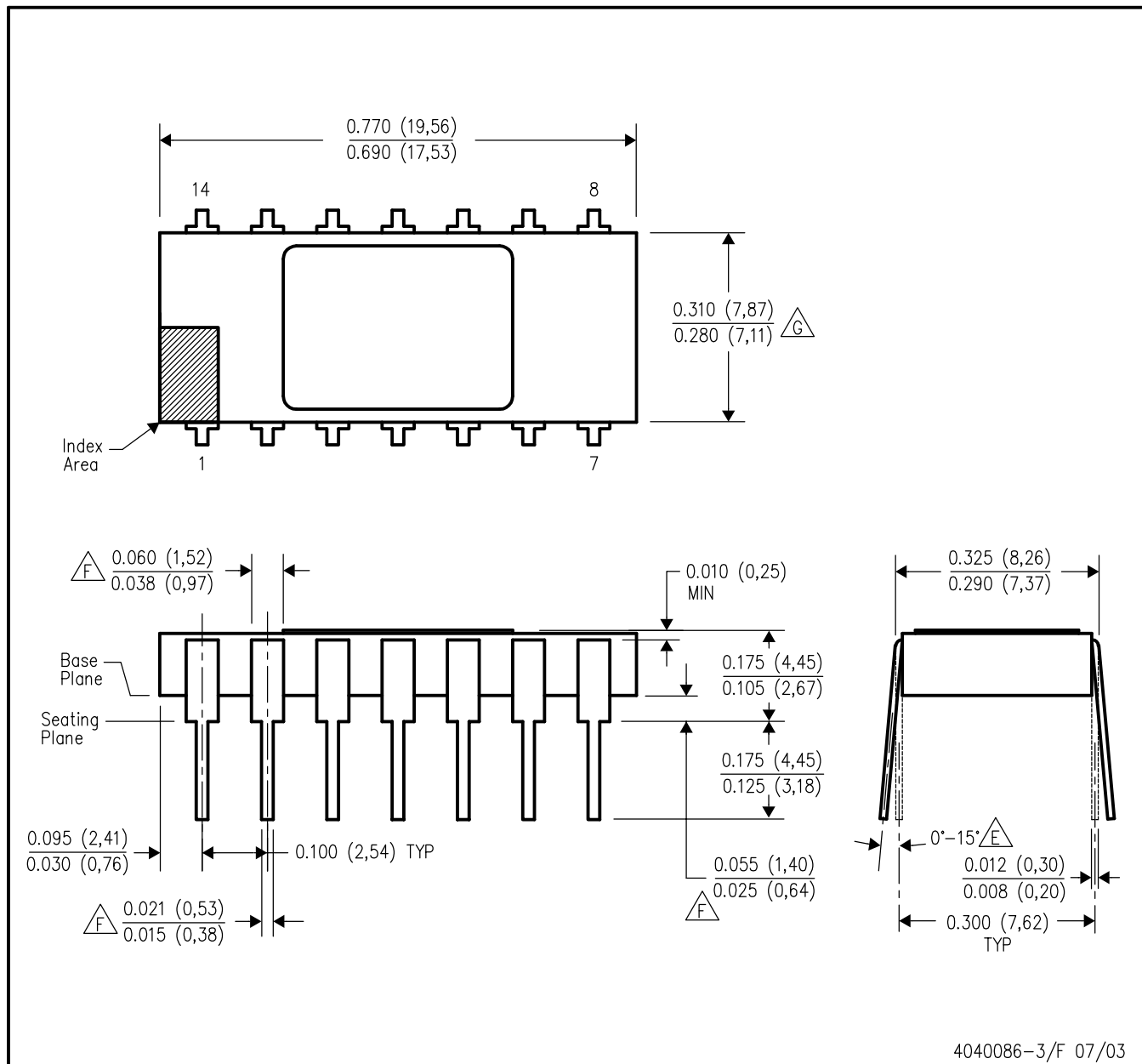


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XTR101AU/1K	SOIC	DW	16	1000	367.0	367.0	38.0

JD (R-CDIP-T14)

CERAMIC SIDE-BRAZE DUAL-IN-LINE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Controlling dimension: inch.
  - Leads within 0.005 (0,13) radius of true position (TP) at gage plane with maximum material condition and unit installed.
  - Angle applies to spread leads prior to installation.
  - Outlines on which the seating plane is coincident with the plane (standoff = 0), terminals lead standoffs are not required, and lead shoulder may equal lead width along any part of the lead above the seating/base plane.

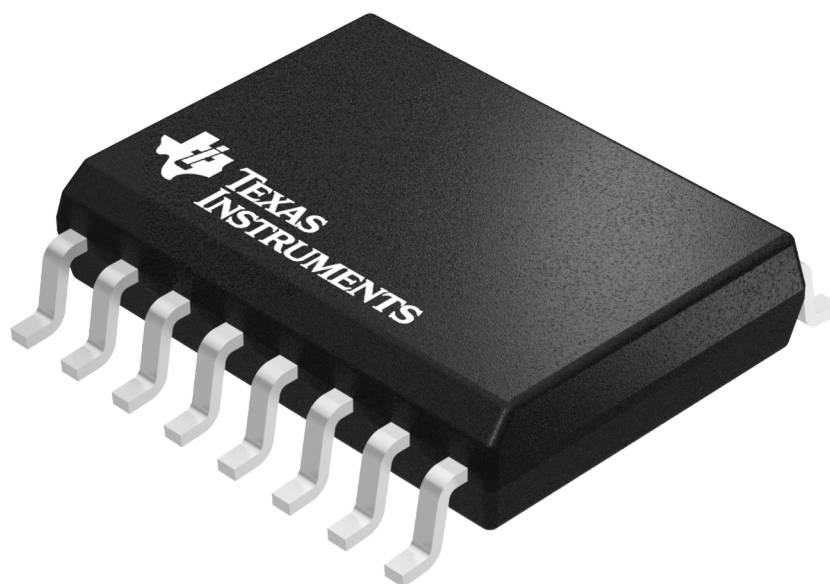
- Body width does not include particles of packing materials.
- A visual index feature must be located within the cross-hatched area.

**DW 16**

## GENERIC PACKAGE VIEW

**SOIC - 2.65 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040000-2/H



DW0016A

# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



# EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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