CD54/74AC138, CD54/74ACT138, CD74AC238, CD74ACT238

Data sheet acquired from Harris Semiconductor
SCHS234A

September 1998 - Revised May 2000

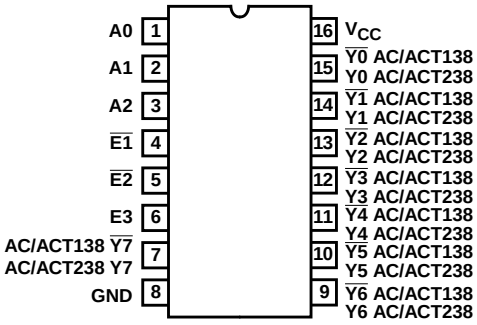
3-to-8-Line Decoders/Demultiplexers

Features

- **'AC138, 'ACT138. . . . . Inverting**
- **CD74AC238, CD74ACT238 . . . . . Non-Inverting**
- **Buffered Inputs**
- **Typical Propagation Delay**
  - **5ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF**
- **Exceeds 2kV ESD Protection MIL-STD-883, Method 3015**
- **SCR-Latchup-Resistant CMOS Process and Circuit Design**
- **Speed of Bipolar FAST™/AS/S with Significantly Reduced Power Consumption**
- **Balanced Propagation Delays**
- **AC Types Feature 1.5V to 5.5V Operation and Balanced Noise Immunity at 30% of the Supply**
- **±24mA Output Drive Current**
  - **Fanout to 15 FAST™ ICs**
  - **Drives 50Ω Transmission Lines**

Pinout

CD54AC138, CD54ACT138
(CERDIP)
CD74AC138, CD74ACT138, CD74AC238, CD74ACT238
(PDIP, SOIC)
TOP VIEW



Description

The 'AC138, 'ACT138, CD74AC238, and CD74ACT238 are 3-to-8-line decoders/demultiplexers that utilize Advanced CMOS Logic technology. Both circuits have three binary select inputs (A0, A1, and A2). If the device is enabled, these inputs determine which one of the eight normally HIGH outputs of the AC/ACT138 will go LOW or which on of the normally LOW outputs of the AC/ACT238 will go HIGH. Two active LOW and one active HIGH enables ($\overline{E1}$, $\overline{E2}$ and E3) are provided to simplify the cascading of these devices.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54AC138F3A	-55 to 125	16 Ld CERDIP
CD74AC138E	0 to 70°C, -40 to 85, -55 to 125	16 Ld PDIP
CD74AC138M	0 to 70°C, -40 to 85, -55 to 125	16 Ld SOIC
CD54ACT138F3A	-55 to 125	16 Ld CERDIP
CD74ACT138E	0 to 70°C, -40 to 85, -55 to 125	16 Ld PDIP
CD74ACT138M	0 to 70°C, -40 to 85, -55 to 125	16 Ld SOIC
CD74AC238E	0 to 70°C, -40 to 85, -55 to 125	16 Ld PDIP
CD74AC238M	0 to 70°C, -40 to 85, -55 to 125	16 Ld SOIC
CD74ACT238E	0 to 70°C, -40 to 85, -55 to 125	16 Ld PDIP
CD74ACT238M	0 to 70°C, -40 to 85, -55 to 125	16 Ld SOIC

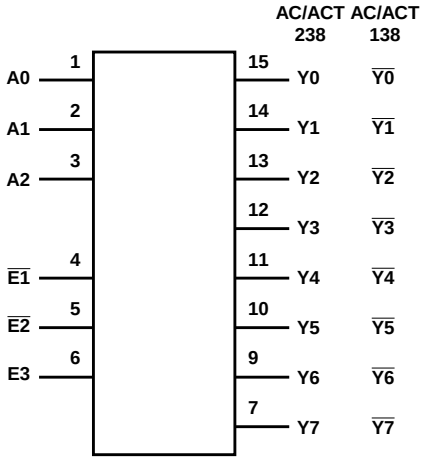
NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

FAST™ is a Trademark of Fairchild Semiconductor.

Functional Diagram



CD74AC/ACT138 TRUTH TABLE

INPUTS					OUTPUTS							
ENABLE		ADDRESS										
E_3	(NOTE 4) $\overline{E0}$	A_2	A_1	A_0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

CD74AC/ACT238 TRUTH TABLE

INPUTS					OUTPUTS							
ENABLE		ADDRESS										
E_3	(NOTE 4) $\overline{E0}$	A_2	A_1	A_0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	H	H	L	L	L	H	L	L	L	L
H	L	H	L	L	L	L	L	L	H	L	L	L
H	L	H	L	H	L	L	L	L	L	H	L	L
H	L	H	H	L	L	L	L	L	L	L	H	L
H	L	H	H	H	L	L	L	L	L	L	L	H

NOTES:

3. H = High Level, L = Low Level, X = Don't Care
4. $\overline{E0} = \overline{E1} + \overline{E2}$

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 6V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±50mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±50mA
DC V_{CC} or Ground Current, I_{CC} or I_{GND} (Note 5) . . . . . ±100mA

Operating Conditions

Temperature Range, T_A . . . . . -55°C to 125°C
Supply Voltage Range, V_{CC} (Note 6)
AC Types. . . . . 1.5V to 5.5V
ACT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Slew Rate, dt/dv
AC Types, 1.5V to 3V . . . . . 50ns (Max)
AC Types, 3.6V to 5.5V. . . . . 20ns (Max)
ACT Types, 4.5V to 5.5V. . . . . 10ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 7)	θ_{JA} (°C/W)
PDIP Package	90
SOIC Package	160

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

5. For up to 4 outputs per device, add ±25mA for each additional output.
6. Unless otherwise specified, all voltages are referenced to ground.
7. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
AC TYPES											
High Level Input Voltage	V_{IH}	-	-	1.5	1.2	-	1.2	-	1.2	-	V
				3	2.1	-	2.1	-	2.1	-	V
				5.5	3.85	-	3.85	-	3.85	-	V
Low Level Input Voltage	V_{IL}	-	-	1.5	-	0.3	-	0.3	-	0.3	V
				3	-	0.9	-	0.9	-	0.9	V
				5.5	-	1.65	-	1.65	-	1.65	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	-	1.4	-	1.4	-	V
			-0.05	3	2.9	-	2.9	-	2.9	-	V
			-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-4	3	2.58	-	2.48	-	2.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 8, 9)	5.5	-	-	3.85	-	-	-	V
			-50 (Note 8, 9)	5.5	-	-	-	-	3.85	-	V

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	0.05	1.5	-	0.1	-	0.1	-	0.1	V
			0.05	3	-	0.1	-	0.1	-	0.1	V
			0.05	4.5	-	0.1	-	0.1	-	0.1	V
			12	3	-	0.36	-	0.44	-	0.5	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 8, 9)	5.5	-	-	-	1.65	-	-	V
			50 (Note 8, 9)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I_I	V_{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	µA
Quiescent Supply Current MSI	I_{CC}	V_{CC} or GND	0	5.5	-	8	-	80	-	160	µA
ACT TYPES											
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 8, 9)	5.5	-	-	3.85	-	-	-	V
			-50 (Note 8, 9)	5.5	-	-	-	-	3.85	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	0.05	4.5	-	0.1	-	0.1	-	0.1	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 8, 9)	5.5	-	-	-	1.65	-	-	V
			50 (Note 8, 9)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I_I	V_{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	µA
Quiescent Supply Current MSI	I_{CC}	V_{CC} or GND	0	5.5	-	8	-	80	-	160	µA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI_{CC}	V_{CC} -2.1	-	4.5 to 5.5	-	2.4	-	2.8	-	3	mA

NOTES:

8. Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
9. Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

ACT Input Load Table

INPUT	UNIT LOAD
A0-A2	0.83
$\overline{E1}$, $\overline{E2}$	1
E3	0.42

NOTE: Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

Switching Specifications Input t_r, t_f = 3ns, C_L = 50pF (Worst Case)

PARAMETER	SYMBOL	V_{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
AC TYPES									
Propagation Delay, An to Output (CD54/74AC/ACT138)	t_{PLH}, t_{PHL}	1.5	-	-	125	-	-	138	ns
		3.3 (Note 11)	4	-	14	3.9	-	15.4	ns
		5 (Note 12)	2.8	-	10	2.8	-	11	ns
Propagation Delay, $\overline{E1}$, $\overline{E2}$ to Output (CD54/74AC/ACT138)	t_{PLH}, t_{PHL}	1.5	-	-	114	-	-	125	ns
		3.3	3.6	-	12.7	3.5	-	14	ns
		5	2.6	-	9.1	2.5	-	10	ns
Propagation Delay, E3 to Output (CD54/74AC/ACT138)	t_{PLH}, t_{PHL}	1.5	-	-	125	-	-	138	ns
		3.3	4	-	14	3.9	-	15.4	ns
		5	2.8	-	10	2.8	-	11	ns
Propagation Delay, An to Output (CD74AC/ACT238)	t_{PLH}, t_{PHL}	1.5	-	-	170	-	-	187	ns
		3.3	5.4	-	19.1	5.3	-	21	ns
		5	3.9	-	13.6	3.8	-	15	ns
Propagation Delay, $\overline{E1}$, $\overline{E2}$ to Output (CD74AC/ACT238)	t_{PLH}, t_{PHL}	1.5	-	-	135	-	-	149	ns
		3.3	4.3	-	15.2	4.2	-	16.7	ns
		5	3.1	-	10.7	3	-	11.9	ns
Propagation Delay, E3 to Output (CD74AC/ACT238)	t_{PLH}, t_{PHL}	1.5	-	-	189	-	-	208	ns
		3.3	6	-	21.1	5.8	-	23.2	ns
		5	4.3	-	15.1	4.2	-	16.6	ns
Input Capacitance	C_I	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C_{PD} (Note 13)	-	-	110	-	-	110	-	pF
ACT TYPES									
Propagation Delay, An to Output (CD54/74AC/ACT138)	t_{PLH}, t_{PHL}	5 (Note 12)	3.1	-	10.9	3	-	12	ns
Propagation Delay, $\overline{E1}$, $\overline{E2}$ to Output (CD54/74AC/ACT138)	t_{PLH}, t_{PHL}	5	2.7	-	9.5	2.6	-	10.5	ns
Propagation Delay, E3 to Output (CD54/74AC/ACT138)	t_{PLH}, t_{PHL}	5	2.8	-	10	2.8	-	11	ns
Propagation Delay, An to Output (CD74AC/ACT238)	t_{PLH}, t_{PHL}	5	4	-	14.2	3.9	-	15.6	ns
Propagation Delay, $\overline{E1}$, $\overline{E2}$ to Output (CD74AC/ACT238)	t_{PLH}, t_{PHL}	5	3.7	-	12.9	3.6	-	14.2	ns

Switching Specifications Input t_r, t_f = 3ns, C_L = 50pF (Worst Case) **(Continued)**

PARAMETER	SYMBOL	V_{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay, E3 to Output (CD74AC/ACT238)	t_{PLH}, t_{PHL}	5	3.5	-	12.4	3.4	-	13.6	ns
Input Capacitance	C_I	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C_{PD} (Note 13)	-	-	110	-	-	110	-	pF

NOTES:

10. Limits tested at 100%.
11. 3.3V Min at 3.6V, Max at 3V.
12. 5V Min at 5.5V, Max at 4.5V.
13. C_{PD} is used to determine the dynamic power consumption per package.
    AC: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
    ACT: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

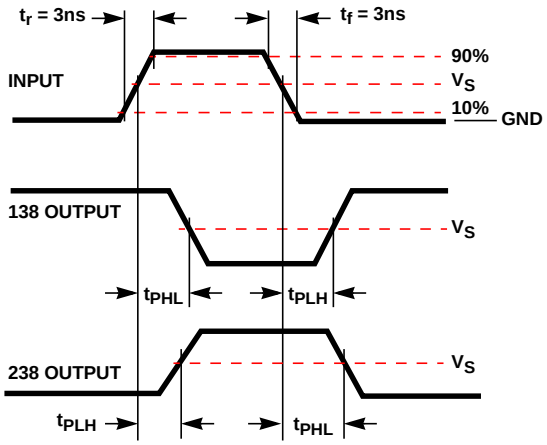


FIGURE 1. PROPAGATION DELAY TIMES

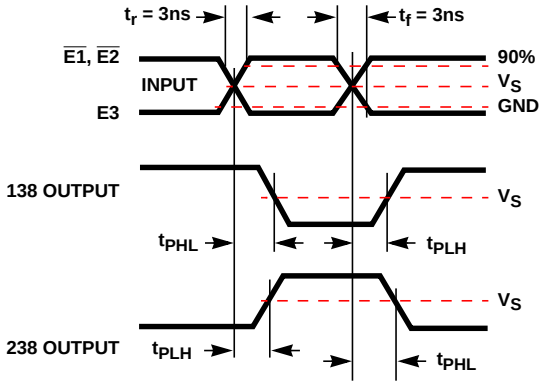
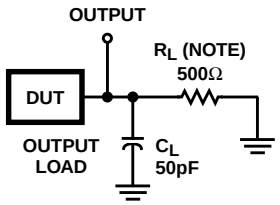


FIGURE 2. PROPAGATION DELAY TIMES



NOTE: For AC Series Only: When V_{CC} = 1.5V, R_L = 1kΩ.

	AC	ACT
Input Level	V_{CC}	3V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

FIGURE 3. PROPAGATION DELAY TIMES

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.