

SN54AHC244, SN74AHC244 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS226H – OCTOBER 1995 – REVISED JANUARY 2000

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Operating Range 2-V to 5.5-V V_{CC}**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs**

description

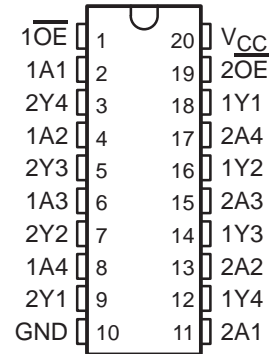
These octal buffers/drivers are designed specifically to improve the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The 'AHC244 devices are organized as two 4-bit buffers/line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

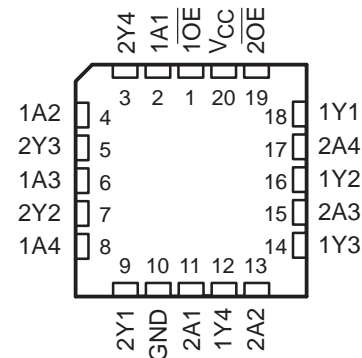
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54AHC244 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AHC244 is characterized for operation from -40°C to 85°C .

SN54AHC244 . . . J OR W PACKAGE
SN74AHC244 . . . DB, DGV, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC244 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each 4-bit buffer/driver)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

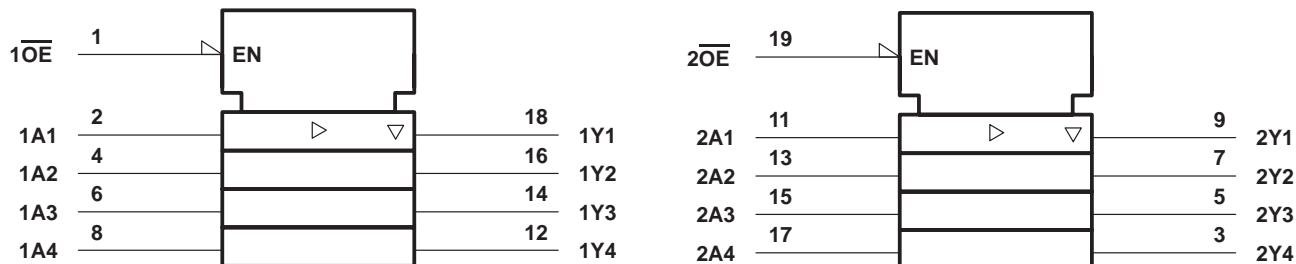
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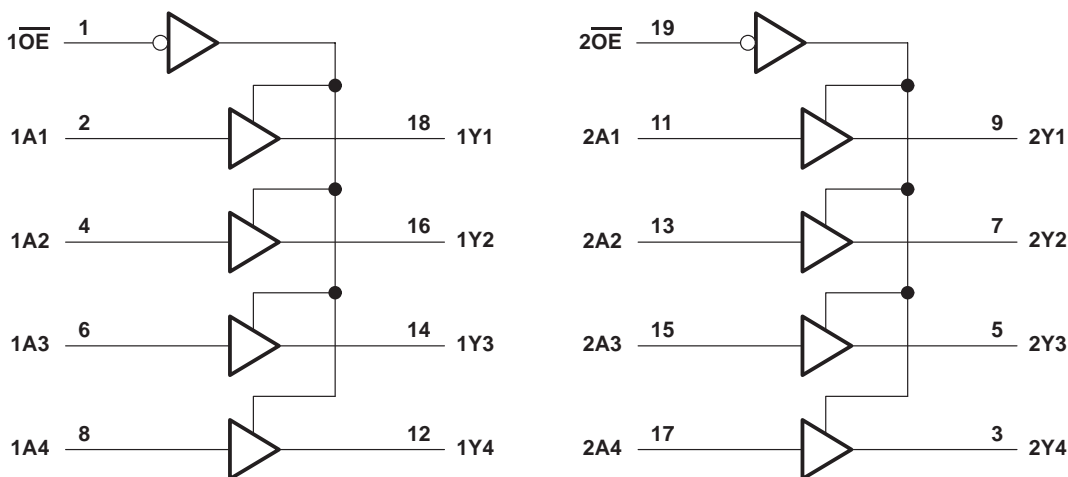
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DB package	70°C/W
DGV package	92°C/W
DW package	58°C/W
N package	69°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.



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recommended operating conditions (see Note 3)

		SN54AHC244		SN74AHC244		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V		1.5		V
		V _{CC} = 3 V		2.1		
		V _{CC} = 5.5 V		3.85		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		V
		V _{CC} = 3 V		0.9		
		V _{CC} = 5.5 V		1.65		
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		-50		μA
		V _{CC} = 3.3 V ± 0.3 V		-4		
		V _{CC} = 5 V ± 0.5 V		-8		
I _{OL}	Low-level output current	V _{CC} = 2 V		50		μA
		V _{CC} = 3.3 V ± 0.3 V		4		
		V _{CC} = 5 V ± 0.5 V		8		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V		100		ns/V
		V _{CC} = 5 V ± 0.5 V		20		
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC244		SN74AHC244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	2 V	1.9	2		1.9		1.9	V	
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	2 V				0.1		0.1	V	
		3 V				0.1		0.1		
		4.5 V				0.1		0.1		
	I _{OL} = 4 mA	3 V				0.36		0.44		
	I _{OL} = 8 mA	4.5 V				0.36		0.44		
I _I	V _I = V _{CC} or GND	0 V to 5.5 V				±0.1		±1*	μA	
I _{OZ}	V _O = V _{CC} or GND, V _I (OE) = V _{IL} or V _{IH}	5.5 V				±0.25		±2.5	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V				4		40	μA	
C _i	V _I = V _{CC} or GND	5 V		2	10			10	pF	
C _o	V _O = V _{CC} or GND	5 V		3.5					pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.



SN54AHC244, SN74AHC244 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC244		SN74AHC244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	5.8*	8.4*	1*	10*	1	10	ns	
t_{PHL}				5.8*	8.4*	1*	10*	1	10		
t_{PZH}	\overline{OE}	Y	$C_L = 15\text{ pF}$	6.6*	10.6*	1*	12.5*	1	12.5	ns	
t_{PZL}				6.6*	10.6*	1*	12.5*	1	12.5		
t_{PHZ}	\overline{OE}	Y	$C_L = 15\text{ pF}$	5*	9.7*	1*	11*	1	11	ns	
t_{PLZ}				5*	9.7*	1*	11*	1	11		
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	8.3	11.9	1	13.5	1	13.5	ns	
t_{PHL}				8.3	11.9	1	13.5	1	13.5		
t_{PZH}	\overline{OE}	Y	$C_L = 50\text{ pF}$	9.1	14.1	1	16	1	16	ns	
t_{PZL}				9.1	14.1	1	16	1	16		
t_{PHZ}	\overline{OE}	Y	$C_L = 50\text{ pF}$	10.3	14	1	16	1	16	ns	
t_{PLZ}				10.3	14	1	16	1	16		
$t_{sk(o)}$			$C_L = 50\text{ pF}$			1.5**			1.5	ns	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC244		SN74AHC244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	3.9*	5.5*	1*	6.5*	1	6.5	ns	
t_{PHL}				3.9*	5.5*	1*	6.5*	1	6.5		
t_{PZH}	\overline{OE}	Y	$C_L = 15\text{ pF}$	4.7*	7.3*	1*	8.5*	1	8.5	ns	
t_{PZL}				4.7*	7.3*	1*	8.5*	1	8.5		
t_{PHZ}	\overline{OE}	Y	$C_L = 15\text{ pF}$	5*	7.2*	1*	8.5*	1	8.5	ns	
t_{PLZ}				5*	7.2*	1*	8.5*	1	8.5		
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	5.4	7.5	1	8.5	1	8.5	ns	
t_{PHL}				5.4	7.5	1	8.5	1	8.5		
t_{PZH}	\overline{OE}	Y	$C_L = 50\text{ pF}$	6.2	9.3	1	10.5	1	10.5	ns	
t_{PZL}				6.2	9.3	1	10.5	1	10.5		
t_{PHZ}	\overline{OE}	Y	$C_L = 50\text{ pF}$	6.7	9.2	1	10.5	1	10.5	ns	
t_{PLZ}				6.7	9.2	1	10.5	1	10.5		
$t_{sk(o)}$			$C_L = 50\text{ pF}$			1**			1	ns	

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noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER	SN74AHC244			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}		0.5		V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}		-0.2		V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}		4.8		V
$V_{IH(D)}$ High-level dynamic input voltage	3.5			V
$V_{IL(D)}$ Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are for surface-mount packages only.

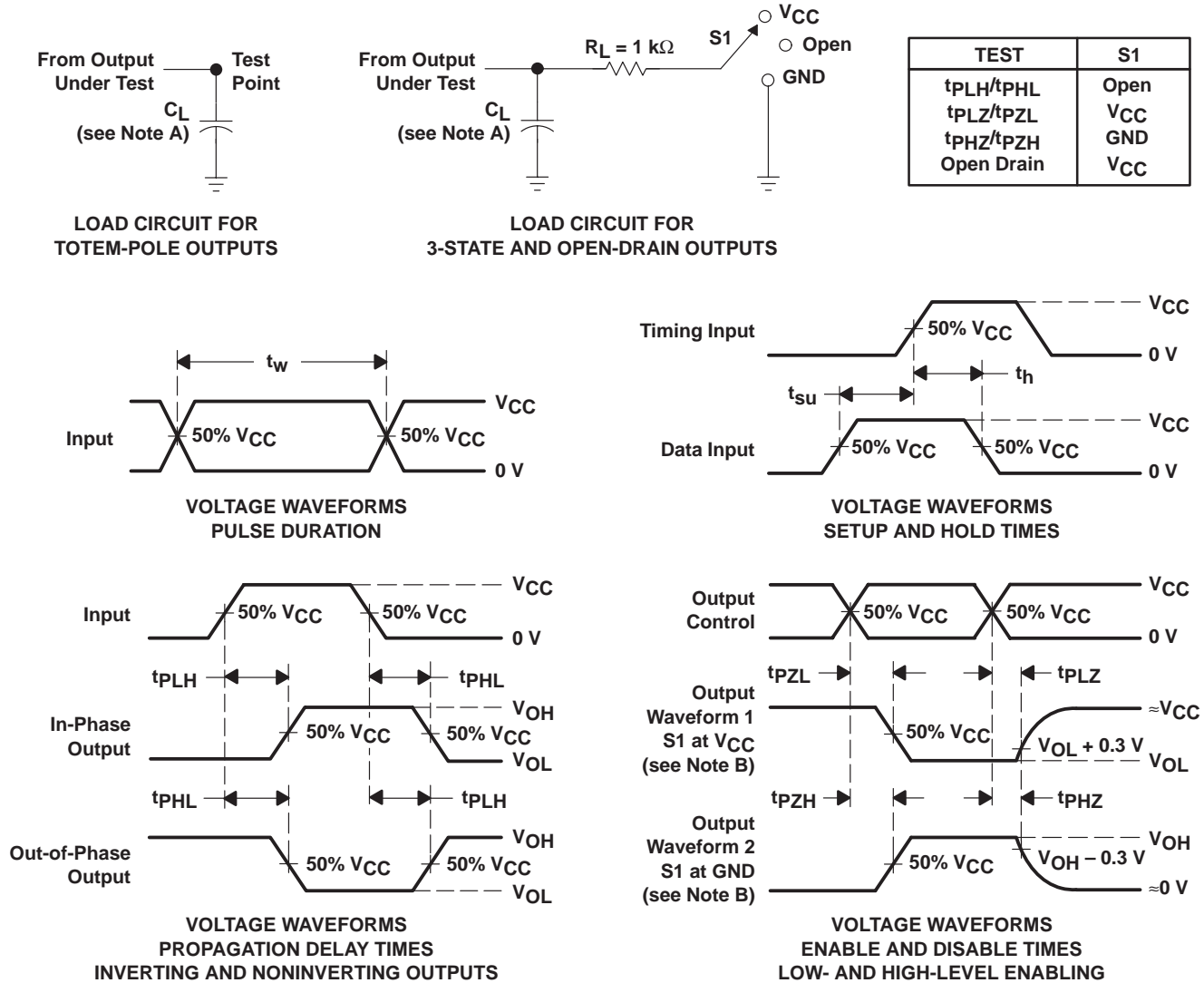
operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	8.6	pF

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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