

## WIDEBAND, LOW-NOISE, LOW DISTORTION, FULLY DIFFERENTIAL AMPLIFIER

### FEATURES

- Fully Differential Architecture
- Centered Input Common-Mode Range
- Output Common-Mode Control
- Minimum Gain of 2 V/V (6 dB)
- Bandwidth: 1900 MHz
- Slew Rate: 6600 V/ $\mu$ s
- 1% Settling Time: 2 ns
- HD<sub>2</sub>: –75 dBc at 100 MHz
- HD<sub>3</sub>: –80 dBc at 100 MHz
- OIP<sub>3</sub>: 37 dBm at 70 MHz
- Input Voltage Noise: 1.9 nV/ $\sqrt{\text{Hz}}$  ( $f > 10$  MHz)
- Power-Supply Voltage: 3 V to 5 V
- Power-Supply Current: 37.7 mA
- Power-Down Current: 0.65 mA

### APPLICATIONS

- 5-V Data Acquisition Systems High Linearity ADC Amplifier
- Wireless Communication
- Medical Imaging
- Test and Measurement

### RELATED PRODUCTS

Device	Min. Gain	Common-Mode Range of Input <sup>(1)</sup>
THS4508	6 dB	–0.3 V to 2.3 V
THS4509	6 dB	1.1 V to 3.9 V
THS4511	0 dB	–0.3 V to 2.3 V
THS4513	0 dB	1.1 V to 3.9 V

1. Assumes a 5-V single-ended power supply.

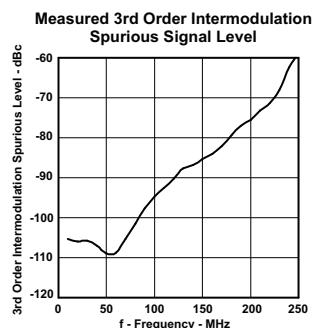
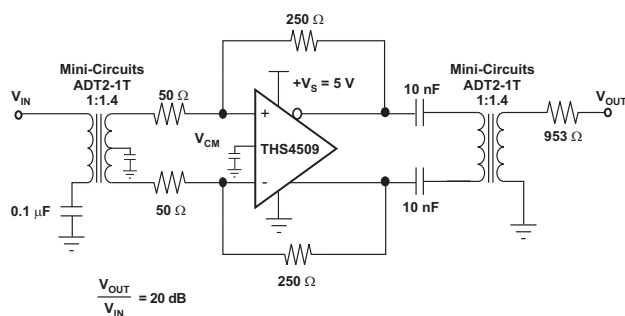
### DESCRIPTION

The THS4509 is a wideband, fully differential op amp designed for 5-V data acquisition systems. It has a low noise at 1.9 nV/ $\sqrt{\text{Hz}}$ , and low harmonic distortion of –75 dBc HD<sub>2</sub> and –80 dBc HD<sub>3</sub> at 100 MHz with 2 V<sub>PP</sub>, G = 10 dB, and 1 k $\Omega$  load. Slew rate is high at 6600 V/ $\mu$ s, and with settling time of 2 ns to 1% (2 V step), it is ideal for pulsed applications. It is designed for a minimum gain of 6 dB, but is optimized for gains of 10 dB.

To allow for dc coupling to ADCs, its unique output common-mode control circuit maintains the output common-mode voltage within 3 mV offset (typ) from the set voltage, when set within 0.5 V of mid-supply, with less than 4 mV differential offset voltage. The common-mode set point is set to mid-supply by internal circuitry, which may be over-driven from an external source.

The input and output are optimized for best performance with their common-mode voltages set to mid-supply. Along with high performance at low power-supply voltage, this design makes it ideal for high-performance, single-supply 5-V data acquisition systems. The combined performance of the THS4509 in a gain of 10 dB driving the ADS5500 ADC, sampling at 125 MSPS, is 81 dBc SFDR and 69.1 dBc SNR with a –1 dBFS signal at 70 MHz.

The THS4509 is offered in a quad, leadless QFN-16 package (RGT), and is characterized for operation over the full industrial temperature range from –40°C to +85°C.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**PACKAGING/ORDERING INFORMATION<sup>(1)</sup>**

TEMPERATURE	PACKAGED DEVICES	
	QUAD QFN <sup>(2)</sup> <sup>(3)</sup> (RGT-16)	SYMBOL
–40°C to +85°C	THS4509RGTT	—
	THS4509RGTR	

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) This package is available taped and reeled. The R suffix standard quantity is 3000. The T suffix standard quantity is 250.
- (3) The exposed thermal pad is electrically isolated from all other pins.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Over operating free-air temperature range, unless otherwise noted.

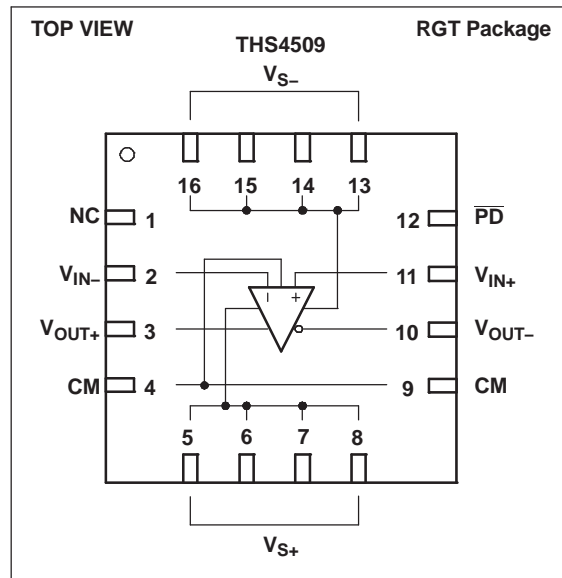
		UNIT
V <sub>S-</sub> to V <sub>S+</sub>	Supply voltage	6 V
V <sub>I</sub>	Input voltage	±V <sub>S</sub>
V <sub>ID</sub>	Differential input voltage	4 V
I <sub>O</sub>	Output current <sup>(2)</sup>	200 mA
	Continuous power dissipation	See <a href="#">Dissipation Rating Table</a>
T <sub>J</sub>	Maximum junction temperature	+150°C
T <sub>A</sub>	Operating free-air temperature range	–40°C to +85°C
T <sub>stg</sub>	Storage temperature range	–65°C to +150°C
ESD ratings	HBM	2000 V
	CDM	1500 V
	MM	100 V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) The THS4509 incorporates a (QFN) exposed thermal pad on the underside of the chip. This pad acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical briefs [SLMA002](#) and [SLMA004](#) for more information about using the QFN thermally-enhanced package.

**DISSIPATION RATINGS TABLE**

PACKAGE	θ <sub>JC</sub>	θ <sub>JA</sub>	POWER RATING	
			T <sub>A</sub> ≤ +25°C	T <sub>A</sub> = +85°C
RGT (16)	2.4°C/W	39.5°C/W	2.3 W	225 mW

## DEVICE INFORMATION



## TERMINAL FUNCTIONS

TERMINAL (RGT PACKAGE)		DESCRIPTION
NO.	NAME	
1	NC	No internal connection
2	$V_{IN-}$	Inverting amplifier input
3	$V_{OUT+}$	Noninverting amplifier output
4, 9	CM	Common-mode voltage input
5-8	$V_{S+}$	Positive amplifier power-supply input
10	$V_{OUT-}$	Inverted amplifier output
11	$V_{IN+}$	Noninverting amplifier input
12	$\overline{PD}$	Power-down: $\overline{PD}$ = logic low puts part into low power mode, $\overline{PD}$ = logic high or open for normal operation
13-16	$V_{S-}$	Negative amplifier power-supply input

**ELECTRICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 5\text{ V}$**

Test conditions are at  $V_{S+} = +2.5\text{ V}$ ,  $V_{S-} = -2.5\text{ V}$ ,  $G = 10\text{ dB}$ ,  $CM = \text{open}$ ,  $V_O = 2\text{ V}_{PP}$ ,  $R_F = 349\ \Omega$ ,  $R_L = 200\ \Omega$  differential,  $T_A = +25^\circ\text{C}$ , single-ended input, differential output, and input and output referenced to mid-supply, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL <sup>(1)</sup>
<b>AC PERFORMANCE</b>						
Small-signal bandwidth	$G = 6\text{ dB}$ , $V_O = 100\text{ mV}_{PP}$		2.0		GHz	C
	$G = 10\text{ dB}$ , $V_O = 100\text{ mV}_{PP}$		1.9		GHz	
	$G = 14\text{ dB}$ , $V_O = 100\text{ mV}_{PP}$		600		MHz	
	$G = 20\text{ dB}$ , $V_O = 100\text{ mV}_{PP}$		275		MHz	
Gain-bandwidth product	$G = 20\text{ dB}$		3		GHz	
Bandwidth for 0.1-dB flatness	$G = 10\text{ dB}$ , $V_O = 2\text{ V}_{PP}$		300		MHz	
Large-signal bandwidth	$G = 10\text{ dB}$ , $V_O = 2\text{ V}_{PP}$		1.5		GHz	
Slew rate (differential)			6600		V/ $\mu\text{s}$	
Rise time	2-V Step		0.5		ns	
Fall time			0.5			
Settling time to 1%			2			
Settling time to 0.1%			10			
2nd-order harmonic distortion	$f = 10\text{ MHz}$		-104		dBc	
	$f = 50\text{ MHz}$		-80			
	$f = 100\text{ MHz}$		-68			
3rd-order harmonic distortion	$f = 10\text{ MHz}$		-108		dBc	
	$f = 50\text{ MHz}$		-92			
	$f = 100\text{ MHz}$		-81			
2nd-order intermodulation distortion	200 kHz Tone spacing, $R_L = 499\ \Omega$	$f_C = 70\text{ MHz}$	-78		dBc	
3rd-order intermodulation distortion		$f_C = 140\text{ MHz}$	-64			
		$f_C = 70\text{ MHz}$	-95			
		$f_C = 140\text{ MHz}$	-78			
2nd-order output intercept point	200 kHz Tone spacing $R_L = 100\ \Omega$ , referenced to 50 $\Omega$ output	$f_C = 70\text{ MHz}$	78		dBm	
3rd-order output intercept point		$f_C = 140\text{ MHz}$	58			
		$f_C = 70\text{ MHz}$	43			
		$f_C = 140\text{ MHz}$	38			
1-dB compression point	$f_C = 70\text{ MHz}$		12.2		dBm	
	$f_C = 140\text{ MHz}$		10.8			
Noise figure	50 $\Omega$ System, 10 MHz		17.1		dB	
Input voltage noise	$f > 10\text{ MHz}$		1.9		nV/ $\sqrt{\text{Hz}}$	
Input current noise	$f > 10\text{ MHz}$		2.2		pA/ $\sqrt{\text{Hz}}$	
<b>DC PERFORMANCE</b>						
Open-loop voltage gain ( $A_{OL}$ )			68		dB	C
Input offset voltage	$T_A = +25^\circ\text{C}$		1	4	mV	A
	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		1	5	mV	
Average offset voltage drift	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		2.6		$\mu\text{V}/^\circ\text{C}$	B
Input bias current	$T_A = +25^\circ\text{C}$		8	15.5	$\mu\text{A}$	A
	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		8	18.5	$\mu\text{A}$	
Average bias current drift	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		20		nA/ $^\circ\text{C}$	B
Input offset current	$T_A = +25^\circ\text{C}$		1.6	3.6	$\mu\text{A}$	A
	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		1.6	7	$\mu\text{A}$	
Average offset current drift	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		4		nA/ $^\circ\text{C}$	B

(1) Test levels: (A) 100% tested at  $+25^\circ\text{C}$ . Over-temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

**ELECTRICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 5\text{ V}$  (continued)**

Test conditions are at  $V_{S+} = +2.5\text{ V}$ ,  $V_{S-} = -2.5\text{ V}$ ,  $G = 10\text{ dB}$ ,  $CM = \text{open}$ ,  $V_O = 2\text{ V}_{PP}$ ,  $R_F = 349\ \Omega$ ,  $R_L = 200\ \Omega$  differential,  $T_A = +25^\circ\text{C}$ , single-ended input, differential output, and input and output referenced to mid-supply, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL <sup>(1)</sup>	
<b>INPUT</b>							
Common-mode input range high			1.4		V	B	
Common-mode input range low			-1.4				
Common-mode rejection ratio			90		dB		
Differential input impedance			1.3    1.8		M $\Omega$    pF	C	
Common-mode input impedance			1.0    2.3		M $\Omega$    pF	C	
<b>OUTPUT</b>							
Maximum output voltage high	Each output with 100 $\Omega$ to mid-supply	$T_A = +25^\circ\text{C}$	1.2	1.4	V	A	
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	1.1	1.4			
Minimum output voltage low		$T_A = +25^\circ\text{C}$		-1.4	-1.2		V
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		-1.4	-1.1		
Differential output voltage swing		4.8	5.6		V		
	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	4.4					
Differential output current drive	$R_L = 10\ \Omega$		96		mA	C	
Output balance error	$V_O = 100\text{ mV}$ , $f = 1\text{ MHz}$		-49		dB		
Closed-loop output impedance	$f = 1\text{ MHz}$		0.3		$\Omega$		
<b>OUTPUT COMMON-MODE VOLTAGE CONTROL</b>							
Small-signal bandwidth			700		MHz	C	
Slew rate			110		V/ $\mu\text{s}$		
Gain			1		V/V		
Output common-mode offset from CM input	$1.25\text{ V} < CM < 3.5\text{ V}$		5		mV		
CM input bias current	$1.25\text{ V} < CM < 3.5\text{ V}$		$\pm 40$		$\mu\text{A}$		
CM input voltage range			-1.5 to 1.5		V		
CM input impedance			23    1		k $\Omega$    pF		
CM default voltage			0		V		
<b>POWER SUPPLY</b>							
Specified operating voltage		3	5	5.25	V	C	
Maximum quiescent current	$T_A = +25^\circ\text{C}$		37.7	40.9	mA	A	
	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		37.7	41.9			
Minimum quiescent current	$T_A = +25^\circ\text{C}$	34.5	37.7		mA		
	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	33.5	37.7				
Power-supply rejection ( $\pm\text{PSRR}$ )			90		dB	C	
<b>POWER-DOWN</b>							
Enable voltage threshold	Assured on above $2.1\text{ V} + V_{S-}$		$> 2.1 + V_{S-}$		V	C	
Disable voltage threshold	Assured off below $0.7\text{ V} + V_{S-}$		$< 0.7 + V_{S-}$		V		
Power-down quiescent current	$T_A = +25^\circ\text{C}$		0.65	0.9	mA	A	
	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		0.65	1			
Input bias current	$\overline{PD} = V_{S-}$		100		$\mu\text{A}$		
Input impedance			50    2		k $\Omega$    pF		
Turn-on time delay	Measured to output on		55		ns	C	
Turn-off time delay	Measured to output off		10		$\mu\text{s}$		

**ELECTRICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 3\text{ V}$**

Test conditions at  $V_{S+} = +1.5\text{ V}$ ,  $V_{S-} = -1.5\text{ V}$ ,  $G = 10\text{ dB}$ ,  $CM = \text{open}$ ,  $V_O = 1\text{ V}_{PP}$ ,  $R_F = 349\ \Omega$ ,  $R_L = 200\ \Omega$  differential,  $T_A = +25^\circ\text{C}$ , single-ended input, differential output, and input and output referenced to mid-supply, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL <sup>(1)</sup>
<b>AC PERFORMANCE</b>						
Small-signal bandwidth	$G = 6\text{ dB}$ , $V_O = 100\text{ mV}_{PP}$		1.9		GHz	C
	$G = 10\text{ dB}$ , $V_O = 100\text{ mV}_{PP}$		1.6		GHz	
	$G = 14\text{ dB}$ , $V_O = 100\text{ mV}_{PP}$		625		MHz	
	$G = 20\text{ dB}$ , $V_O = 100\text{ mV}_{PP}$		260		MHz	
Gain-bandwidth product	$G = 20\text{ dB}$		3		GHz	
Bandwidth for 0.1-dB flatness	$G = 10\text{ dB}$ , $V_O = 1\text{ V}_{PP}$		400		MHz	
Large-signal bandwidth	$G = 10\text{ dB}$ , $V_O = 1\text{ V}_{PP}$		1.5		GHz	
Slew rate (differential)	2-V Step		3500		V/ $\mu\text{s}$	
Rise time			0.25		ns	
Fall time			0.25			
Settling time to 1%			1			
Settling time to 0.1%			10			
2nd-order harmonic distortion	$f = 10\text{ MHz}$		-107		dBc	
	$f = 50\text{ MHz}$		-83			
	$f = 100\text{ MHz}$		-60			
3rd-order harmonic distortion	$f = 10\text{ MHz}$		-87		dBc	
	$f = 50\text{ MHz}$		-65			
	$f = 100\text{ MHz}$		-54			
2nd-order intermodulation distortion	200 kHz Tone spacing, $R_L = 499\ \Omega$	$f_C = 70\text{ MHz}$	-77		dBc	
3rd-order intermodulation distortion		$f_C = 140\text{ MHz}$	-54			
		$f_C = 70\text{ MHz}$	-77			
		$f_C = 140\text{ MHz}$	-62			
2nd-order output intercept point	200 kHz Tone spacing $R_L = 100\ \Omega$	$f_C = 70\text{ MHz}$	72		dBm	
3rd-order output intercept point		$f_C = 140\text{ MHz}$	52			
		$f_C = 70\text{ MHz}$	38.5			
		$f_C = 140\text{ MHz}$	30			
1-dB compression point	$f_C = 70\text{ MHz}$		2.2		dBm	
	$f_C = 140\text{ MHz}$		0.25			
Noise figure	50 $\Omega$ System, 10 MHz		17.1		dB	
Input voltage noise	$f > 10\text{ MHz}$		1.9		nV/ $\sqrt{\text{Hz}}$	
Input current noise	$f > 10\text{ MHz}$		2.2		pA/ $\sqrt{\text{Hz}}$	
<b>DC PERFORMANCE</b>						
Open-loop voltage gain ( $A_{OL}$ )			68		dB	C
Input offset voltage	$T_A = +25^\circ\text{C}$		1		mV	
Average offset voltage drift	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		2.6		$\mu\text{V}/^\circ\text{C}$	
Input bias current	$T_A = +25^\circ\text{C}$		6		$\mu\text{A}$	
Average bias current drift	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		20		nA/ $^\circ\text{C}$	
Input offset current	$T_A = +25^\circ\text{C}$		1.6		$\mu\text{A}$	
Average offset current drift	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		4		nA/ $^\circ\text{C}$	

(1) Test levels: (A) 100% tested at  $+25^\circ\text{C}$ . Over-temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

**ELECTRICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 3\text{ V}$  (continued)**

Test conditions at  $V_{S+} = +1.5\text{ V}$ ,  $V_{S-} = -1.5\text{ V}$ ,  $G = 10\text{ dB}$ ,  $CM = \text{open}$ ,  $V_O = 1\text{ V}_{PP}$ ,  $R_F = 349\ \Omega$ ,  $R_L = 200\ \Omega$  differential,  $T_A = +25^\circ\text{C}$ , single-ended input, differential output, and input and output referenced to mid-supply, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL <sup>(1)</sup>
<b>INPUT</b>						
Common-mode input range high			0.4		V	B
Common-mode input range low			-0.4			
Common-mode rejection ratio			80			
Differential input impedance			1.3    1.8		M $\Omega$    pF	C
Common-mode input impedance			1.0    2.3		M $\Omega$    pF	C
<b>OUTPUT</b>						
Maximum output voltage high	Each output with 100 $\Omega$ to mid-supply	$T_A = +25^\circ\text{C}$	0.45		V	C
Minimum output voltage low		$T_A = +25^\circ\text{C}$	-0.45		V	
Differential output voltage swing			1.8		V	
Differential output current drive	$R_L = 10\ \Omega$		50		mA	
Output balance error	$V_O = 100\text{ mV}$ , $f = 1\text{ MHz}$		-49		dB	
Closed-loop output impedance	$f = 1\text{ MHz}$		0.3		$\Omega$	
<b>OUTPUT COMMON-MODE VOLTAGE CONTROL</b>						
Small-signal bandwidth			570		MHz	C
Slew rate			60		V/ $\mu\text{s}$	
Gain			1		V/V	
Output common-mode offset from CM input	$1.25\text{ V} < CM < 3.5\text{ V}$		4		mV	
CM input bias current	$1.25\text{ V} < CM < 3.5\text{ V}$		$\pm 40$		$\mu\text{A}$	
CM input voltage range			-1.5 to 1.5		V	
CM input impedance			20    1		k $\Omega$    pF	
CM default voltage			0		V	
<b>POWER SUPPLY</b>						
Specified operating voltage			3		V	C
Quiescent current	$T_A = +25^\circ\text{C}$		34.8		mA	A
Power-supply rejection ( $\pm\text{PSRR}$ )			70		dB	C
<b>POWER-DOWN</b>						
	Referenced to $V_{S-}$					
Enable voltage threshold	Assured <i>on</i> above $2.1\text{ V} + V_{S-}$		$> 2.1 + V_{S-}$		V	C
Disable voltage threshold	Assured <i>off</i> below $0.7\text{ V} + V_{S-}$		$< 0.7 + V_{S-}$		V	
Power-down quiescent current			0.46		mA	
Input bias current	$\overline{PD} = V_{S-}$		65		$\mu\text{A}$	
Input impedance			50    2		k $\Omega$    pF	
Turn-on time delay	Measured to output on		100		ns	
Turn-off time delay	Measured to output off		10		$\mu\text{s}$	

**TYPICAL AC PERFORMANCE:  $V_{S+} - V_{S-} = 5\text{ V}$**

Test conditions at  $V_{S+} = +2.5\text{ V}$ ,  $V_{S-} = -2.5\text{ V}$ , CM = open,  $V_O = 2\text{ V}_{PP}$ ,  $R_F = 349\ \Omega$ ,  $R_L = 200\ \Omega$  differential, G = 10 dB, single-ended input, and input and output referenced to midrail, unless otherwise noted.

Small-Signal Frequency Response			<a href="#">Figure 1</a>
Large-Signal Frequency Response			<a href="#">Figure 2</a>
Harmonic Distortion	HD <sub>2</sub> , G = 6 dB, V <sub>OD</sub> = 2 V <sub>PP</sub>	vs Frequency	<a href="#">Figure 3</a>
	HD <sub>3</sub> , G = 6 dB, V <sub>OD</sub> = 2 V <sub>PP</sub>	vs Frequency	<a href="#">Figure 4</a>
	HD <sub>2</sub> , G = 10 dB, V <sub>OD</sub> = 2 V <sub>PP</sub>	vs Frequency	<a href="#">Figure 5</a>
	HD <sub>3</sub> , G = 10 dB, V <sub>OD</sub> = 2 V <sub>PP</sub>	vs Frequency	<a href="#">Figure 6</a>
	HD <sub>2</sub> , G = 14 dB, V <sub>OD</sub> = 2 V <sub>PP</sub>	vs Frequency	<a href="#">Figure 7</a>
	HD <sub>3</sub> , G = 14 dB, V <sub>OD</sub> = 2 V <sub>PP</sub>	vs Frequency	<a href="#">Figure 8</a>
	HD <sub>2</sub> , G = 10 dB	vs Output Voltage	<a href="#">Figure 9</a>
	HD <sub>3</sub> , G = 10 dB	vs Output Voltage	<a href="#">Figure 10</a>
	HD <sub>2</sub> , G = 10 dB	vs Common-Mode Input Voltage	<a href="#">Figure 11</a>
	HD <sub>3</sub> , G = 10 dB	vs Common-Mode Input Voltage	<a href="#">Figure 12</a>
Intermodulation Distortion	IMD <sub>2</sub> , G = 6 dB, V <sub>OD</sub> = 2 V <sub>PP</sub>	vs Frequency	<a href="#">Figure 13</a>
	IMD <sub>3</sub> , G = 6 dB, V <sub>OD</sub> = 2 V <sub>PP</sub>	vs Frequency	<a href="#">Figure 14</a>
	IMD <sub>2</sub> , G = 10 dB, V <sub>OD</sub> = 2 V <sub>PP</sub>	vs Frequency	<a href="#">Figure 15</a>
	IMD <sub>3</sub> , G = 10 dB, V <sub>OD</sub> = 2 V <sub>PP</sub>	vs Frequency	<a href="#">Figure 16</a>
	IMD <sub>2</sub> , G = 14 dB, V <sub>OD</sub> = 2 V <sub>PP</sub>	vs Frequency	<a href="#">Figure 17</a>
	IMD <sub>3</sub> , G = 14 dB, V <sub>OD</sub> = 2 V <sub>PP</sub>	vs Frequency	<a href="#">Figure 18</a>
Output Intercept Point	OIP <sub>2</sub>	vs Frequency	<a href="#">Figure 19</a>
	OIP <sub>3</sub>	vs Frequency	<a href="#">Figure 20</a>
0.1 dB Flatness			<a href="#">Figure 21</a>
S-Parameters		vs Frequency	<a href="#">Figure 22</a>
Transition Rate		vs Output Voltage	<a href="#">Figure 23</a>
Transient Response			<a href="#">Figure 24</a>
Settling Time			<a href="#">Figure 25</a>
Rejection Ratio		vs Frequency	<a href="#">Figure 26</a>
Output Impedance		vs Frequency	<a href="#">Figure 27</a>
Overdrive Recovery			<a href="#">Figure 28</a>
Output Voltage Swing		vs Load Resistance	<a href="#">Figure 29</a>
Turn-Off Time			<a href="#">Figure 30</a>
Turn-On Time			<a href="#">Figure 31</a>
Input Offset Voltage		vs Input Common-Mode Voltage	<a href="#">Figure 32</a>
Open-Loop Gain		vs Frequency	<a href="#">Figure 33</a>
Input Referred Noise		vs Frequency	<a href="#">Figure 34</a>
Noise Figure		vs Frequency	<a href="#">Figure 35</a>
Quiescent Current		vs Supply Voltage	<a href="#">Figure 36</a>
Power-Supply Current		vs Supply Voltage in Power-Down Mode	<a href="#">Figure 37</a>
Output Balance Error		vs Frequency	<a href="#">Figure 38</a>
CM Input Impedance		vs Frequency	<a href="#">Figure 39</a>
CM Small-Signal Frequency Response			<a href="#">Figure 40</a>
CM Input Bias Current		vs CM Input Voltage	<a href="#">Figure 41</a>
Differential Output Offset Voltage		vs CM Input Voltage	<a href="#">Figure 42</a>
Output Common-Mode Offset		vs CM Input Voltage	<a href="#">Figure 43</a>



**TYPICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 5\text{ V}$**

Test conditions at  $V_{S+} = +2.5\text{ V}$ ,  $V_{S-} = -2.5\text{ V}$ , CM = open,  $V_O = 2\text{ V}_{PP}$ ,  $R_F = 349\ \Omega$ ,  $R_L = 200\ \Omega$  differential,  $G = 10\text{ dB}$ , single-ended input, and input and output referenced to midrail, unless otherwise noted.

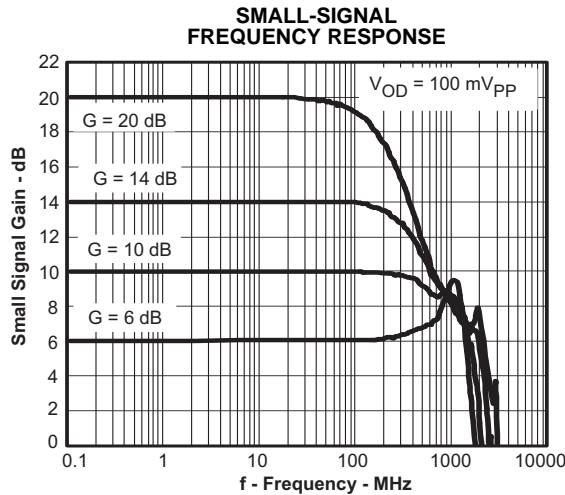


Figure 1.

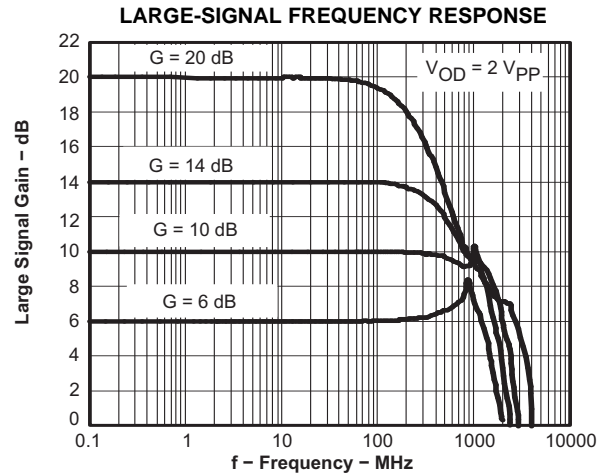


Figure 2.

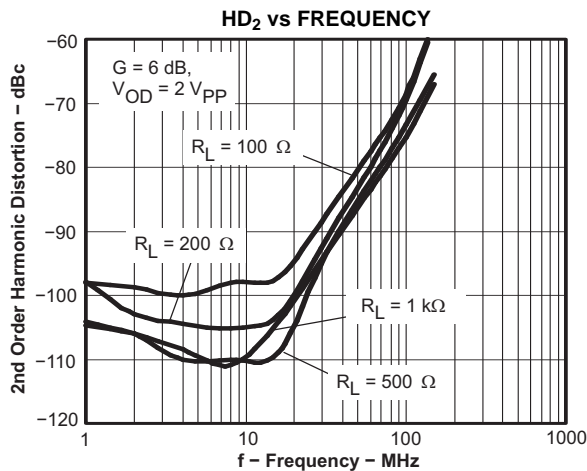


Figure 3.

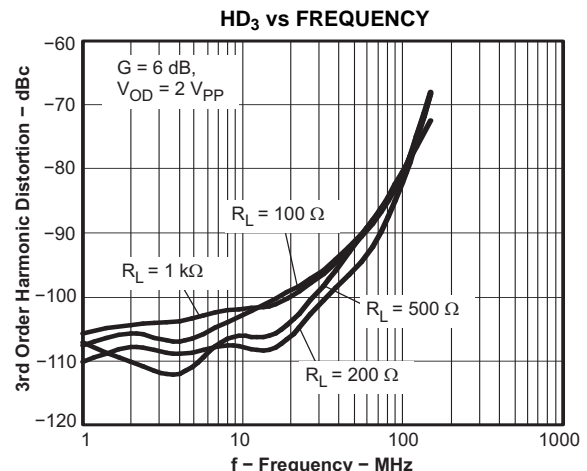


Figure 4.

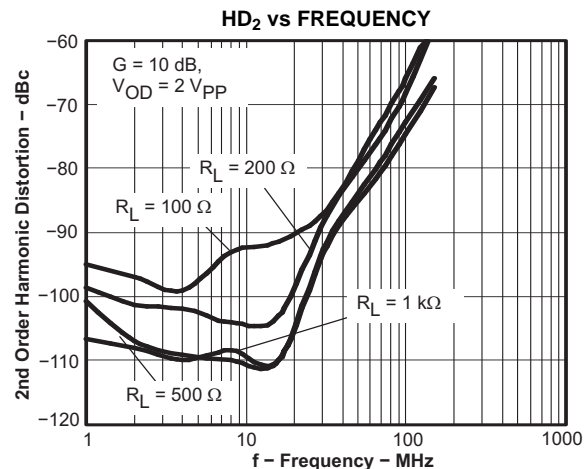


Figure 5.

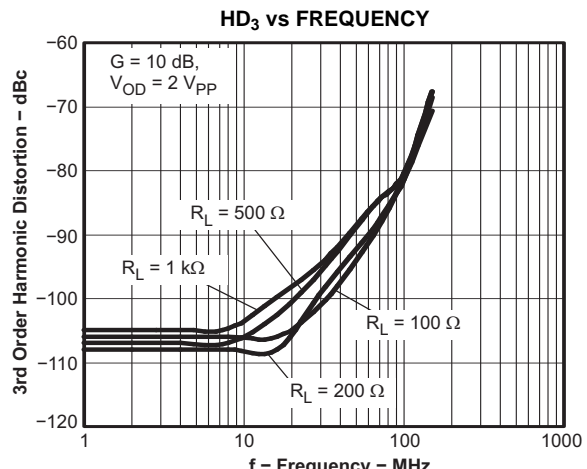


Figure 6.

**TYPICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 5\text{ V}$  (continued)**

Test conditions at  $V_{S+} = +2.5\text{ V}$ ,  $V_{S-} = -2.5\text{ V}$ , CM = open,  $V_{O} = 2\text{ V}_{PP}$ ,  $R_F = 349\ \Omega$ ,  $R_L = 200\ \Omega$  differential,  $G = 10\text{ dB}$ , single-ended input, and input and output referenced to midrail, unless otherwise noted.

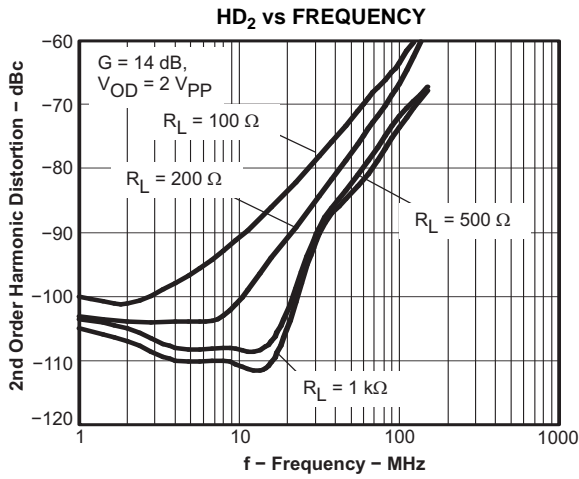


Figure 7.

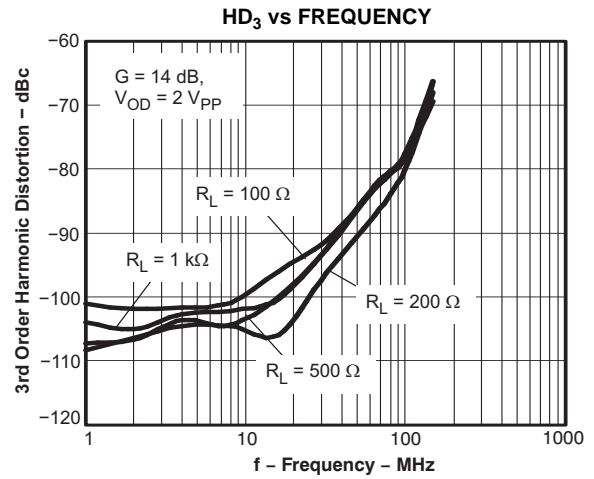


Figure 8.

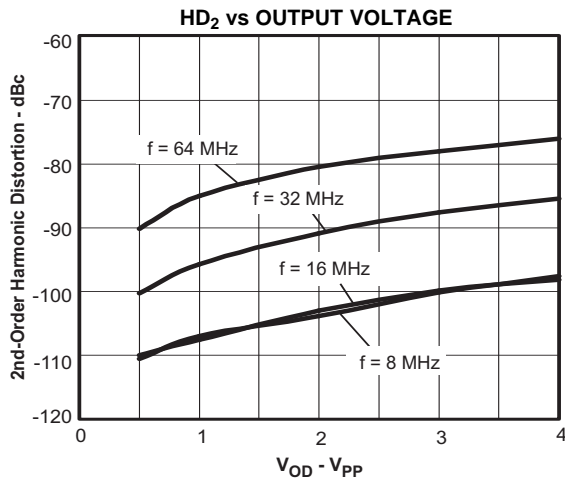


Figure 9.

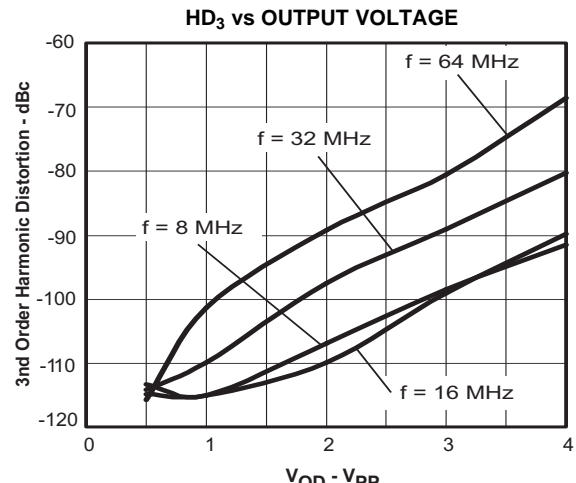


Figure 10.

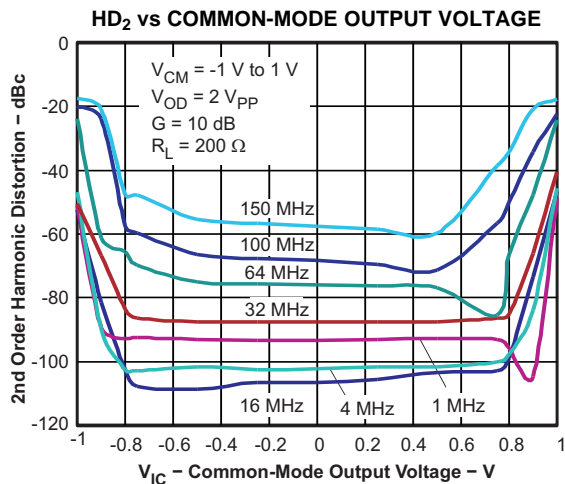


Figure 11.

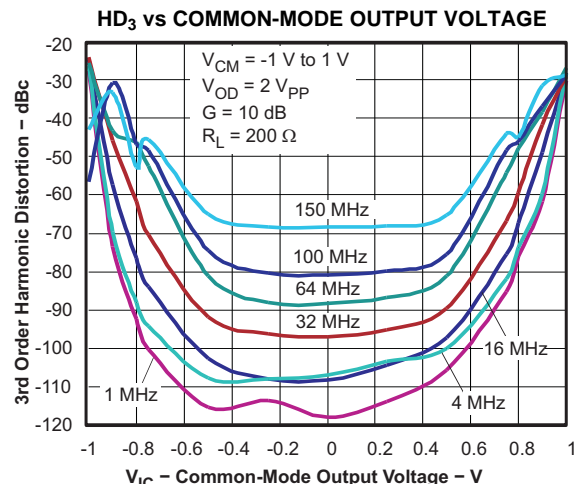


Figure 12.

**TYPICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 5\text{ V}$  (continued)**

Test conditions at  $V_{S+} = +2.5\text{ V}$ ,  $V_{S-} = -2.5\text{ V}$ , CM = open,  $V_{O} = 2\text{ V}_{PP}$ ,  $R_F = 349\ \Omega$ ,  $R_L = 200\ \Omega$  differential, G = 10 dB, single-ended input, and input and output referenced to midrail, unless otherwise noted.

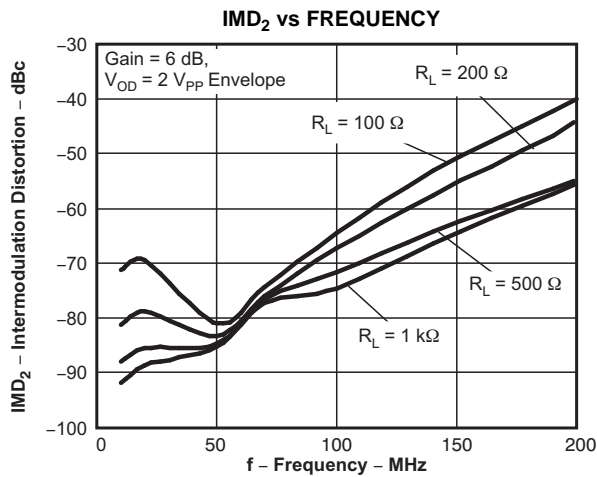


Figure 13.

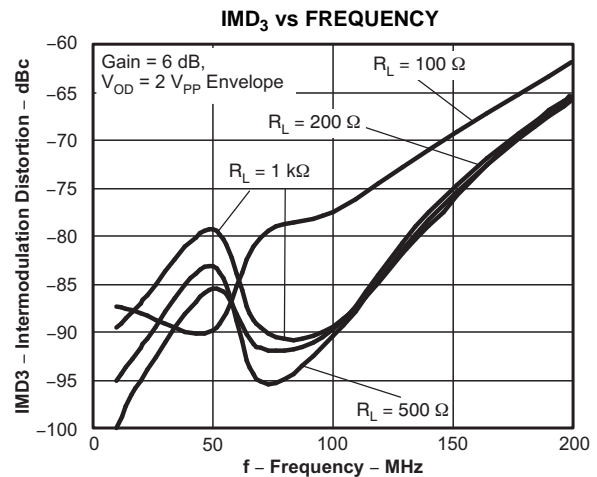


Figure 14.

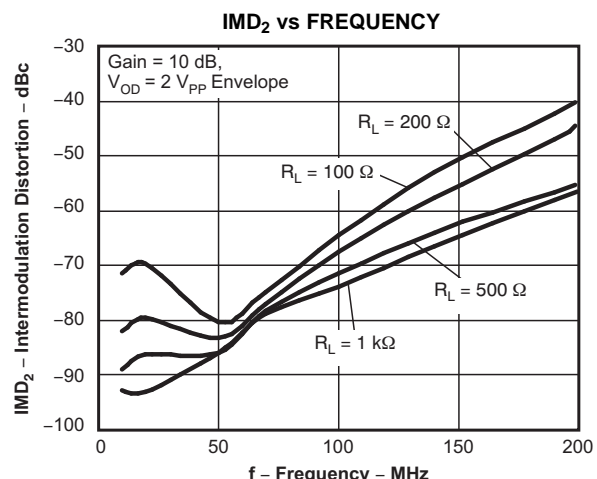


Figure 15.

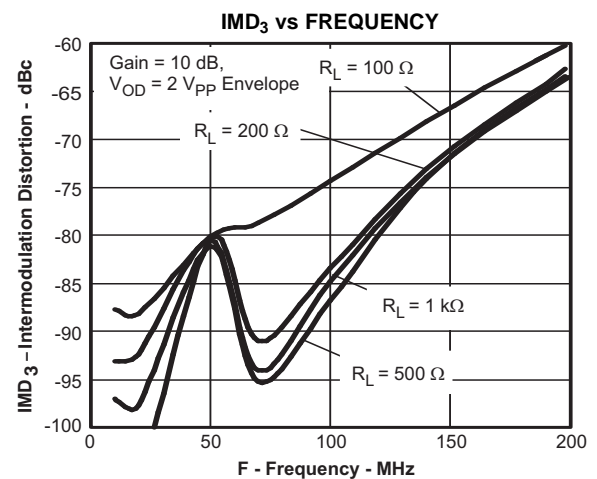


Figure 16.

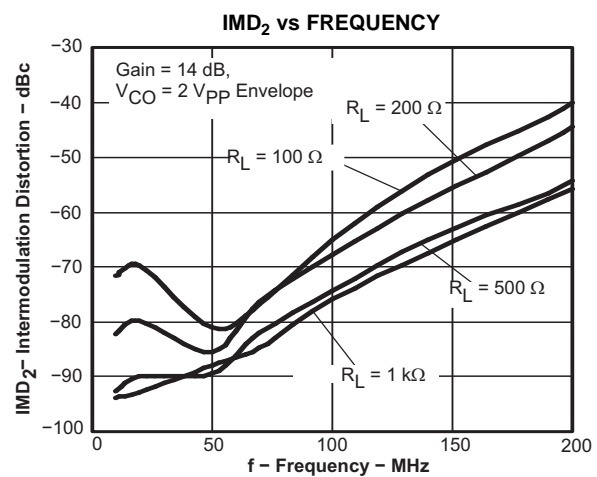


Figure 17.

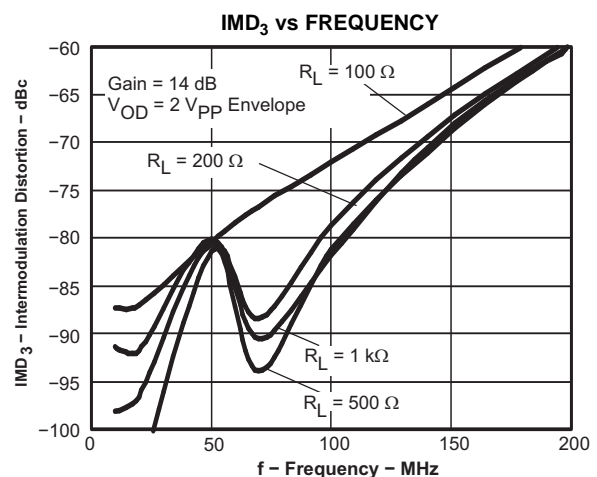


Figure 18.

**TYPICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 5\text{ V}$  (continued)**

Test conditions at  $V_{S+} = +2.5\text{ V}$ ,  $V_{S-} = -2.5\text{ V}$ , CM = open,  $V_O = 2\text{ V}_{PP}$ ,  $R_F = 349\ \Omega$ ,  $R_L = 200\ \Omega$  differential, G = 10 dB, single-ended input, and input and output referenced to midrail, unless otherwise noted.

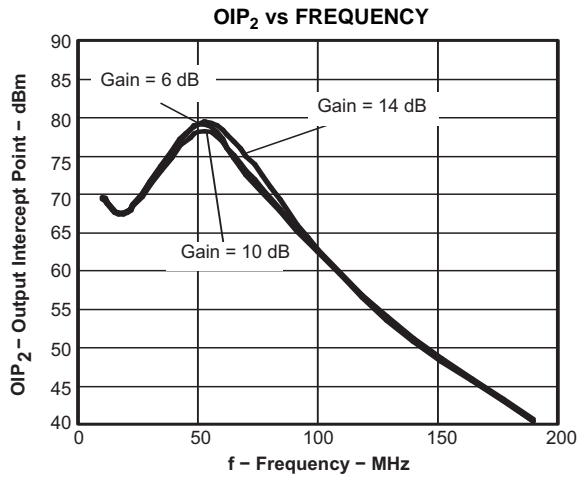


Figure 19.

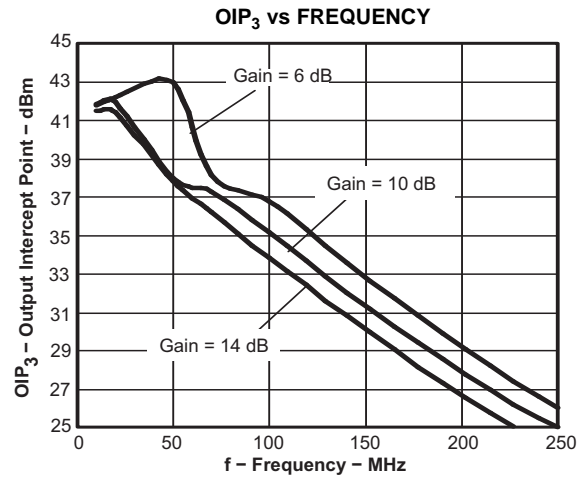


Figure 20.

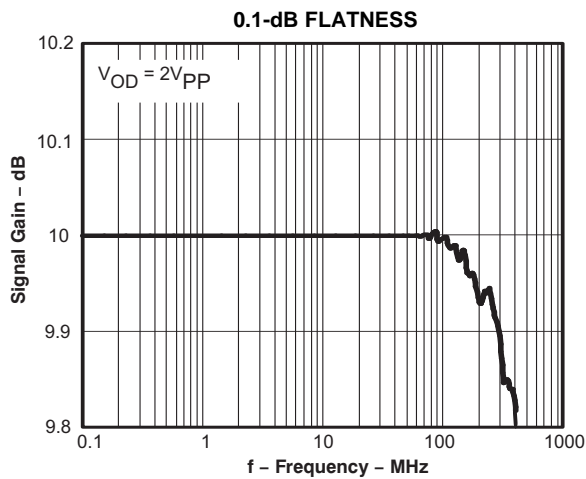


Figure 21.

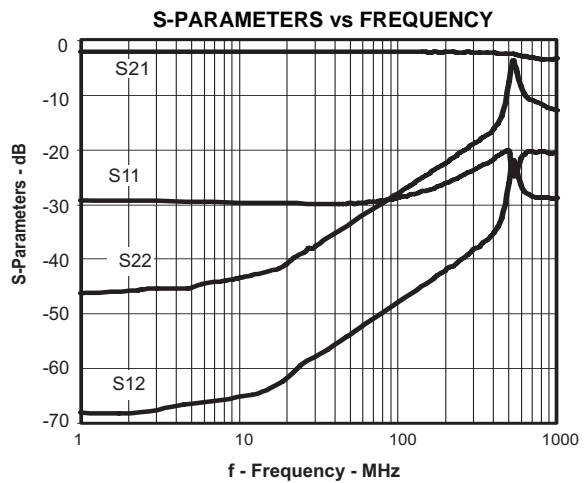


Figure 22.

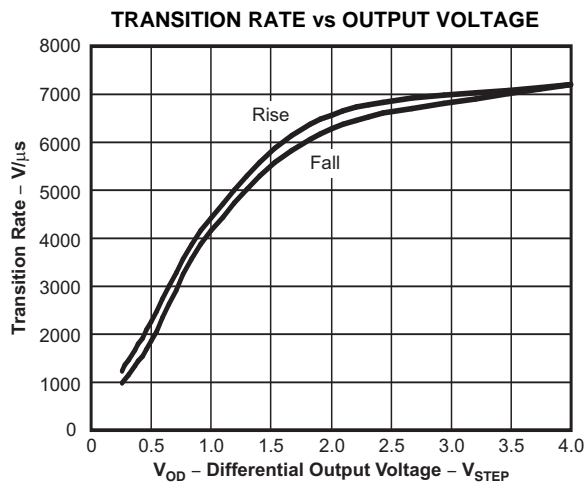


Figure 23.

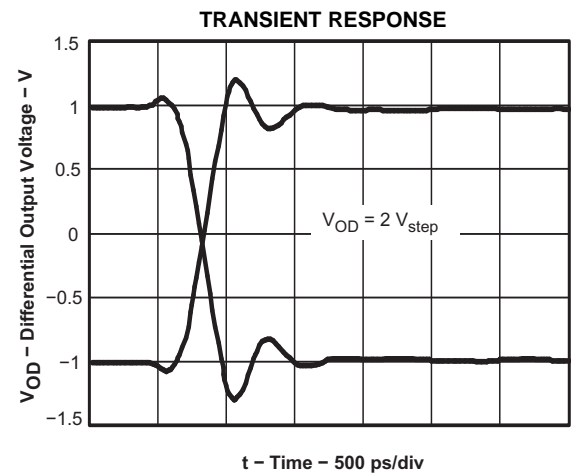


Figure 24.

**TYPICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 5\text{ V}$  (continued)**

Test conditions at  $V_{S+} = +2.5\text{ V}$ ,  $V_{S-} = -2.5\text{ V}$ , CM = open,  $V_O = 2\text{ V}_{PP}$ ,  $R_F = 349\ \Omega$ ,  $R_L = 200\ \Omega$  differential, G = 10 dB, single-ended input, and input and output referenced to midrail, unless otherwise noted.

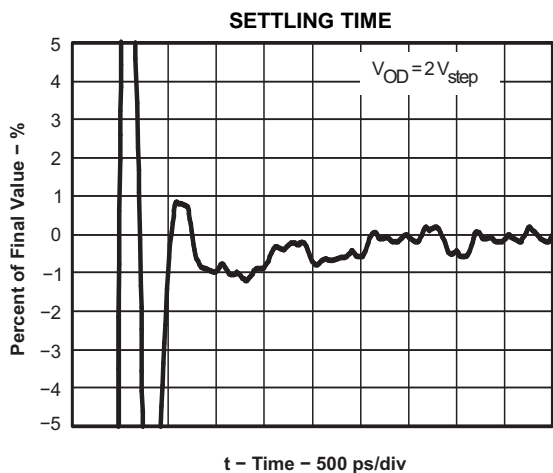


Figure 25.

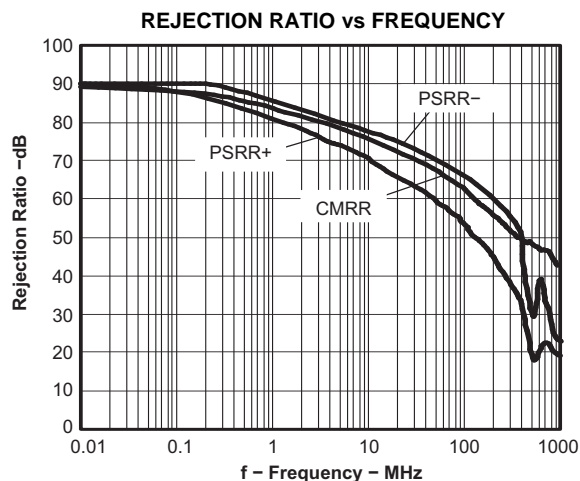


Figure 26.

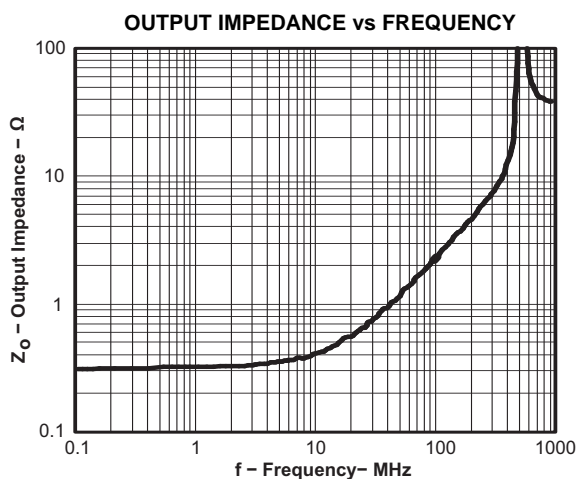


Figure 27.

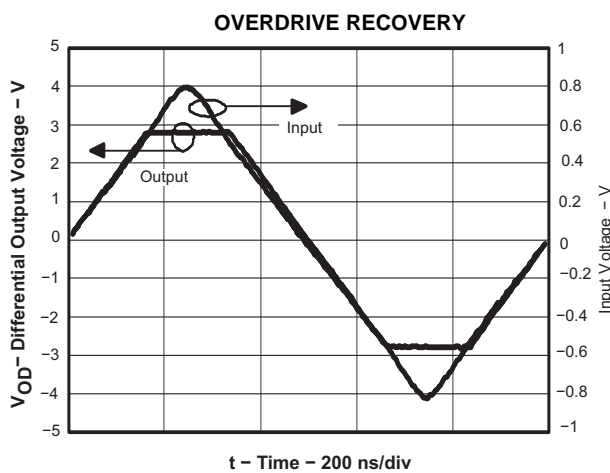


Figure 28.

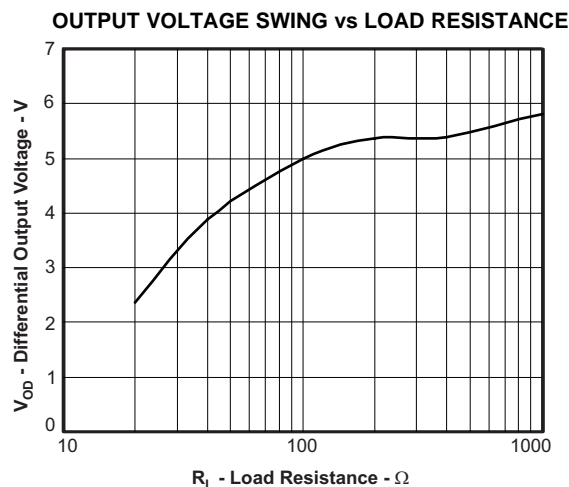


Figure 29.

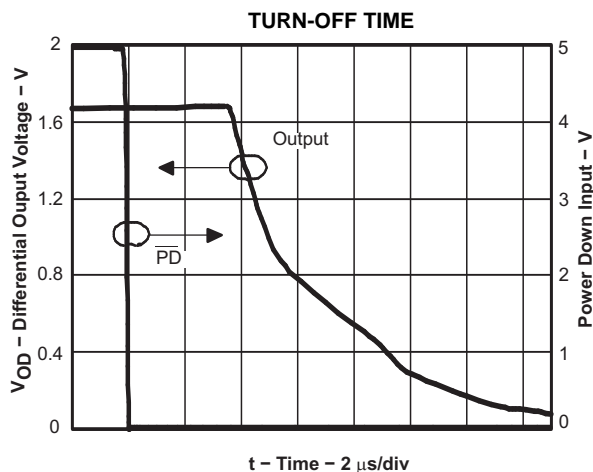


Figure 30.

**TYPICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 5\text{ V}$  (continued)**

Test conditions at  $V_{S+} = +2.5\text{ V}$ ,  $V_{S-} = -2.5\text{ V}$ , CM = open,  $V_O = 2\text{ V}_{PP}$ ,  $R_F = 349\ \Omega$ ,  $R_L = 200\ \Omega$  differential,  $G = 10\text{ dB}$ , single-ended input, and input and output referenced to midrail, unless otherwise noted.

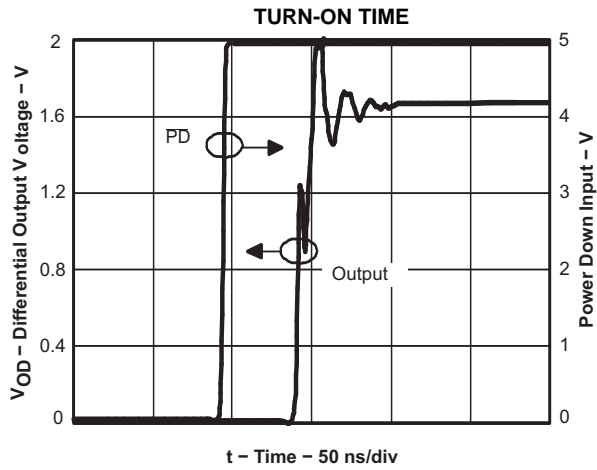


Figure 31.

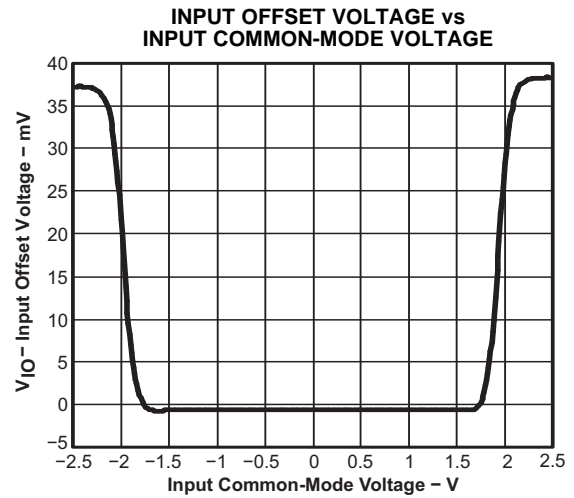


Figure 32.

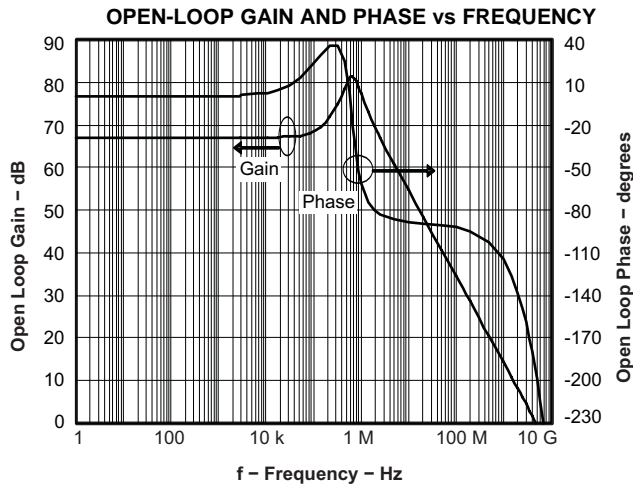


Figure 33.

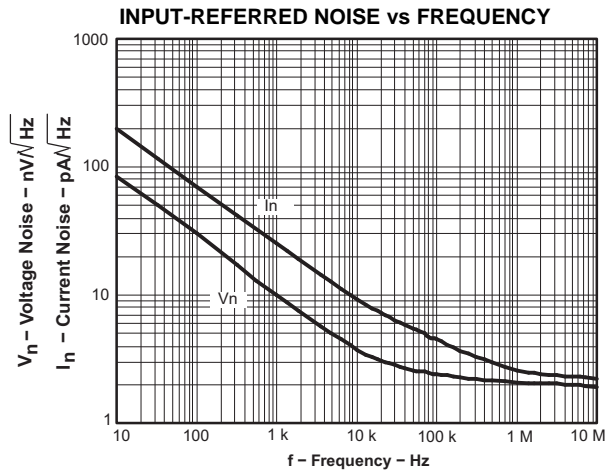


Figure 34.

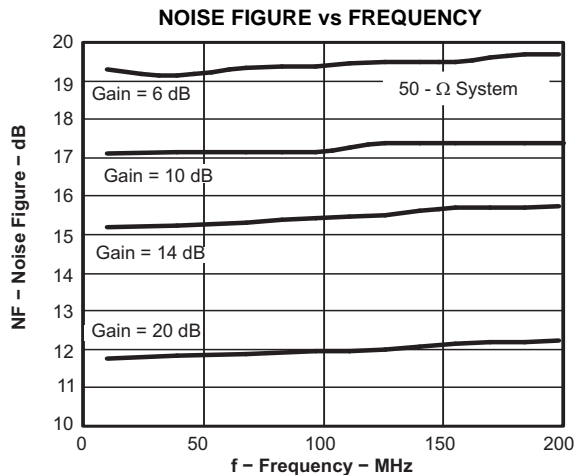


Figure 35.

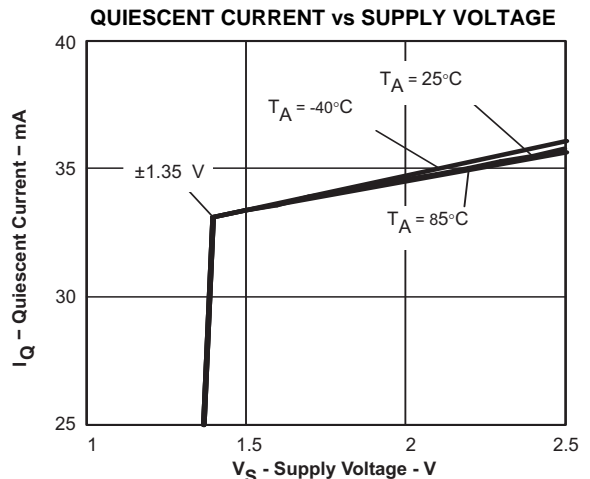


Figure 36.

**TYPICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 5\text{ V}$  (continued)**

Test conditions at  $V_{S+} = +2.5\text{ V}$ ,  $V_{S-} = -2.5\text{ V}$ , CM = open,  $V_O = 2\text{ V}_{PP}$ ,  $R_F = 349\ \Omega$ ,  $R_L = 200\ \Omega$  differential,  $G = 10\text{ dB}$ , single-ended input, and input and output referenced to midrail, unless otherwise noted.

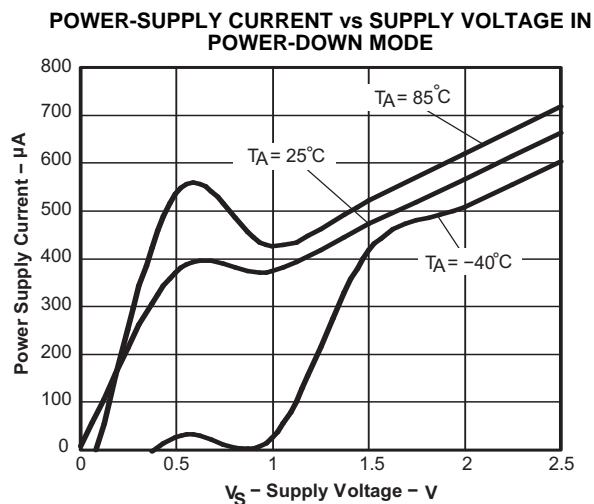


Figure 37.

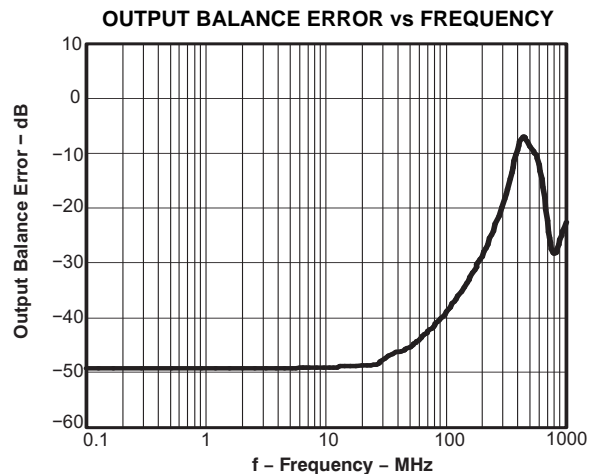


Figure 38.

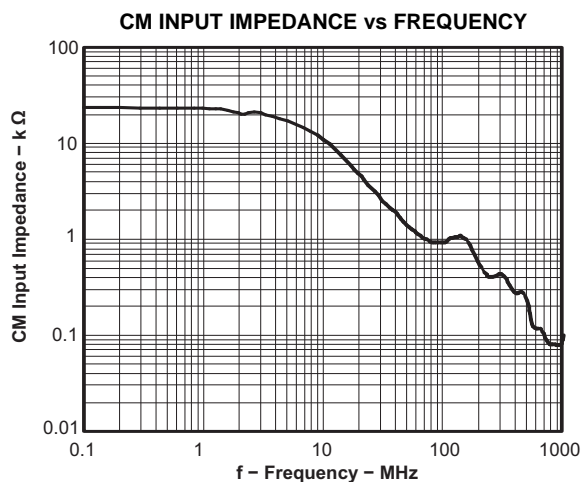


Figure 39.

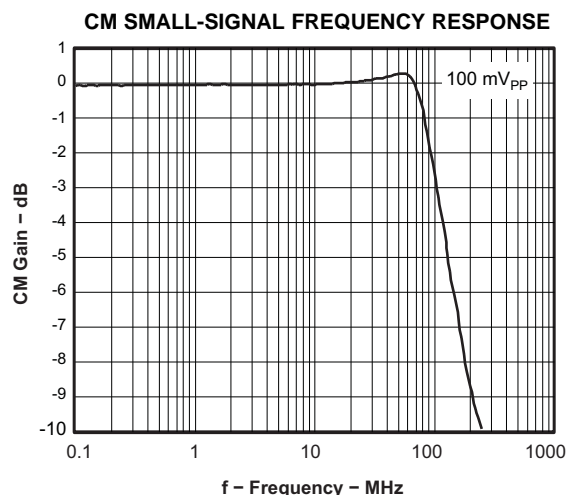


Figure 40.

**TYPICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 5\text{ V}$  (continued)**

Test conditions at  $V_{S+} = +2.5\text{ V}$ ,  $V_{S-} = -2.5\text{ V}$ , CM = open,  $V_O = 2\text{ V}_{PP}$ ,  $R_F = 349\ \Omega$ ,  $R_L = 200\ \Omega$  differential,  $G = 10\text{ dB}$ , single-ended input, and input and output referenced to midrail, unless otherwise noted.

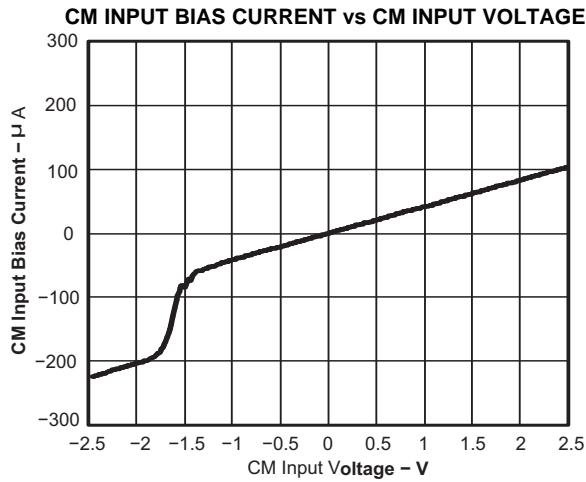


Figure 41.

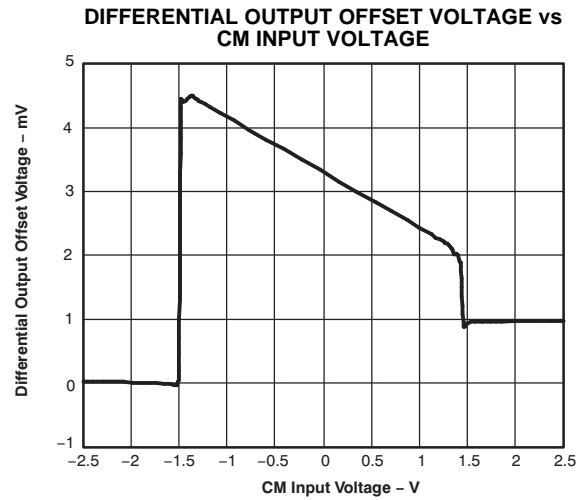


Figure 42.

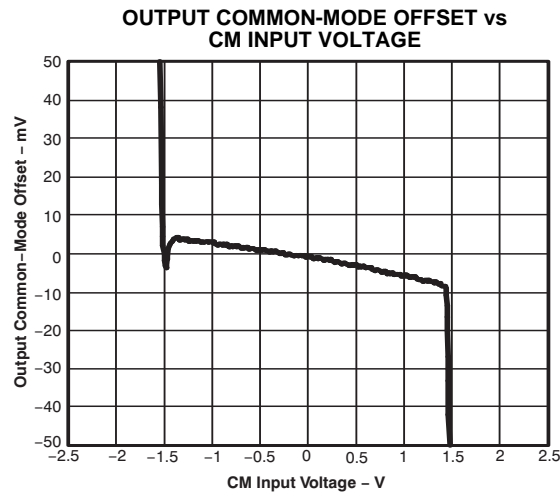


Figure 43.



**TYPICAL AC PERFORMANCE:  $V_{S+} - V_{S-} = 3\text{ V}$** 

Test conditions at  $V_{S+} = +1.5\text{ V}$ ,  $V_{S-} = -1.5\text{ V}$ , CM = open,  $V_{OD} = 1\text{ V}_{PP}$ ,  $R_F = 349\ \Omega$ ,  $R_L = 200\ \Omega$  differential,  $G = 10\text{ dB}$ , single-ended input, and input and output referenced to midrail, unless otherwise noted.

Small-Signal Frequency Response			<a href="#">Figure 44</a>
Large-Signal Frequency Response			<a href="#">Figure 45</a>
Harmonic Distortion	HD <sub>2</sub> , G = 6 dB, V <sub>OD</sub> = 1 V <sub>PP</sub>	vs Frequency	<a href="#">Figure 46</a>
	HD <sub>3</sub> , G = 6 dB, V <sub>OD</sub> = 1 V <sub>PP</sub>	vs Frequency	<a href="#">Figure 47</a>
	HD <sub>2</sub> , G = 10 dB, V <sub>OD</sub> = 1 V <sub>PP</sub>	vs Frequency	<a href="#">Figure 48</a>
	HD <sub>3</sub> , G = 10 dB, V <sub>OD</sub> = 1 V <sub>PP</sub>	vs Frequency	<a href="#">Figure 49</a>
	HD <sub>2</sub> , G = 14 dB, V <sub>OD</sub> = 1 V <sub>PP</sub>	vs Frequency	<a href="#">Figure 50</a>
	HD <sub>3</sub> , G = 14 dB, V <sub>OD</sub> = 1 V <sub>PP</sub>	vs Frequency	<a href="#">Figure 51</a>
Intermodulation Distortion	IMD <sub>2</sub> , G = 6 dB, V <sub>OD</sub> = 1 V <sub>PP</sub>	vs Frequency	<a href="#">Figure 52</a>
	IMD <sub>3</sub> , G = 6 dB, V <sub>OD</sub> = 1 V <sub>PP</sub>	vs Frequency	<a href="#">Figure 53</a>
	IMD <sub>2</sub> , G = 10 dB, V <sub>OD</sub> = 1 V <sub>PP</sub>	vs Frequency	<a href="#">Figure 54</a>
	IMD <sub>3</sub> , G = 10 dB, V <sub>OD</sub> = 1 V <sub>PP</sub>	vs Frequency	<a href="#">Figure 55</a>
	IMD <sub>2</sub> , G = 14 dB, V <sub>OD</sub> = 1 V <sub>PP</sub>	vs Frequency	<a href="#">Figure 56</a>
	IMD <sub>3</sub> , G = 14 dB, V <sub>OD</sub> = 1 V <sub>PP</sub>	vs Frequency	<a href="#">Figure 57</a>
Output Intercept Point	OIP <sub>2</sub>	vs Frequency	<a href="#">Figure 58</a>
	OIP <sub>3</sub>	vs Frequency	<a href="#">Figure 59</a>
0.1 dB Flatness			<a href="#">Figure 60</a>
S-Parameters		vs Frequency	<a href="#">Figure 61</a>
Transition Rate		vs Output Voltage	<a href="#">Figure 62</a>
Transient Response			<a href="#">Figure 63</a>
Settling Time			<a href="#">Figure 64</a>
Output Voltage Swing		vs Load Resistance	<a href="#">Figure 65</a>
Rejection Ratio		vs Frequency	<a href="#">Figure 66</a>
Overdrive Recovery			<a href="#">Figure 67</a>
Output Impedance		vs Frequency	<a href="#">Figure 68</a>
Turn-Off Time			<a href="#">Figure 69</a>
Turn-On Time			<a href="#">Figure 70</a>
Output Balance Error		vs Frequency	<a href="#">Figure 71</a>
Noise Figure		vs Frequency	<a href="#">Figure 72</a>
CM Input Impedance		vs Frequency	<a href="#">Figure 73</a>
Differential Output Offset Voltage		vs CM Input Voltage	<a href="#">Figure 74</a>
Output Common-Mode Offset		vs CM Input Voltage	<a href="#">Figure 75</a>

**TYPICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 3\text{ V}$**

Test conditions at  $V_{S+} = +1.5\text{ V}$ ,  $V_{S-} = -1.5\text{ V}$ , CM = open,  $V_{OD} = 1\text{ V}_{PP}$ ,  $R_F = 349\ \Omega$ ,  $R_L = 200\ \Omega$  differential,  $G = 10\text{ dB}$ , single-ended input, and input and output referenced to midrail, unless otherwise noted.

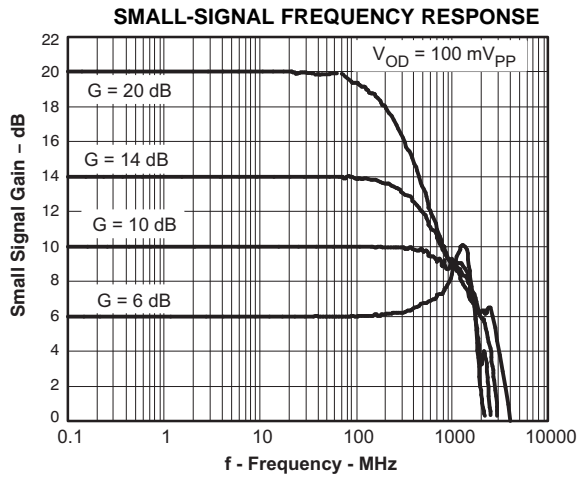


Figure 44.

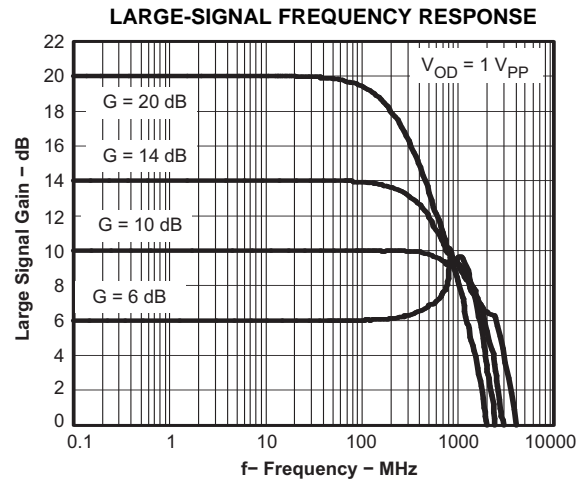


Figure 45.

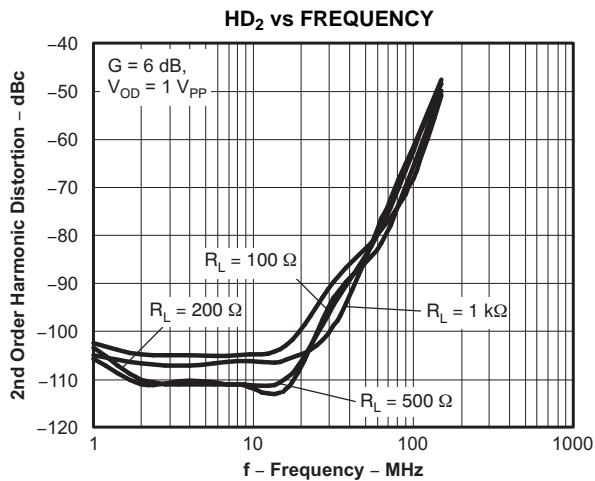


Figure 46.

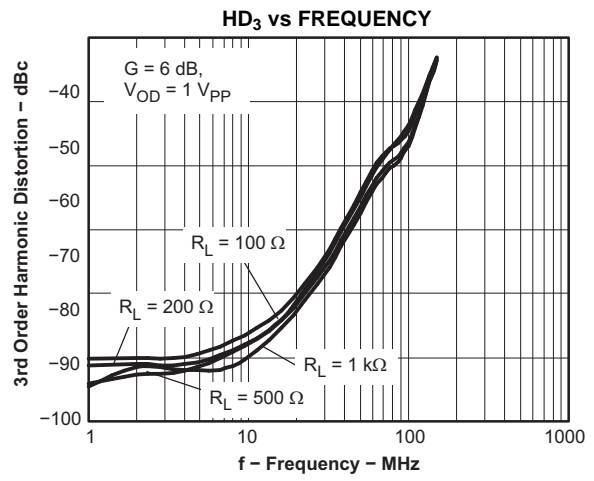


Figure 47.

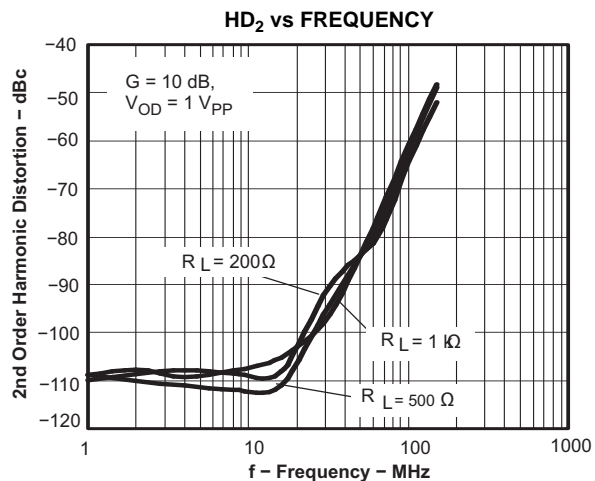


Figure 48.

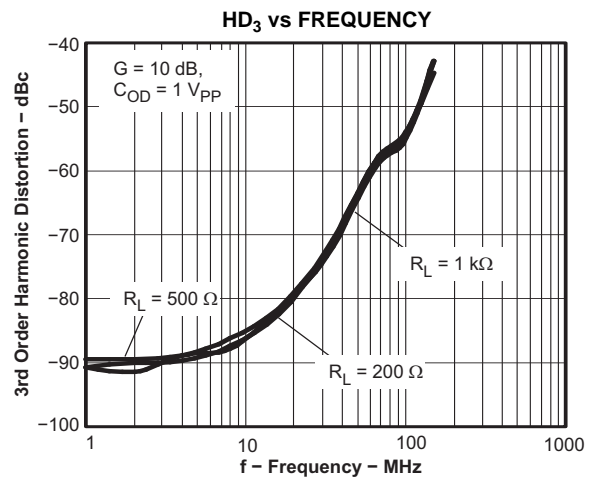


Figure 49.

**TYPICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 3\text{ V}$  (continued)**

Test conditions at  $V_{S+} = +1.5\text{ V}$ ,  $V_{S-} = -1.5\text{ V}$ , CM = open,  $V_{OD} = 1\text{ V}_{PP}$ ,  $R_F = 349\ \Omega$ ,  $R_L = 200\ \Omega$  differential,  $G = 10\text{ dB}$ , single-ended input, and input and output referenced to midrail, unless otherwise noted.

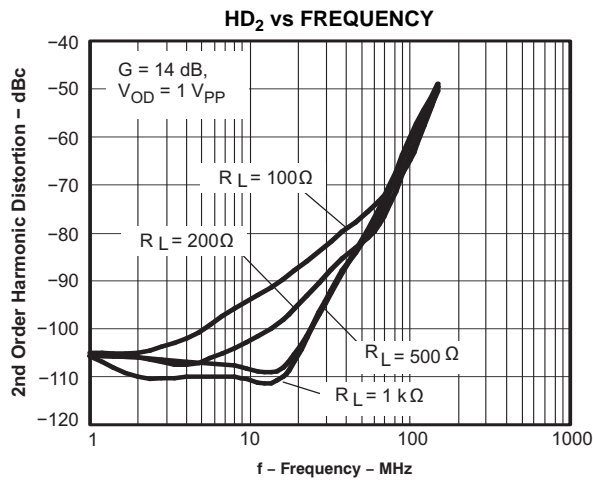


Figure 50.

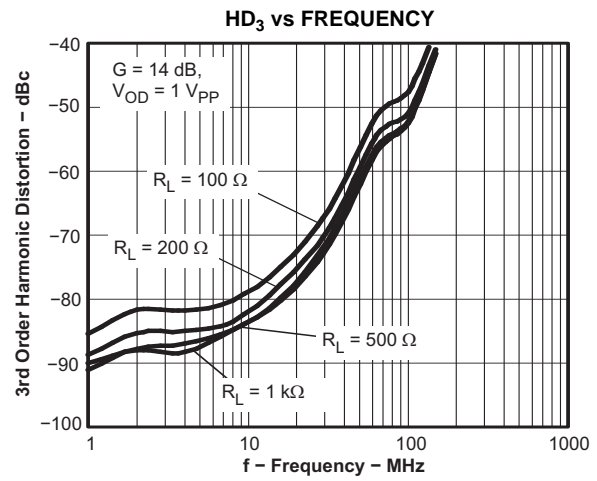


Figure 51.

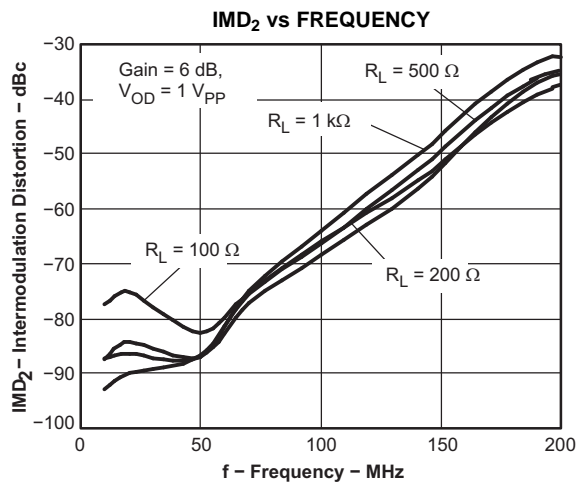


Figure 52.

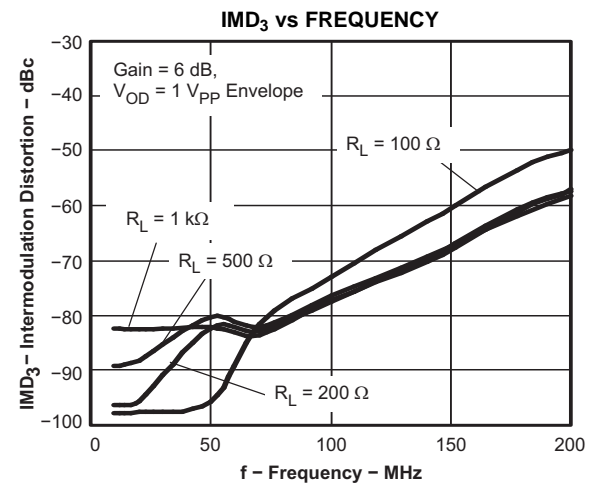


Figure 53.

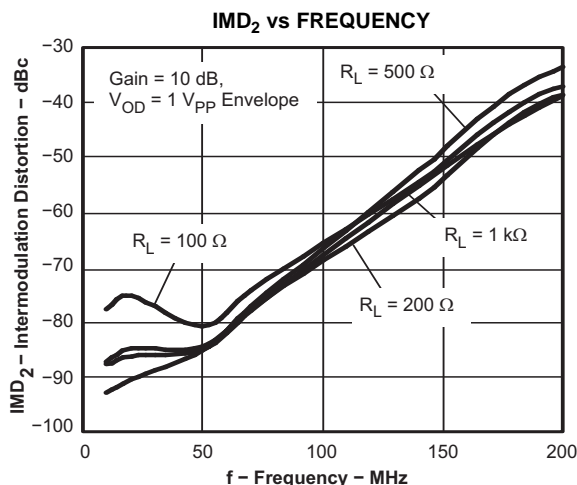


Figure 54.

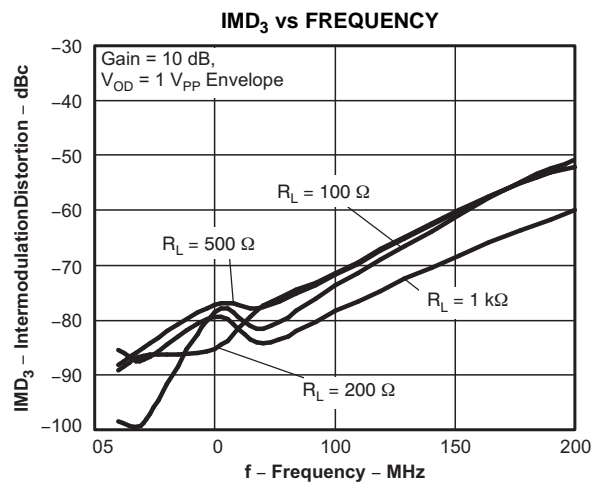


Figure 55.

**TYPICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 3\text{ V}$  (continued)**

Test conditions at  $V_{S+} = +1.5\text{ V}$ ,  $V_{S-} = -1.5\text{ V}$ , CM = open,  $V_{OD} = 1\text{ V}_{PP}$ ,  $R_F = 349\ \Omega$ ,  $R_L = 200\ \Omega$  differential, G = 10 dB, single-ended input, and input and output referenced to midrail, unless otherwise noted.

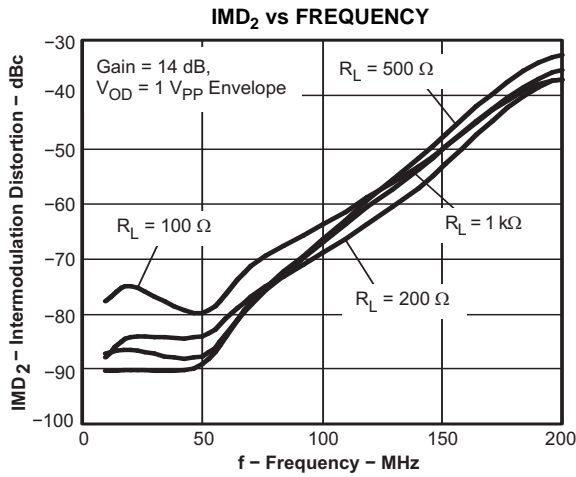


Figure 56.

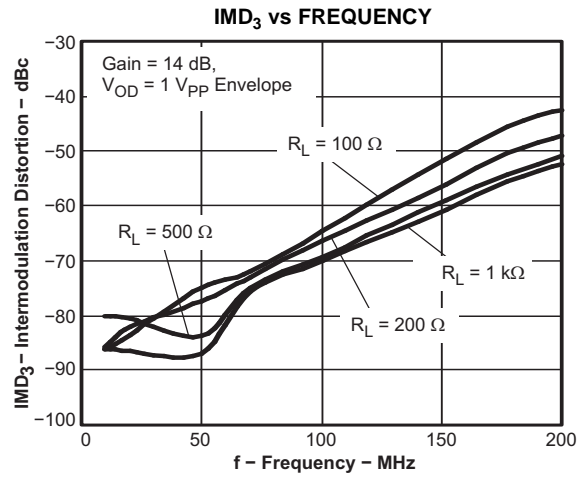


Figure 57.

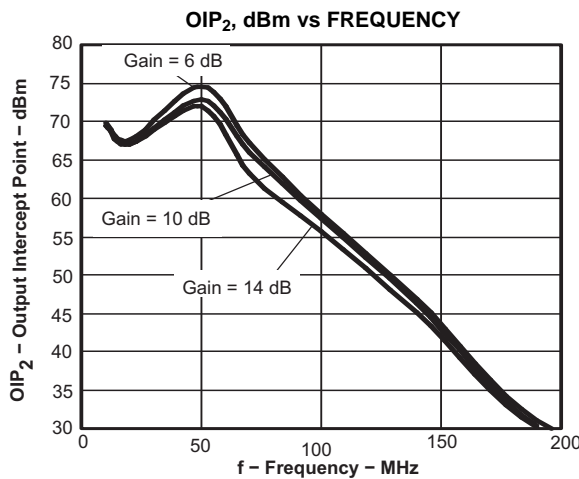


Figure 58.

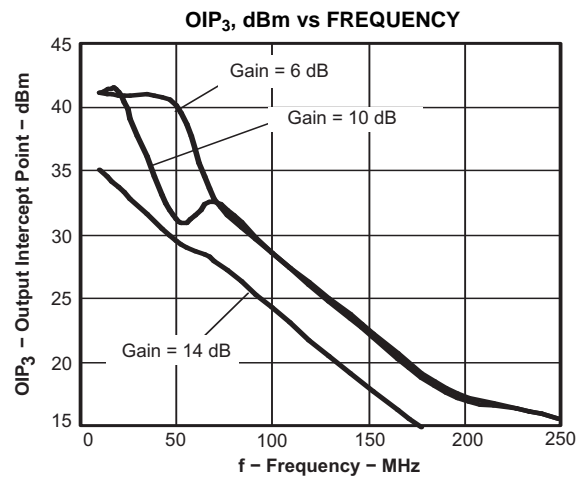


Figure 59.

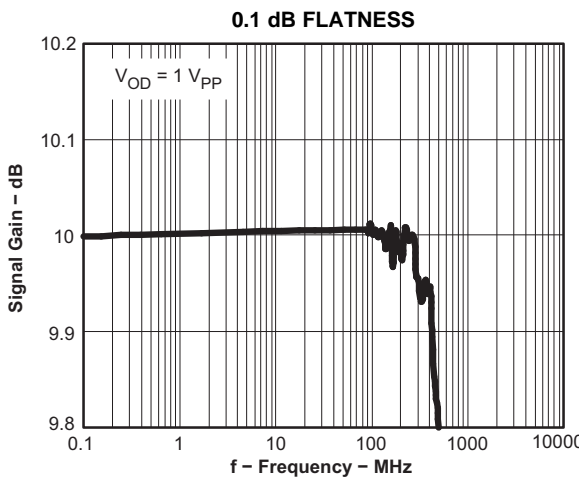


Figure 60.

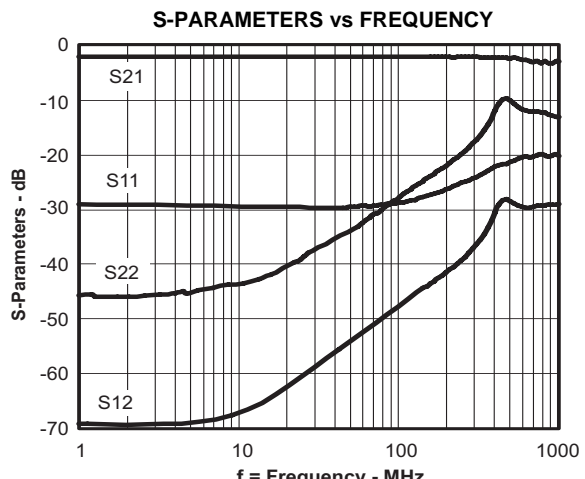


Figure 61.

**TYPICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 3\text{ V}$  (continued)**

Test conditions at  $V_{S+} = +1.5\text{ V}$ ,  $V_{S-} = -1.5\text{ V}$ , CM = open,  $V_{OD} = 1\text{ V}_{PP}$ ,  $R_F = 349\ \Omega$ ,  $R_L = 200\ \Omega$  differential, G = 10 dB, single-ended input, and input and output referenced to midrail, unless otherwise noted.

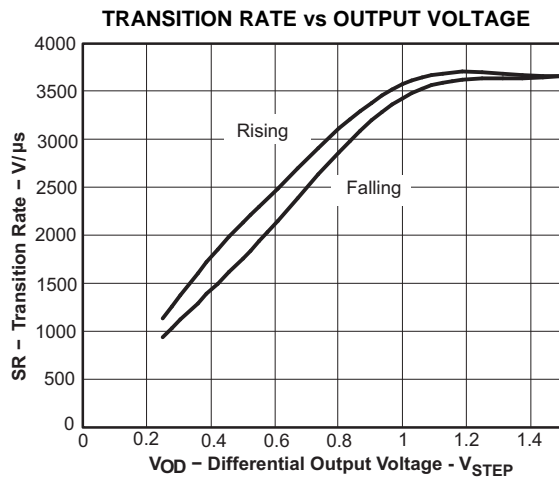


Figure 62.

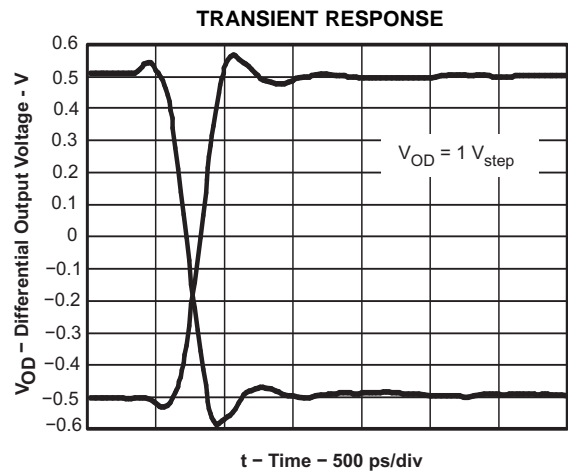


Figure 63.

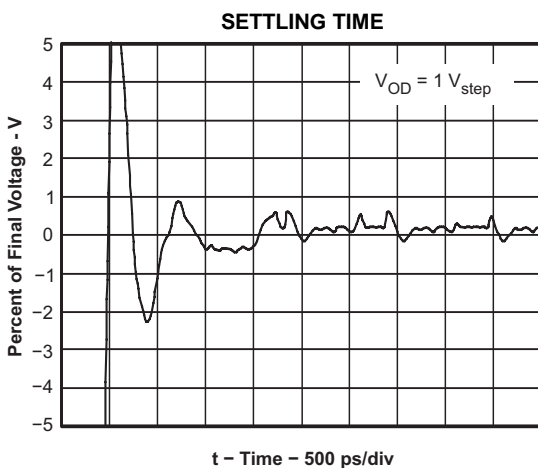


Figure 64.

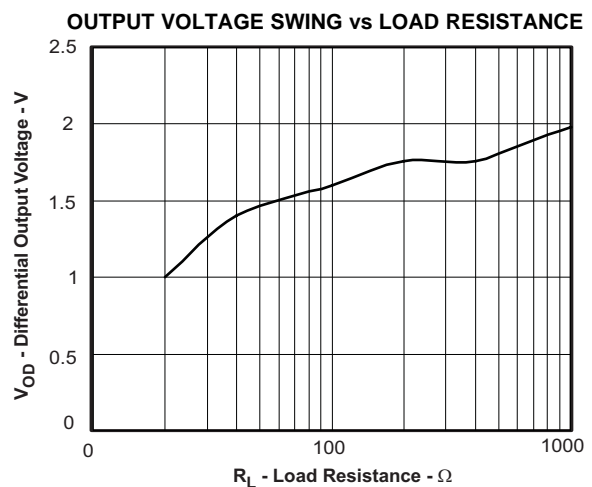


Figure 65.

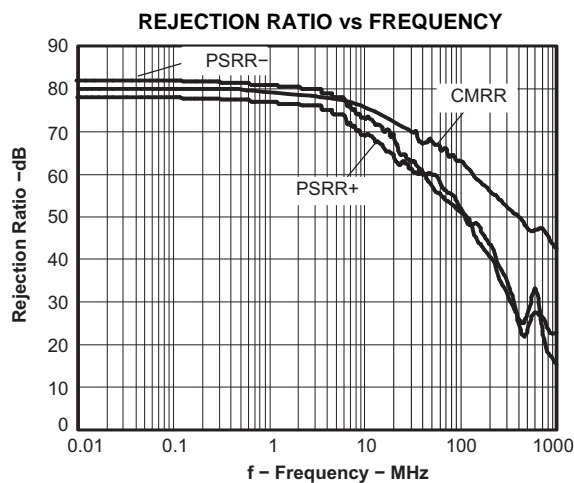


Figure 66.

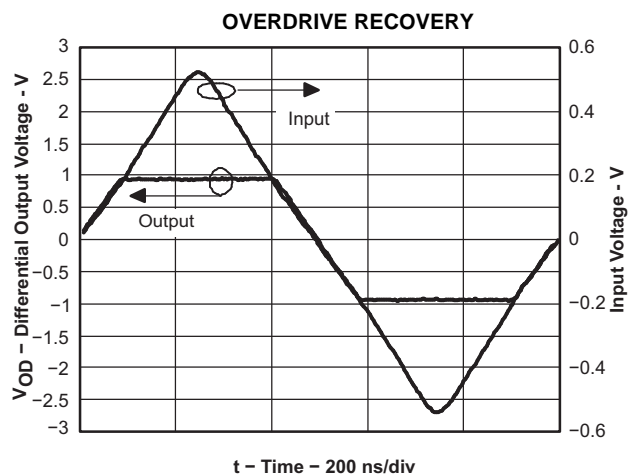


Figure 67.

**TYPICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 3\text{ V}$  (continued)**

Test conditions at  $V_{S+} = +1.5\text{ V}$ ,  $V_{S-} = -1.5\text{ V}$ , CM = open,  $V_{OD} = 1\text{ V}_{PP}$ ,  $R_F = 349\ \Omega$ ,  $R_L = 200\ \Omega$  differential, G = 10 dB, single-ended input, and input and output referenced to midrail, unless otherwise noted.

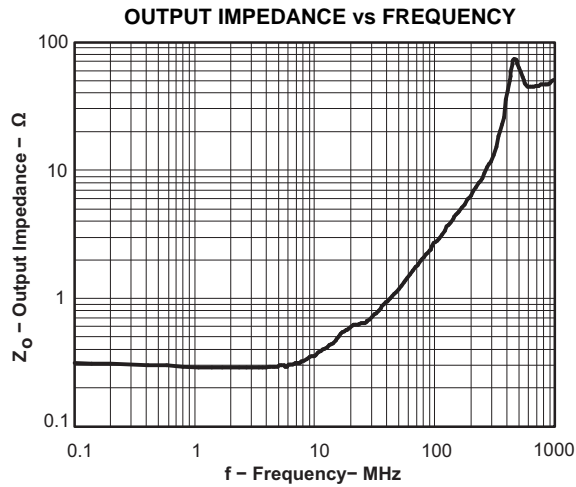


Figure 68.

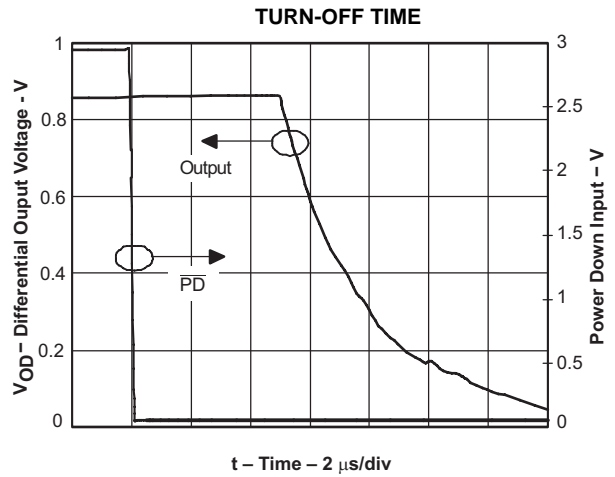


Figure 69.

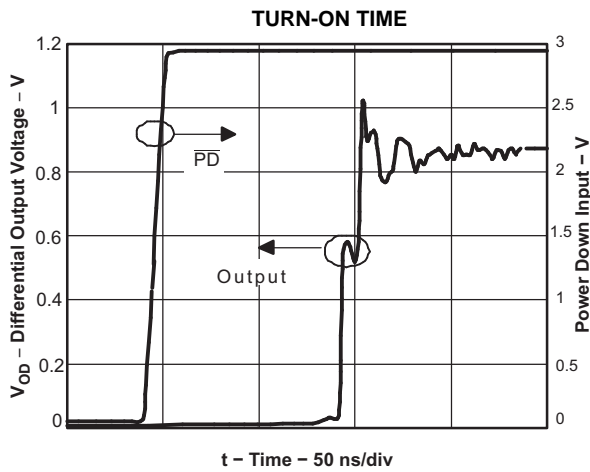


Figure 70.

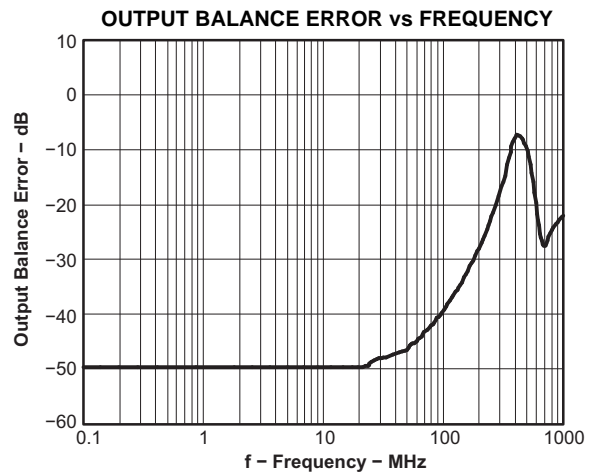


Figure 71.

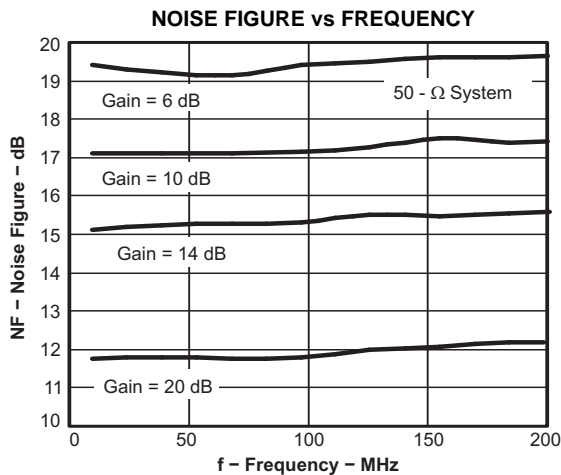


Figure 72.

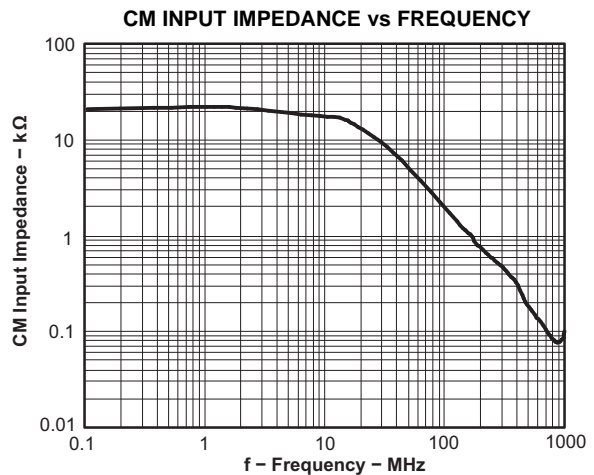


Figure 73.

**TYPICAL CHARACTERISTICS:  $V_{S+} - V_{S-} = 3\text{ V}$  (continued)**

Test conditions at  $V_{S+} = +1.5\text{ V}$ ,  $V_{S-} = -1.5\text{ V}$ , CM = open,  $V_{OD} = 1\text{ V}_{PP}$ ,  $R_F = 349\ \Omega$ ,  $R_L = 200\ \Omega$  differential,  $G = 10\text{ dB}$ , single-ended input, and input and output referenced to midrail, unless otherwise noted.

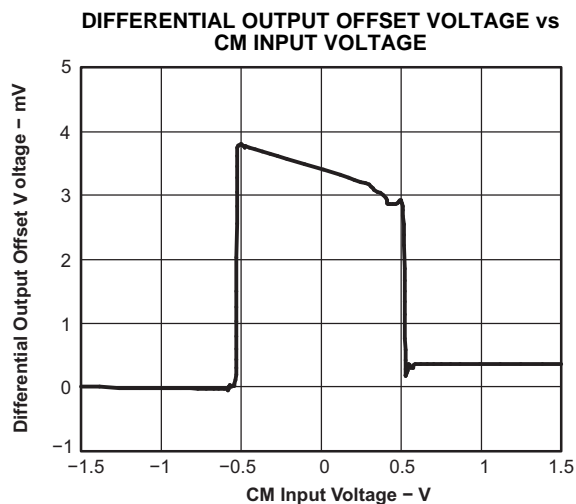


Figure 74.

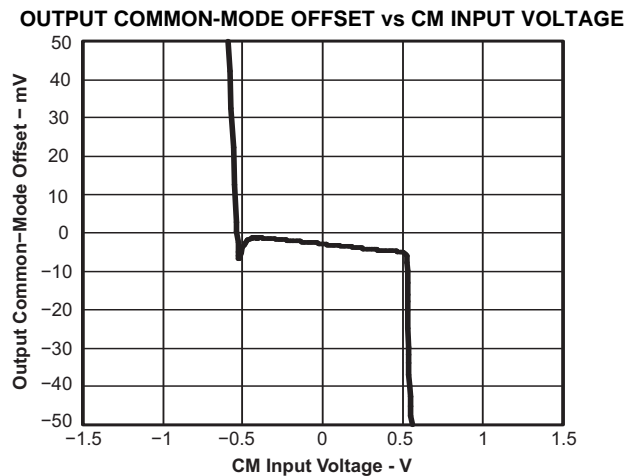


Figure 75.

### TEST CIRCUITS

The THS4509 is tested with the following test circuits built on the EVM. For simplicity, power-supply decoupling is not shown—see the [Layout Recommendations](#) section in the applications section for recommendations. Depending on the test conditions, component values are changed per the following tables, or as otherwise noted. The signal generators used are ac-coupled, 50-Ω sources and a 0.22-μF capacitor and a 49.9-Ω resistor to ground are inserted across  $R_{IT}$  on the alternate input to balance the circuit. A split power supply is used to ease the interface to common test equipment, but the amplifier can be operated single-supply as described in the applications section with no impact on performance.

**Table 1. Gain Component Values**

GAIN	$R_F$	$R_G$	$R_{IT}$
6 dB	348 Ω	165 Ω	61.9 Ω
10 dB	348 Ω	100 Ω	69.8 Ω
14 dB	348 Ω	56.2 Ω	88.7 Ω
20 dB	348 Ω	16.5 Ω	287 Ω

**Note the gain setting includes 50-Ω source impedance. Components are chosen to achieve gain and 50-Ω input termination.**

**Table 2. Load Component Values**

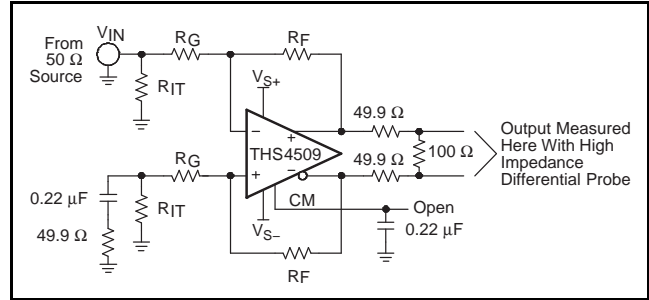
$R_L$	$R_O$	$R_{OT}$	Atten.
100 Ω	25 Ω	Open	6 dB
200 Ω	86.6 Ω	69.8 Ω	16.8 dB
499 Ω	237 Ω	56.2 Ω	25.5 dB
1k Ω	487 Ω	52.3 Ω	31.8 dB

**Note the total load includes 50-Ω termination by the test equipment. Components are chosen to achieve load and 50-Ω line termination through a 1:1 transformer.**

Due to the voltage divider on the output formed by the load component values, the amplifier output is attenuated. The column *Atten* in [Table 2](#) shows the attenuation expected from the resistor divider. When using a transformer at the output as shown in [Figure 77](#), the signal will see slightly more loss, and these numbers will be approximate.

### Frequency Response

The circuit shown in [Figure 76](#) is used to measure the frequency response of the circuit.



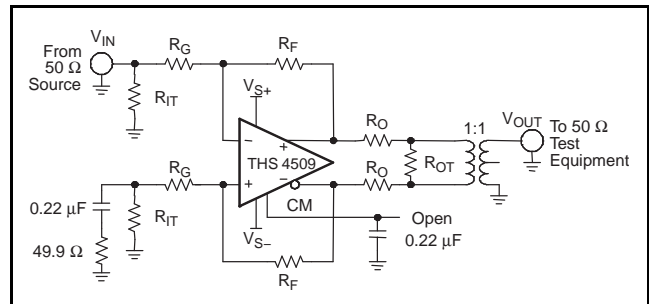
**Figure 76. Frequency Response Test Circuit**

A network analyzer is used as the signal source and as the measurement device. The output impedance of the network analyzer is 50 Ω.  $R_{IT}$  and  $R_G$  are chosen to impedance match to 50 Ω, and to maintain the proper gain. To balance the amplifier, a 0.22-μF capacitor and a 49.9-Ω resistor to ground are inserted across  $R_{IT}$  on the alternate input.

The output is probed using a high-impedance differential probe across the 100-Ω resistor. The gain is referred to the amplifier output by adding back the 6-dB loss due to the voltage divider on the output.

### Distortion and 1-dB Compression

The circuit shown in [Figure 77](#) is used to measure harmonic distortion, intermodulation distortion, and 1-dB compression point of the amplifier.



**Figure 77. Distortion Test Circuit**



A signal generator is used as the signal source and the output is measured with a spectrum analyzer. The output impedance of the signal generator is 50 Ω.  $R_{IT}$  and  $R_G$  are chosen to impedance-match to 50 Ω, and to maintain the proper gain. To balance the amplifier, a 0.22-μF capacitor and 49.9-Ω resistor to ground are inserted across  $R_{IT}$  on the alternate input.

A low-pass filter is inserted in series with the input to reduce harmonics generated at the signal source. The level of the fundamental is measured, then a high-pass filter is inserted at the output to reduce the fundamental so that it does not generate distortion in the input of the spectrum analyzer.

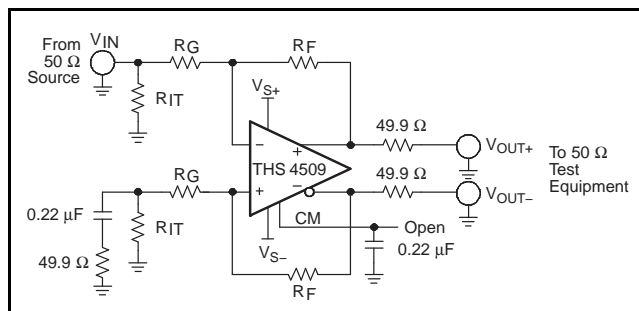
The transformer used in the output to convert the signal from differential to single-ended is an ADT1-1WT. It limits the frequency response of the circuit so that measurements cannot be made below approximately 1 MHz.

The 1-dB compression point is measured with a spectrum analyzer with 50-Ω double termination or 100-Ω termination; see Table 2. The input power is increased until the output is 1 dB lower than expected. The number reported in the table data is the power delivered to the spectrum analyzer input. Add 3 dB to refer to the amplifier output.

### S-Parameter, Slew Rate, Transient Response, Settling Time, Output Impedance, Overdrive, Output Voltage, and Turn-On/Off Time

The circuit shown in Figure 78 is used to measure s-parameters, slew rate, transient response, settling time, output impedance, overdrive recovery, output voltage swing, and turn-on/turn-off times of the amplifier. For output impedance, the signal is injected at  $V_{OUT}$  with  $V_{IN}$  left open and the drop across the 49.9 Ω resistor is used to calculate the impedance seen looking into the amplifier's output.

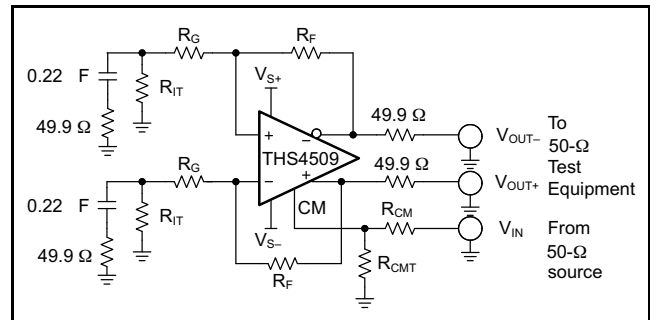
Because  $S_{21}$  is measured single-ended at the load with 50-Ω double termination, add 12 dB to refer to the amplifier output as a differential signal.



**Figure 78. S-Parameter, SR, Transient Response, Settling Time,  $Z_0$ , Overdrive Recovery,  $V_{OUT}$  Swing, and Turn-on/off Test Circuit**

### CM Input

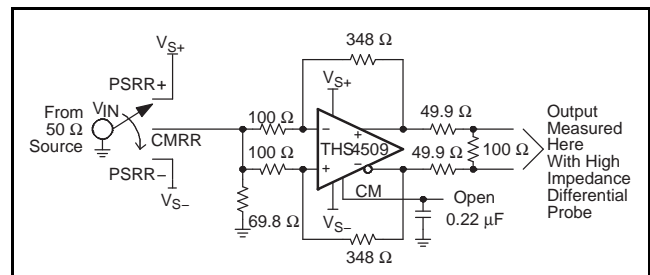
The circuit shown in Figure 79 is used to measure the frequency response and input impedance of the CM input. Frequency response is measured single-ended at  $V_{OUT+}$  or  $V_{OUT-}$  with the input injected at  $V_{IN}$ ,  $R_{CM} = 0 \Omega$  and  $R_{CMT} = 49.9 \Omega$ . The input impedance is measured with  $R_{CM} = 49.9 \Omega$  with  $R_{CMT} = \text{open}$ , and calculated by measuring the voltage drop across  $R_{CM}$  to determine the input current.



**Figure 79. CM Input Test Circuit**

### CMRR and PSRR

The circuit shown in Figure 80 is used to measure the CMRR and PSRR of  $V_{S+}$  and  $V_{S-}$ . The input is switched appropriately to match the test being performed.



**Figure 80. CMRR and PSRR Test Circuit**

APPLICATION INFORMATION

APPLICATIONS

The following circuits show application information for the THS4509. For simplicity, power-supply decoupling capacitors are not shown in these diagrams. Please see the [THS4509 EVM](#) section for recommendations. For more detail on the use and operation of fully differential op amps refer to application report *Fully-Differential Amplifiers* (SLOA054).

Differential Input to Differential Output Amplifier

The THS4509 is a fully differential op amp, and can be used to amplify differential input signals to differential output signals. A basic block diagram of the circuit is shown in [Figure 81](#) (CM input not shown). The gain of the circuit is set by  $R_F$  divided by  $R_G$ .

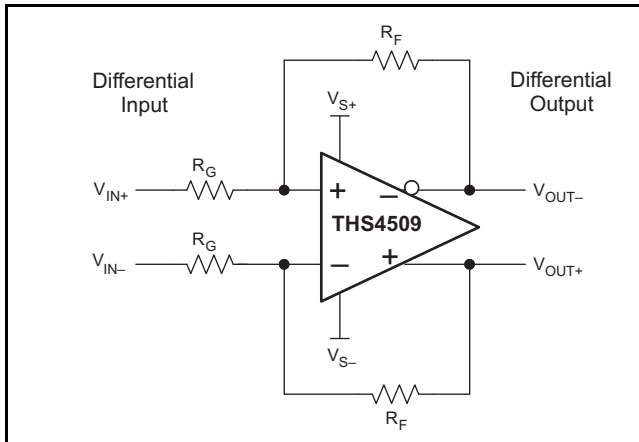


Figure 81. Differential Input to Differential Output Amplifier

Depending on the source and load, input and output termination can be accomplished by adding  $R_{IT}$  and  $R_O$ .

Single-Ended Input to Differential Output Amplifier

The THS4509 can be used to amplify and convert single-ended input signals to differential output signals. A basic block diagram of the circuit is shown in [Figure 82](#) (CM input not shown). The gain of the circuit is again set by  $R_F$  divided by  $R_G$ .

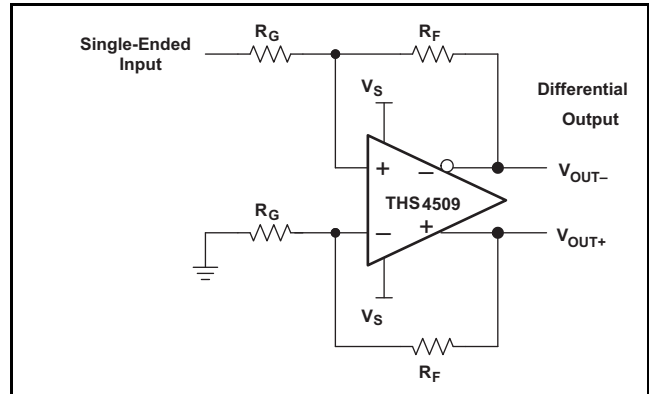


Figure 82. Single-Ended Input to Differential Output Amplifier

Input Common-Mode Voltage Range

The input common-mode voltage of a fully differential op amp is the voltage at the '+' and '-' input pins of the op amp.

It is important to not violate the input common-mode voltage range ( $V_{ICR}$ ) of the op amp. Assuming the op amp is in linear operation the voltage across the input pins is only a few millivolts at most. So finding the voltage at one input pin will determine the input common-mode voltage of the op amp.

Treating the negative input as a summing node, the voltage is given by [Equation 1](#):

$$V_{IC} = \left( V_{OUT+} \times \frac{R_G}{R_G + R_F} \right) + \left( V_{IN-} \times \frac{R_F}{R_G + R_F} \right) \tag{1}$$

To determine the  $V_{ICR}$  of the op amp, the voltage at the negative input is evaluated at the extremes of  $V_{OUT+}$ .

As the gain of the op amp increases, the input common-mode voltage becomes closer and closer to the input common-mode voltage of the source.

### Setting the Output Common-Mode Voltage

The output common-mode voltage is set by the voltage at the CM pin(s). The internal common-mode control circuit maintains the output common-mode voltage within 3-mV offset (typ) from the set voltage, when set within 0.5 V of mid-supply, with less than 4-mV differential offset voltage. If left unconnected, the common-mode set point is set to mid-supply by internal circuitry, which may be over-driven from an external source. Figure 83 is representative of the CM input. The internal CM circuit has about 700 MHz of –3-dB bandwidth, which is required for best performance, but it is intended to be a dc bias input pin. Bypass capacitors are recommended on this pin to reduce noise at the output. The external current required to overdrive the internal resistor divider is given by Equation 2:

$$I_{EXT} = \frac{2V_{CM} - (V_{S+} - V_{S-})}{50 \text{ k}\Omega} \quad (2)$$

where  $V_{CM}$  is the voltage applied to the CM pin.

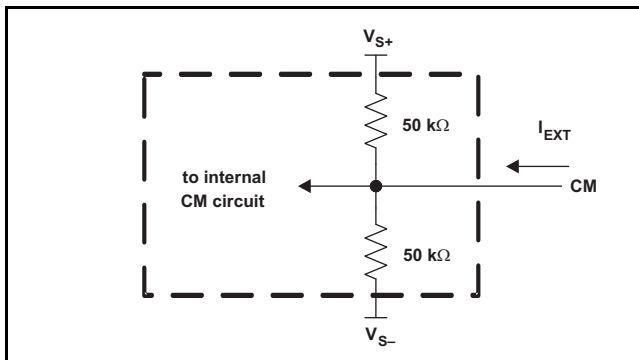


Figure 83. CM Input Circuit

### Single-Supply Operation (3 V to 5 V)

To facilitate testing with common lab equipment, the THS4509 EVM allows split-supply operation, and the characterization data presented in this data sheet was taken with split-supply power inputs. The device can easily be used with a single-supply power input without degrading the performance. Figure 84, Figure 85, and Figure 86 show dc and ac-coupled single-supply circuits with single-ended inputs. These configurations all allow the input and output common-mode voltage to be set to mid-supply allowing for optimum performance. The information presented here can also be applied to differential input sources.

In Figure 84, the source is referenced to the same voltage as the CM pin ( $V_{CM}$ ).  $V_{CM}$  is set by the internal circuit to mid-supply.  $R_T$  along with the input impedance of the amplifier circuit provides input termination, which is also referenced to  $V_{CM}$ .

Note that  $R_S$  and  $R_T$  are added to the alternate input from the signal input to balance the amplifier. Alternately, one resistor can be used equal to the combined value  $R_G + R_S || R_T$  on this input. This is also true of the circuits shown in Figure 85 and Figure 86.

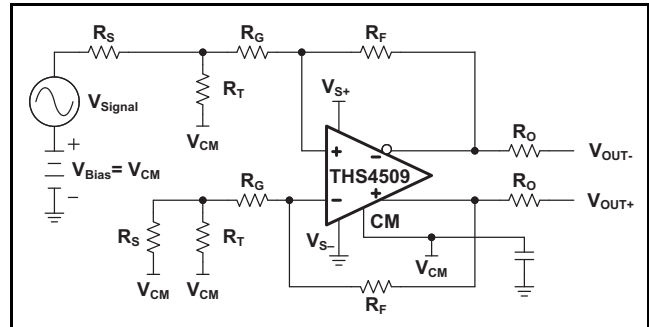


Figure 84. THS4509 DC-Coupled Single-Supply with Input Biased to  $V_{CM}$

In Figure 85 the source is referenced to ground and so is the input termination resistor.  $R_{PU}$  is added to the circuit to avoid violating the  $V_{ICR}$  of the op amp. The proper value of resistor to add can be calculated from Equation 3:

$$R_{PU} = \frac{(V_{IC} - V_{S+})}{V_{CM} \left( \frac{1}{R_F} \right) - V_{IC} \left( \frac{1}{R_{IN}} + \frac{1}{R_F} \right)} \quad (3)$$

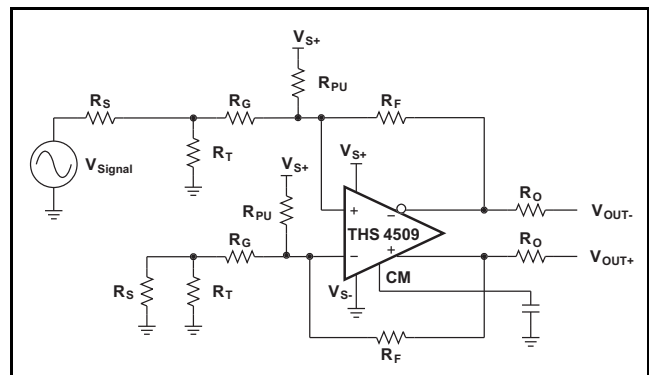


Figure 85. THS4509 DC-Coupled Single-Supply with  $R_{PU}$  Used to Set  $V_{IC}$

$V_{IC}$  is the desired input common-mode voltage,  $V_{CM} = CM$ , and  $R_{IN} = R_G + R_S || R_T$ . To set to mid-supply, make the value of  $R_{PU} = R_G + R_S || R_T$ .

Table 3 is a modification of Table 1 to add the proper values with  $R_{PU}$  assuming a 50-Ω source impedance and setting the input and output common-mode voltage to mid-supply.

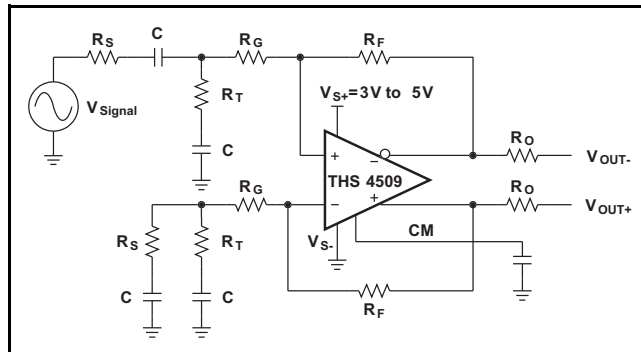
**Table 3. R<sub>PU</sub> Values for Various Gains**

Gain	R <sub>F</sub>	R <sub>G</sub>	R <sub>IT</sub>	R <sub>PU</sub>
6 dB	348 Ω	169 Ω	64.9 Ω	200 Ω
10 dB	348 Ω	102 Ω	78.7 Ω	133 Ω
14 dB	348 Ω	61.9 Ω	115 Ω	97.6 Ω
20 dB	348 Ω	40.2 Ω	221 Ω	80.6 Ω

There are two drawbacks to this configuration. One is that it requires additional current from the power supply. Using the values shown for a gain of 10 dB requires 37 mA more current with 5-V supply, and 22 mA more current with 3-V supply.

The other drawback is this configuration also increases the noise gain of the circuit. In the 10-dB gain case, noise gain increases by a factor of 1.5.

Figure 86 shows ac coupling to the source. Using capacitors in series with the termination resistors allows the amplifier to self-bias both input and output to mid-supply.

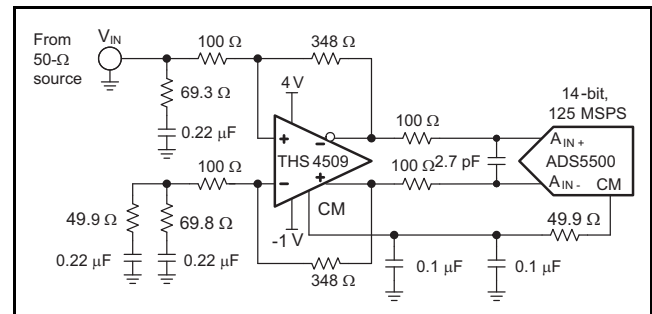


**Figure 86. THS4509 AC-Coupled Single-Supply**

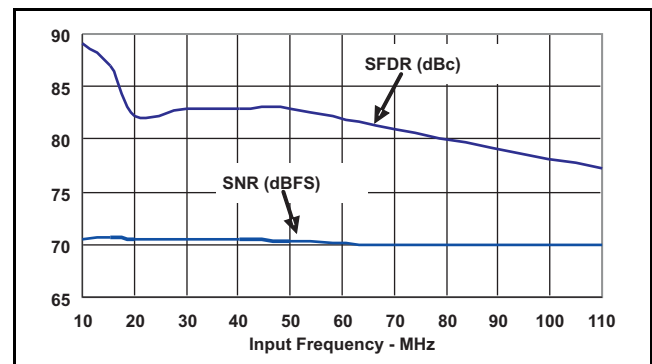
**THS4509 + ADS5500 Combined Performance**

The THS4509 is designed to be a high performance drive amplifier for high performance data converters like the ADS5500 14-bit 125-MSPS ADC. Figure 87 shows a circuit combining the two devices, and Figure 88 shows the combined SNR and SFDR performance versus frequency with -1 dBFS input signal level sampling at 125 MSPS. The THS4509 amplifier circuit provides 10 dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5500. The 100-Ω resistors and 2.7-pF capacitor between the THS4509 outputs and ADS5500 inputs along with the input capacitance of the ADS5500 limit the bandwidth of the signal to 115 MHz (-3 dB). For testing, a signal generator is used for the signal source. The generator is an ac-coupled 50-Ω source. A band-pass filter is inserted in series with the input to reduce harmonics and noise from the signal source. Input termination is accomplished via the 69.8-Ω resistor and 0.22-μF capacitor to ground in conjunction with the input impedance of the amplifier circuit. A 0.22-μF

capacitor and 49.9-Ω resistor is inserted to ground across the 69.8-Ω resistor and 0.22-μF capacitor on the alternate input to balance the circuit. Gain is a function of the source impedance, termination, and 348-Ω feedback resistor. Refer to Table 3 for component values to set proper 50-Ω termination for other common gains. A split power supply of +4V and -1V is used to set the input and output common-mode voltages to approximately mid-supply while setting the input common-mode of the ADS5500 to the recommended +1.55V. This maintains maximum headroom on the internal transistors of the THS4509 to insure optimum performance.



**Figure 87. THS4509 + ADS5500 Circuit**



**Figure 88. THS4509 + ADS5500 SFDR and SNR Performance versus Frequency**

Figure 89 shows the two-tone FFT of the THS4509 + ADS5500 circuit with 65 MHz and 70 MHz input frequencies. The SFDR is 90 dBc.

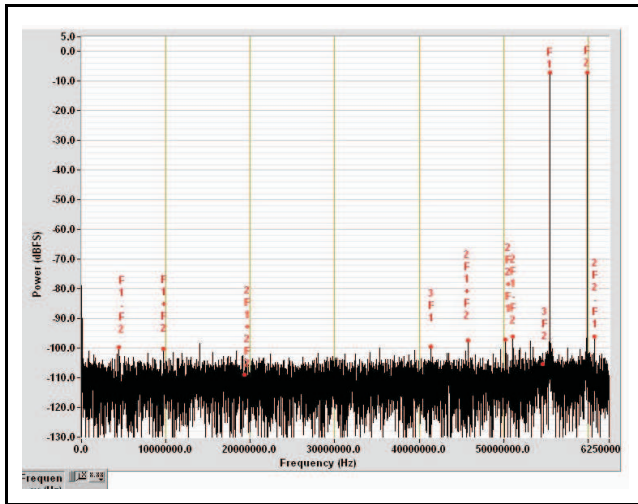


Figure 89. THS4509 and ADS5500 2-Tone FFT with 65 MHz and 70 MHz Input

### THS4509 + ADS5424 Combined Performance

Figure 90 shows the THS4509 driving the ADS5424 ADC, and Figure 91 shows their combined SNR and SFDR performance versus frequency with  $-1$  dBFS input signal level and sampling at 80 MSPS.

As before, the THS4509 amplifier provides 10 dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5424. Input termination and circuit testing is the same as described above for the THS4509 + ADS5500 circuit.

The 225- $\Omega$  resistors and 2.7-pF capacitor between the THS4509 outputs and ADS5424 inputs (along with the input capacitance of the ADC) limit the bandwidth of the signal to about 100MHz ( $-3$  dB).

Since the ADS5424 recommended input common-mode voltage is 2.4 V, the THS4509 is operated from a single power-supply input with  $V_{S+} = 5$  V and  $V_{S-} = 0$  V (ground).

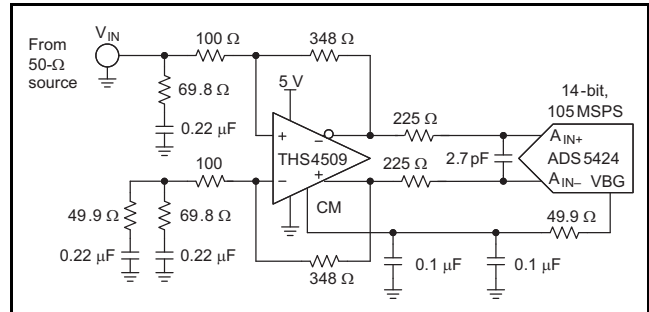


Figure 90. THS4509 + ADS5424 Circuit

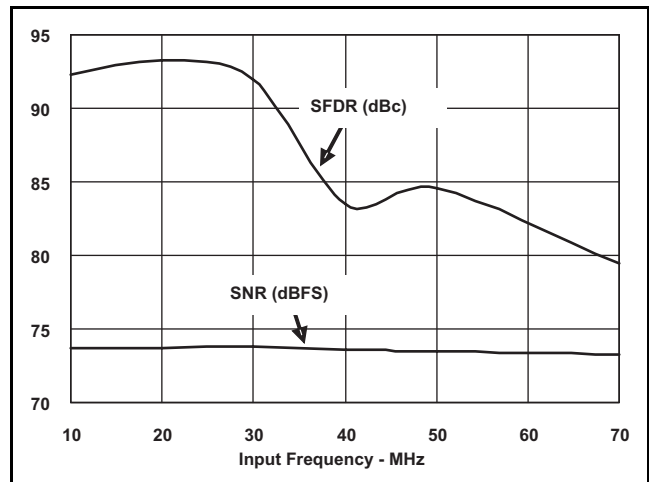


Figure 91. THS4509 + ADS5424 SFDR and SNR Performance vs Frequency

## Layout Recommendations

It is recommended to follow the layout of the external components near the amplifier, ground plane construction, and power routing of the EVM as closely as possible. General guidelines are:

1. Signal routing should be direct and as short as possible into and out of the op amp circuit.
2. The feedback path should be short and direct avoiding vias.
3. Ground or power planes should be removed from directly under the amplifier input and output pins.
4. An output resistor is recommended on each output, as near to the output pin as possible.
5. Two 10- $\mu$ F and two 0.1- $\mu$ F power-supply decoupling capacitors should be placed as near to the power-supply pins as possible.
6. Two 0.1- $\mu$ F capacitors should be placed between the CM input pins and ground. This limits noise coupled into the pins. One each should be placed to ground near pin 4 and pin 9.
7. It is recommended to split the ground panel on layer 2 (L2) as shown below and to use a solid ground on layer 3 (L3). A single-point connection should be used between each split section on L2 and L3.
8. A single-point connection to ground on L2 is recommended for the input termination resistors R1 and R2. This should be applied to the input gain resistors if termination is not used.
9. The THS4509 recommended PCB footprint is shown in Figure 92.

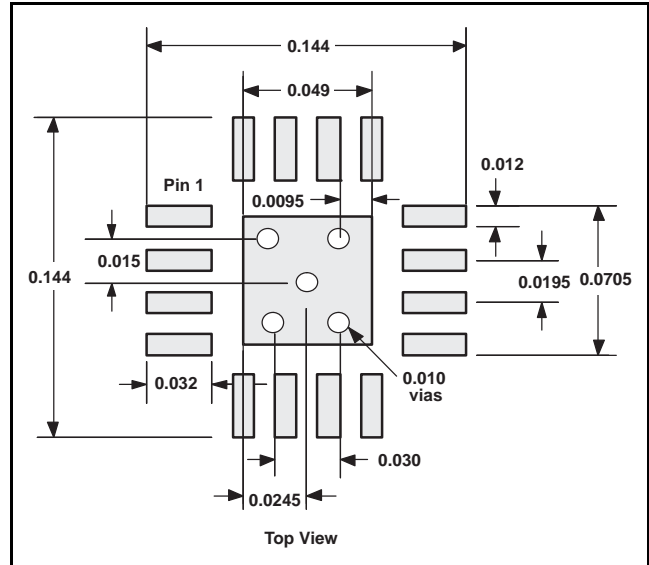


Figure 92. QFN Etch and Via Pattern



THS4509 EVM

Figure 93 is the THS4509 EVAL1 EVM schematic; layers 1 through 4 of the PCB are shown Figure 94, and Table 4 is the bill of material for the EVM as supplied from TI.

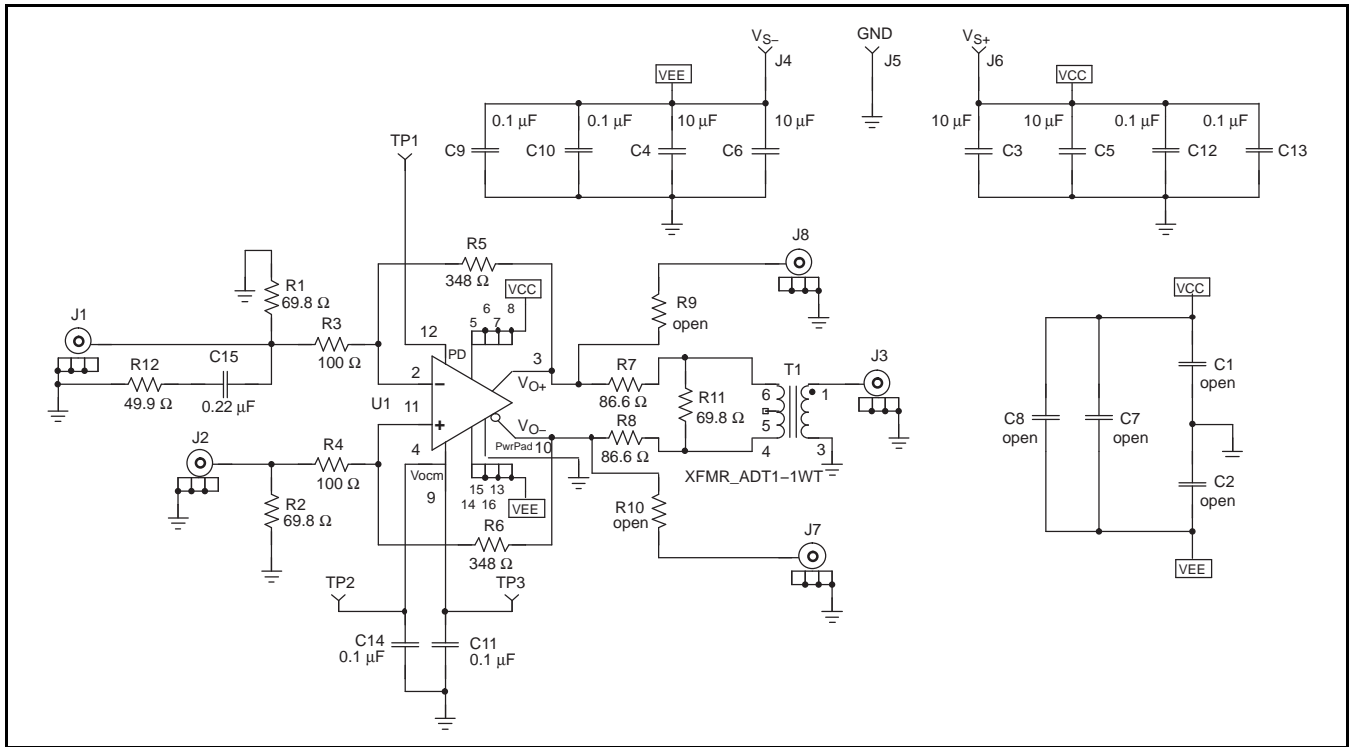


Figure 93. THS4509 EVAL1 EVM Schematic

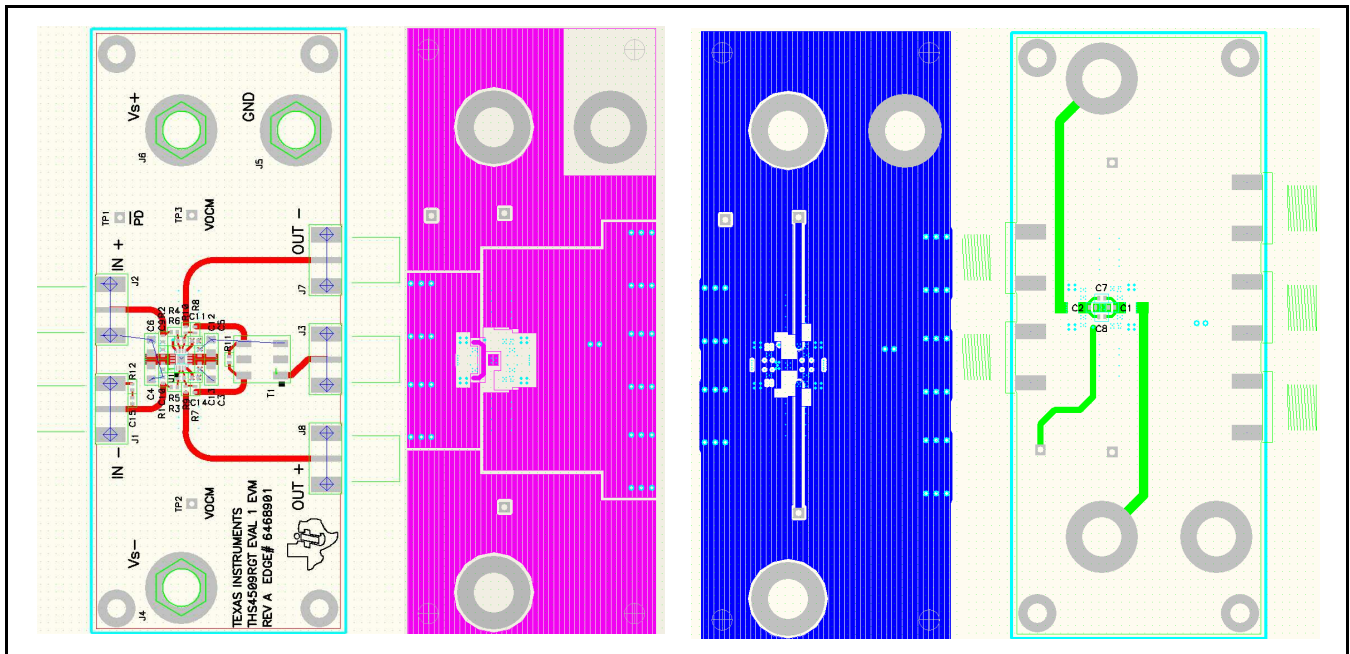


Figure 94. THS4509 EVAL1 EVM Layer 1 through Layer 4

**Table 4. THS4509 EVAL1 EVM Bill of Materials**

ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	PCB QTY	MANUFACTURER PART NUMBER
1	CAP, 10.0 $\mu$ F, Ceramic, X5R, 6.3 V	0805	C3, C4, C5, C6	4	(AVX) 08056D106KAT2A
2	CAP, 0.1 $\mu$ F, Ceramic, X5R, 10 V	0402	C9, C10, C11, C12, C13, C14	6	(AVX) 0402ZD104KAT2A
3	CAP, 0.22 $\mu$ F, Ceramic, X5R, 6.3 V	0402	C15	1	(AVX) 04026D224KAT2A
4	OPEN	0402	C1, C2, C7, C8	4	
5	OPEN	0402	R9, R10	2	
6	Resistor, 49.9 $\Omega$ , 1/16 W, 1%	0402	R12	1	(KOA) RK73H1ETTP49R9F
8	Resistor, 69.8 $\Omega$ , 1/16 W, 1%	0402	R1, R2, R11	3	(KOA) RK73H1ETTP69R8F
9	Resistor, 86.6 $\Omega$ , 1/16 W, 1%	0402	R7, R8	2	(KOA) RK73H1ETTP86R6F
10	Resistor, 100 $\Omega$ , 1/16 W, 1%	0402	R3, R4	2	(KOA) RK73H1ETTP1000F
11	Resistor, 348 $\Omega$ , 1/16 W, 1%	0402	R5, R6	2	(KOA) RK73H1ETTP3480F
12	Transformer, RF		T1	1	(MINI-CIRCUITS) ADT1-1WT
13	Jack, banana receptance, 0.25" diameter hole		J4, J5, J6	3	(HH SMITH) 101
14	OPEN		J1, J7, J8	3	
15	Connector, edge, SMA PCB Jack		J2, J3	2	(JOHNSON) 142-0701-801
16	Test point, Red		TP1, TP2, TP3	3	(KEYSTONE) 5000
17	IC, THS4509		U1	1	(TI) THS4509RGT
18	Standoff, 4-40 HEX, 0.625" length			4	(KEYSTONE) 1808
19	SCREW, PHILLIPS, 4-40, 0.250"			4	SHR-0440-016-SN
20	Printed circuit board			1	(TI) EDGE# 6468901

## EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input and output voltage ranges as specified in the table provided below.

Input Range, $V_{S+}$ to $V_{S-}$	<b>3.0 V to 6.0 V</b>
Input Range, $V_I$	3.0 V to 6.0 V NOT TO EXCEED $V_{S+}$ or $V_{S-}$
Output Range, $V_O$	3.0 V to 6.0 V NOT TO EXCEED $V_{S+}$ or $V_{S-}$

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the product data sheet or EVM user's guide (if user's guide is available) prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +30°C. The EVM is designed to operate properly with certain components above +50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the material provided. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments Post Office Box 655303 Dallas, Texas 75265



## Revision History

Changes from Revision F (October 2007) to Revision G	Page
• Updated document format .....	1
• Changed common-mode range column for THS4509 and THS4513 rows in <a href="#">NoLabel</a> table.....	1
• Added footnote 1 to <a href="#">Absolute Maximum Ratings</a> table.....	2
• Added V (volts) to unit column of ESD ratings rows in <a href="#">Absolute Maximum Ratings</a> table.....	2
• Changed $V_{S+} - V_{S-} = 5\text{ V}$ <i>Input</i> specifications from 1.75 V typ (common-mode input range high) to 1.4 V typ; –1.75 V (common-mode input range low) to –1.4 V; 1.35 M $\Omega$    1.77 pF (differential input impedance) to 1.3 M $\Omega$    1.8 pF; 1.02 M $\Omega$    2.26 pF (common-mode input impedance) to 1.0 M $\Omega$    2.3 pF.....	4
• Changed $V_{S+} - V_{S-} = 3\text{ V}$ <i>Input</i> specifications from 0.75 V typ (common-mode input range high) to 0.4 V typ; –0.75 V (common-mode input range low) to –0.4 V; 1.35 M $\Omega$    1.77 pF (differential input impedance) to 1.3 M $\Omega$    1.8 pF; 1.02 M $\Omega$    2.26 pF (common-mode input impedance) to 1.0 M $\Omega$    2.3 pF.....	6

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
THS4509RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS4509RGTRG4	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS4509RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS4509RGTTG4	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4509RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THS4509RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**

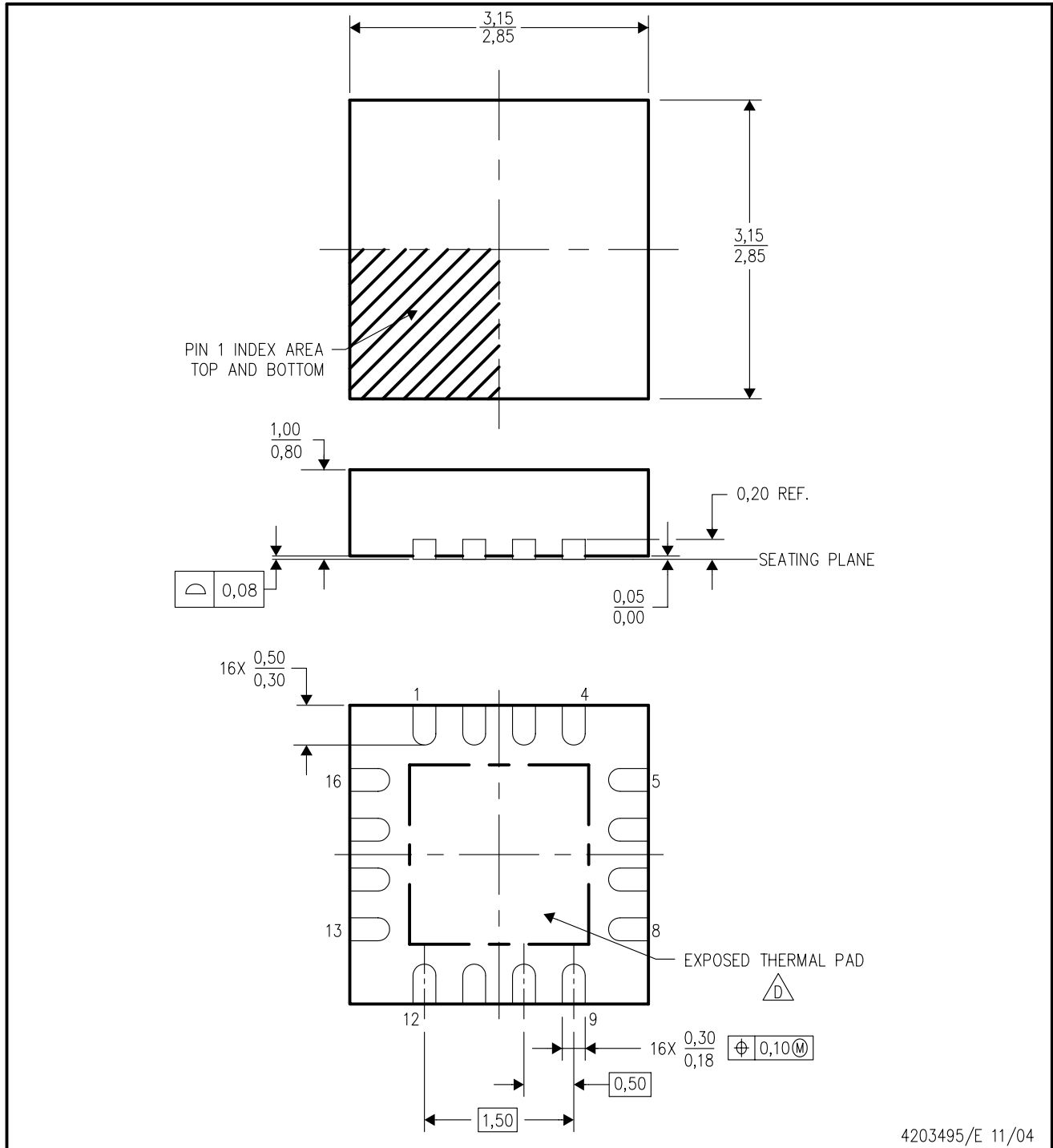


\*All dimensions are nominal


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4509RGTR	QFN	RGT	16	3000	346.0	346.0	29.0
THS4509RGTT	QFN	RGT	16	250	190.5	212.7	31.8

RGT (S-PQFP-N16)

PLASTIC QUAD FLATPACK



4203495/E 11/04

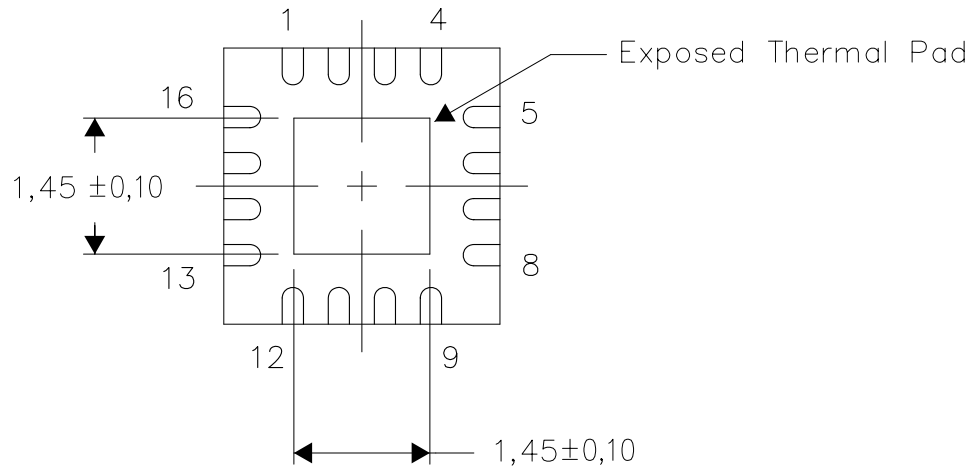
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-leads (QFN) package configuration.
  -  D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Falls within JEDEC MO-220.

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

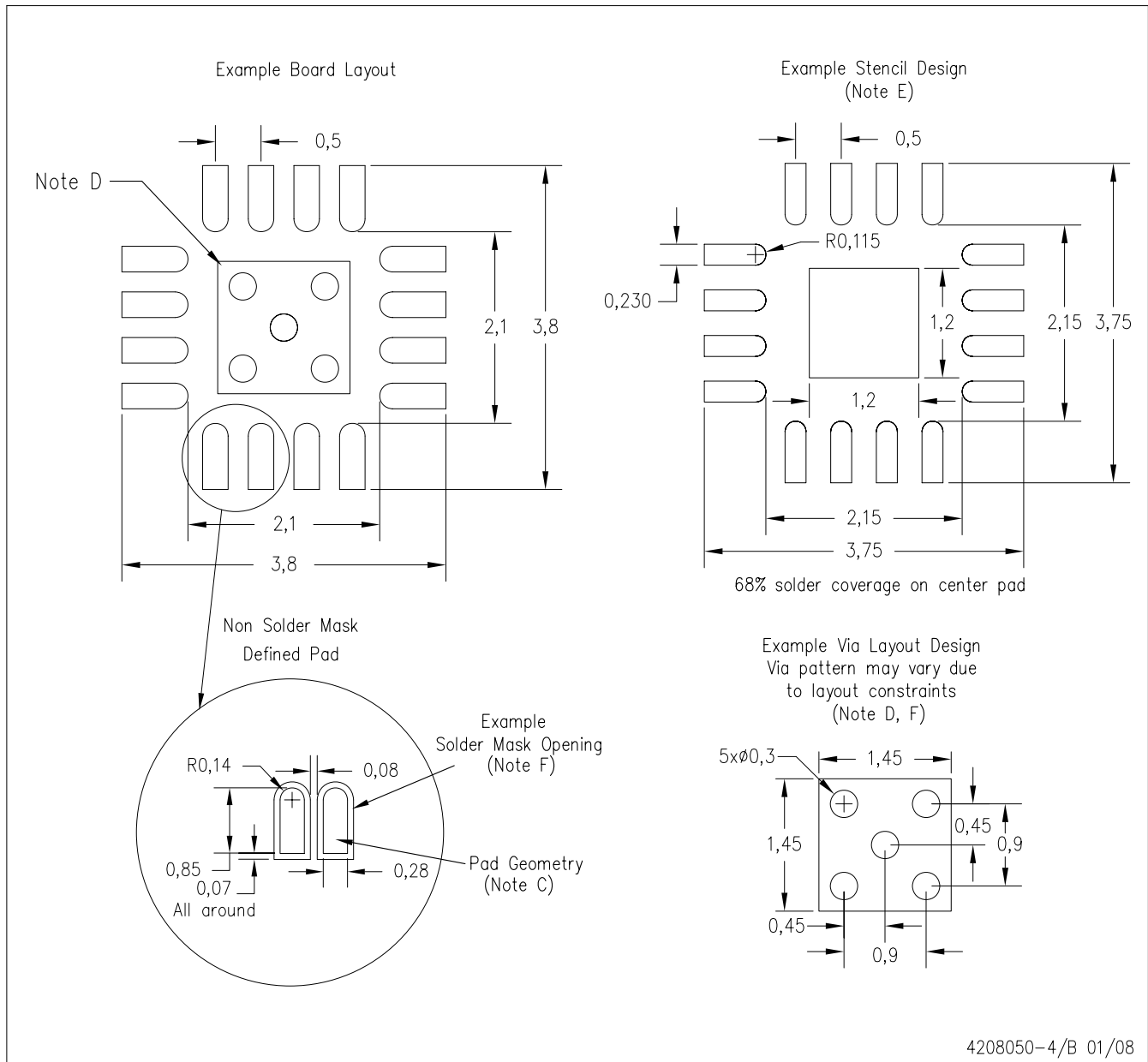


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGT (S-PQFP-N16)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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