LOW INPUT VOLTAGE, ULTRA-LOW r_{ON} LOAD SWITCH WITH CONFIGURABLE ENABLE LOGIC AND CONTROLLED SLEW-RATE

Check for Samples: TPS22932B

FEATURES

- **Input Voltage: 1.1 V to 3.6 V**
- **Ultra-Low ON Resistance**
  - **r_{ON} = 55 mΩ at V_{IN} = 3.6 V**
  - **r_{ON} = 65 mΩ at V_{IN} = 2.5 V**
  - **r_{ON} = 75 mΩ at V_{IN} = 1.8 V**
  - **r_{ON} = 115 mΩ at V_{IN} = 1.2 V**
- **500-mA Maximum Continuous Switch Current**
- **Quiescent Current < 1 µA**
- **Shutdown Current < 1 µA**
- **Low Control Threshold Allows Use of 1.2-V/1.8-V/2.5-V/3.3-V Logic**
- **Configurable Enable Logic**
- **Controlled Slew Rate to Avoid Inrush Currents: 165 µs at 1.8 V**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Six-Terminal Wafer-Chip-Scale Package (WCSP)**
  - **0.8 mm × 1.2 mm, 0.4-mm Pitch, 0.5-mm Height**

APPLICATIONS

- **PDAs**
- **Cell Phones**
- **GPS Devices**
- **MP3 Players**
- **Digital Cameras**
- **Peripheral Ports**
- **Portable Instrumentation**

DESCRIPTION

TPS22932B is a low r_{ON} load switch with controlled turn on. It contains an ultra-low r_{ON} P-channel MOSFET that can operate over an input voltage range of 1.1 V to 3.6 V.

The switch is controlled by eight patterns of 3-bit input. The user can choose the logic functions MUX, AND, OR, NAND, NOR, inverter, and non-inverter. All inputs can be connected to V_{IN} or GND. The control pins can be connected to low voltage GPIOs allowing it to be controlled by whatever 1.2-V, 1.8-V, 2.5-V, or 3.3-V logic signals while keeping extremely low quiescent current.

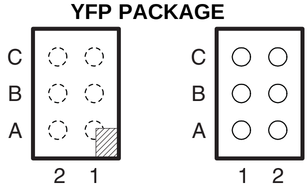
A 120-Ω on-chip load resistor is available for output quick discharge when the switch is turned off. The rise time (slew rate) of the device is internally controlled to avoid inrush current: the rise time of TPS22932B is 165 µs.

TPS22932B is available in a space-saving 6-terminal WCSP (YFP with 0.4-mm pitch). The device is characterized for operation over the free-air temperature range of –40°C to 85°C.

DEVICE	r_{ON} AT 1.8 V (TYP)	SLEW RATE (TYP AT 3.3 V)	QUICK OUTPUT DISCHARGE (1)	MAX OUTPUT CURRENT	ENABLE
TPS22932B	75 mΩ	165 µs	Yes	500 mA	Active high

(1) This feature discharges the output of the switch to ground through a 120-Ω resistor, preventing the output from floating.

YFP PACKAGE



Laser Marking View   Bump View

Table 1. TERMINAL ASSIGNMENTS

C	ON2	ON3
B	ON1	GND
A	V_{IN}	V_{OUT}
	2	**1**

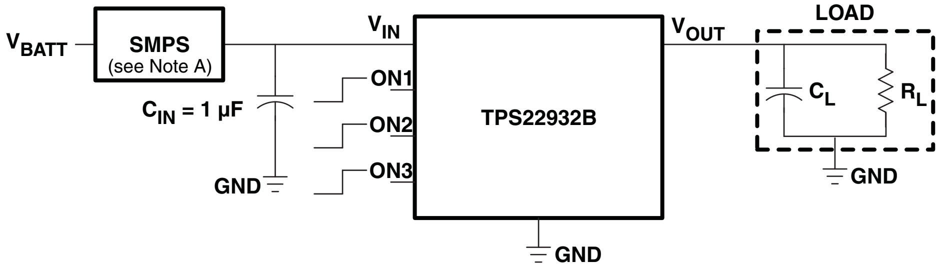
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION

T_A	PACKAGE (1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING (3)
–40°C to 85°C	WCSP – YFP (0.4-mm pitch)	Tape and reel	TPS22932BYFPR	_ _ 48_

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(3) The actual top-side marking has two preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

TYPICAL APPLICATION



A. Switched mode power supply

APPLICATION BLOCK DIAGRAM

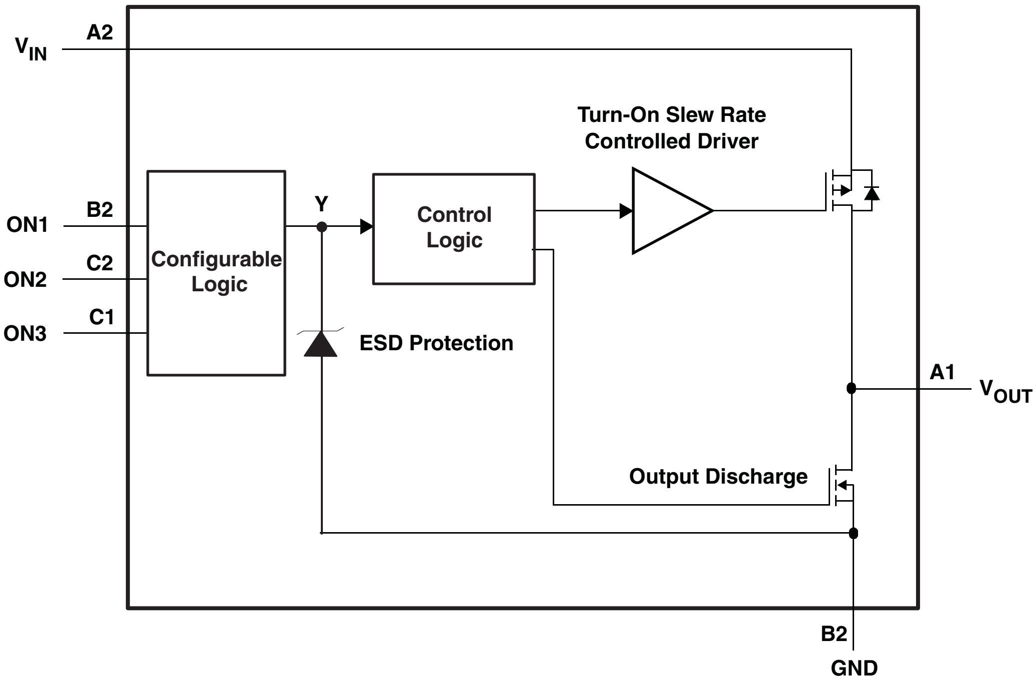


Table 2. CONFIGURABLE LOGIC FUNCTION TABLE

INPUTS			SWITCH CONTROL
ON3	ON2	ON1	Y
L	L	L	OFF
L	L	H	OFF
L	H	L	ON
L	H	H	ON
H	L	L	OFF
H	L	H	ON
H	H	L	OFF
H	H	H	ON

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NO.	NAME	
A1	V_{OUT}	Switch output
A2	V_{IN}	Switch input, bypass this input with a ceramic capacitor to ground
B1	GND	Ground
B2, C2, C1	ON1, ON2, ON3	Switch control input, active high - Do not leave floating

LOGIC DIAGRAM (POSITIVE LOGIC)

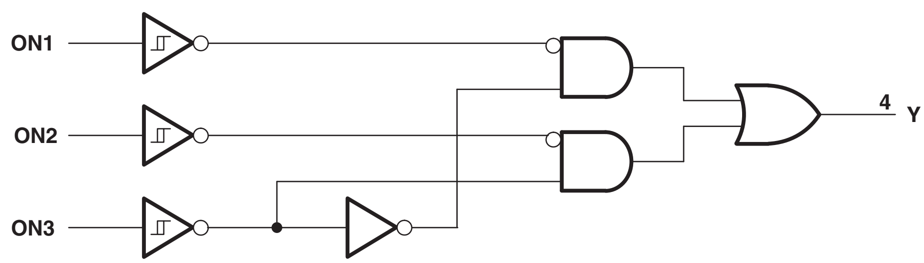


Table 3. FUNCTION SELECTION TABLE

LOGIC FUNCTION	FIGURE NO.
2-to-1 data selector	Figure 1
2-input AND gate	Figure 2
2-input OR gate with one inverted input	Figure 3
2-input NAND gate with one inverted input	Figure 3
2-input AND gate with one inverted input	Figure 4
2-input NOR gate with one inverted input	Figure 4
2-input OR gate	Figure 5
Inverter	Figure 6
Noninverted buffer	Figure 7

LOGIC CONFIGURATIONS

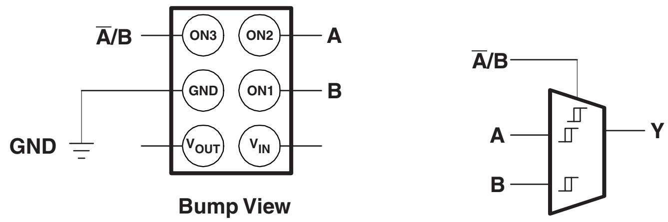


Figure 1. 2-to-1 Data Selector

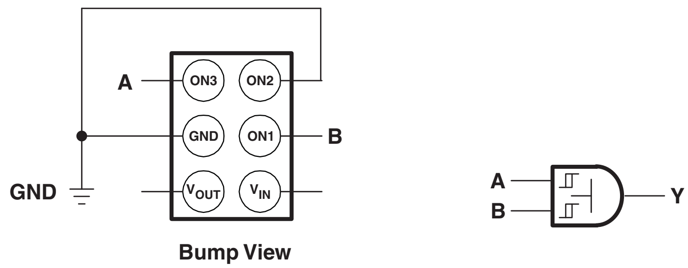


Figure 2. 2-Input AND Gate

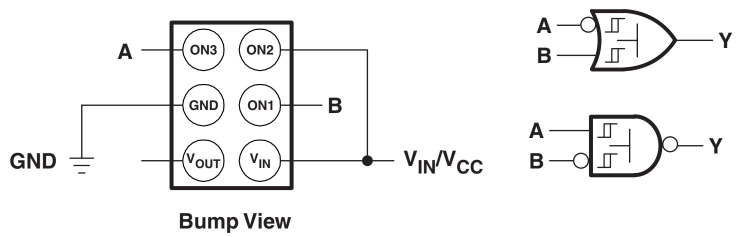


Figure 3. 2-Input OR Gate With One Inverted Input
2-Input NAND Gate With One Inverted Input

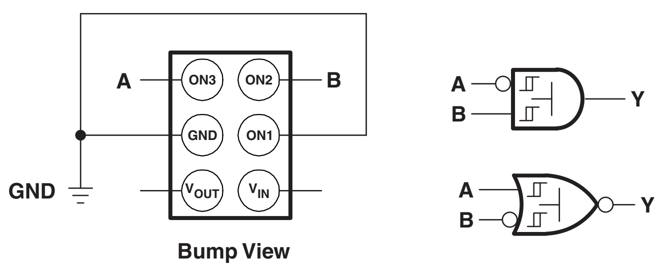


Figure 4. 2-Input AND Gate With One Inverted Input
2-Input NOR Gate With One Inverted Input

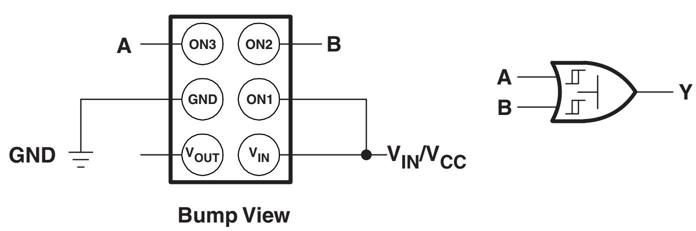


Figure 5. 2-Input OR Gate

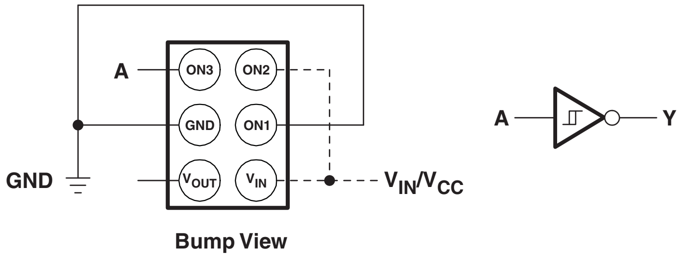


Figure 6. Inverter

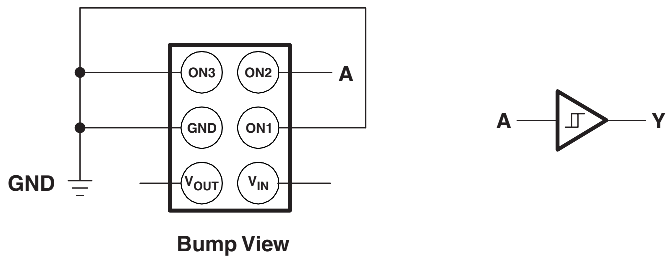


Figure 7. Noninverted Buffer

ABSOLUTE MAXIMUM RATINGS(1)

			MIN	MAX	UNIT
V_{IN}	Input voltage range		–0.3	4	V
V_{OUT}	Output voltage range			V_{IN} + 0.3	V
P	Power dissipation at T_A = 25°C			0.8	W
I_{MAX}	Maximum continuous switch current			500	mA
T_A	Operating free-air temperature range		–40	85	°C
T_{stg}	Storage temperature range		–65	150	°C
T_{lead}	Maximum lead temperature (10-s soldering time)			300	°C
ESD	Electrostatic discharge protection	Human-Body Model (HBM)		2000	V
		Charged Device Model (CDM)		1000	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL IMPEDANCE RATINGS

			TYP	UNIT
θ_{JA}	Package thermal impedance(1)	YFP package	155	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
I_{OUT}	Output current		500	mA
V_{IN}	Input voltage range	1.1	3.6	V
V_{OUT}	Output voltage range		V_{IN}	
C_{IN}	Input capacitor	1(1)		µF

(1) See *Application Information*.

ELECTRICAL CHARACTERISTICS

V_{IN} = 1.1 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP (1)	MAX	UNIT
I_{IN}	Quiescent current	I_{OUT} = 0	V_{IN} = 1.1 V	Full		140	275	nA
			V_{IN} = 1.8 V			280	500	
			V_{IN} = 3.6 V			860	920	
$I_{IN(OFF)}$	OFF-state supply current	V_{ON} = GND, OUT = Open	V_{IN} = 1.1 V	Full		80	225	nA
			V_{IN} = 1.8 V			125	300	
			V_{IN} = 3.6 V			340	650	
$I_{IN(LEAKAGE)}$	OFF-state switch current	V_{ON} = GND, V_{OUT} = 0	V_{IN} = 1.1 V	Full		80	225	nA
			V_{IN} = 1.8 V			125	300	
			V_{IN} = 3.6 V			340	650	
r_{ON}	ON-state resistance	I_{OUT} = –200 mA	V_{IN} = 3.6 V	25°C		55	70	mΩ
				Full			85	
			V_{IN} = 2.5 V	25°C		65	80	
				Full			100	
			V_{IN} = 1.8 V	25°C		75	90	
				Full			110	
			V_{IN} = 1.2 V	25°C		115	130	
				Full			155	
			V_{IN} = 1.1 V	25°C		135	150	
				Full			170	
r_{PD}	Output pulldown resistance	V_{IN} = 3.3 V, V_{ON} = 0, I_{OUT} = 30 mA		25°C		75	120	Ω
I_{ON}	ON-state input leakage current	V_{ON} = 1.1 V to 3.6 V or GND		Full			1	µA
Control Inputs (ON1, ON2, ON3)								
	Input leakage current	V_{IN} = 1.1 V to 3.6 V or GND		Full			1	µA
V_{ON}	Control input voltage			Full			3.6	V
V_{T+}	Positive-going input voltage threshold	V_{IN} = 1.1 V to 1.8 V		Full	0.5		0.8	V
		V_{IN} = 1.8 V to 3.6 V			0.6		0.9	
V_{T-}	Negative-going input voltage threshold	V_{IN} = 1.1 V to 1.8 V		Full	0.2		0.6	V
		V_{IN} = 1.8 V to 3.6 V			0.3		0.7	
ΔV_T	Hysteresis (V_{T+} – V_{T-})	V_{IN} = 1.1 V to 3.6 V		Full	0.2		0.6	V

(1) Typical values are at the specified V_{IN} and T_A = 25°C.

SWITCHING CHARACTERISTICS

V_{IN} = 1.2 V, R_{L_CHIP} = 120 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turn-ON time	R_L = 500 Ω	C_L = 0.1 µF		350		µs
			C_L = 1 µF		390		
			C_L = 3 µF		450		
t_{OFF}	Turn-OFF time	R_L = 500 Ω	C_L = 0.1 µF		30		µs
			C_L = 1 µF		70		
			C_L = 3 µF		160		
t_r	V_{OUT} rise time	R_L = 500 Ω	C_L = 0.1 µF		240		µs
			C_L = 1 µF		240		
			C_L = 3 µF		260		
t_f	V_{OUT} fall time	R_L = 500 Ω	C_L = 0.1 µF		20		µs
			C_L = 1 µF		150		
			C_L = 3 µF		450		

SWITCHING CHARACTERISTICS

V_{IN} = 1.5 V, R_{L_CHIP} = 120 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turn-ON time	R_L = 500 Ω	C_L = 0.1 µF		290		µs
			C_L = 1 µF		320		
			C_L = 3 µF		350		
t_{OFF}	Turn-OFF time	R_L = 500 Ω	C_L = 0.1 µF		30		µs
			C_L = 1 µF		70		
			C_L = 3 µF		150		
t_r	V_{OUT} rise time	R_L = 500 Ω	C_L = 0.1 µF		205		µs
			C_L = 1 µF		205		
			C_L = 3 µF		220		
t_f	V_{OUT} fall time	R_L = 500 Ω	C_L = 0.1 µF		18		µs
			C_L = 1 µF		145		
			C_L = 3 µF		445		

SWITCHING CHARACTERISTICS

V_{IN} = 1.8 V, R_{L_CHIP} = 120 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turn-ON time	R_L = 500 Ω	C_L = 0.1 µF		215		µs
			C_L = 1 µF		240		
			C_L = 3 µF		260		
t_{OFF}	Turn-OFF time	R_L = 500 Ω	C_L = 0.1 µF		24		µs
			C_L = 1 µF		60		
			C_L = 3 µF		142		
t_r	V_{OUT} rise time	R_L = 500	C_L = 0.1 µF		165		µs
			C_L = 1 µF		165		
			C_L = 3 µF		175		
t_f	V_{OUT} fall time	R_L = 500 Ω	C_L = 0.1 µF		18		µs
			C_L = 1 µF		145		
			C_L = 3 µF		440		

SWITCHING CHARACTERISTICS

V_{IN} = 2.5 V, R_{L_CHIP} = 120 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turn-ON time	R_L = 500 Ω	C_L = 0.1 µF		185		µs
			C_L = 1 µF		205		
			C_L = 3 µF		225		
t_{OFF}	Turn-OFF time	R_L = 500 Ω	C_L = 0.1 µF		2		µs
			C_L = 1 µF		60		
			C_L = 3 µF		140		
t_r	V_{OUT} rise time	R_L = 500 Ω	C_L = 0.1 µF		145		µs
			C_L = 1 µF		150		
			C_L = 3 µF		160		
t_f	V_{OUT} fall time	R_L = 500 Ω	C_L = 0.1 µF		18		µs
			C_L = 1 µF		147		
			C_L = 3 µF		445		

SWITCHING CHARACTERISTICS

V_{IN} = 3 V, R_{L_CHIP} = 120 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turn-ON time	R_L = 500 Ω	C_L = 0.1 µF		170		µs
			C_L = 1 µF		190		
			C_L = 3 µF		210		
t_{OFF}	Turn-OFF time	R_L = 500 Ω	C_L = 0.1 µF		2		µs
			C_L = 1 µF		60		
			C_L = 3 µF		140		
t_r	V_{OUT} rise time	R_L = 500 Ω	C_L = 0.1 µF		140		µs
			C_L = 1 µF		140		
			C_L = 3 µF		150		
t_f	V_{OUT} fall time	R_L = 500 Ω	C_L = 0.1 µF		17		µs
			C_L = 1 µF		148		
			C_L = 3 µF		450		

SWITCHING CHARACTERISTICS

V_{IN} = 3.3 V, R_{L_CHIP} = 120 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turn-ON time	R_L = 500 Ω	C_L = 0.1 µF		160		µs
			C_L = 1 µF		175		
			C_L = 3 µF		195		
t_{OFF}	Turn-OFF time	R_L = 500 Ω	C_L = 0.1 µF		20		µs
			C_L = 1 µF		55		
			C_L = 3 µF		135		
t_r	V_{OUT} rise time	R_L = 500 Ω	C_L = 0.1 µF		135		µs
			C_L = 1 µF		135		
			C_L = 3 µF		145		
t_f	V_{OUT} fall time	R_L = 500 Ω	C_L = 0.1 µF		17		µs
			C_L = 1 µF		148		
			C_L = 3 µF		450		

TYPICAL CHARACTERISTICS

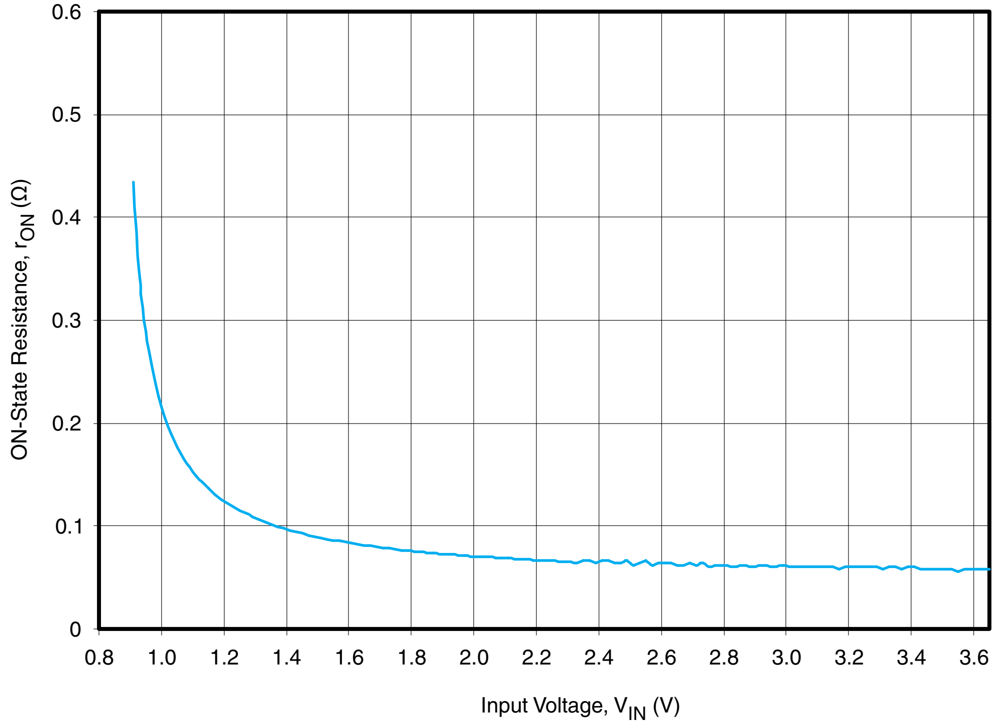


Figure 8. r_{ON} **vs** V_{IN}

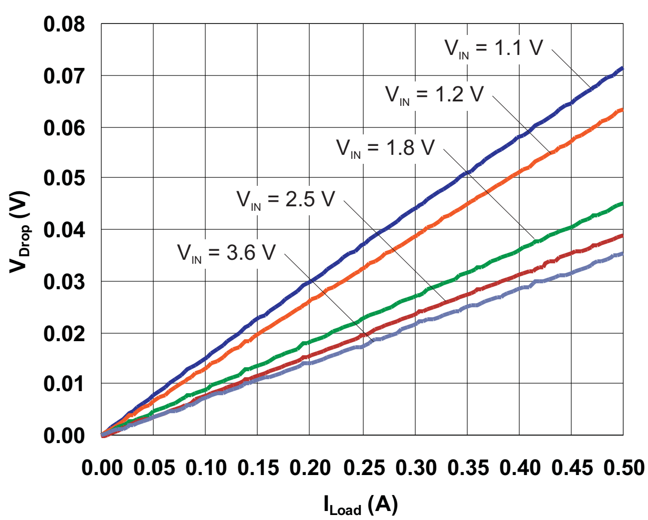


Figure 9. Voltage Drop vs Load Current

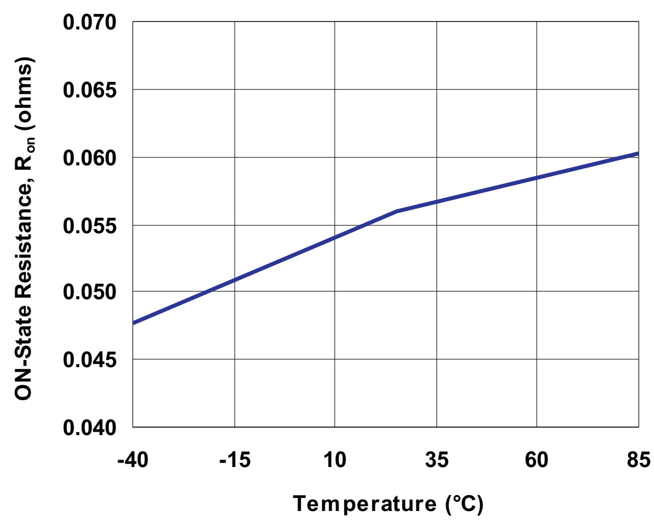


Figure 10. r_{ON} **vs** T_A **(**V_{IN} **= 3.3 V)**

TYPICAL CHARACTERISTICS (continued)

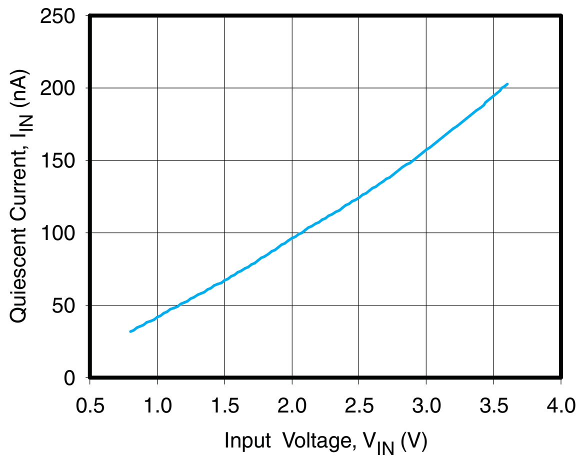


Figure 11. Quiescent Current vs V_{IN} ($ON2 = V_{IN}$, ON1–ON3 = 0 V, I_{out}= 0)

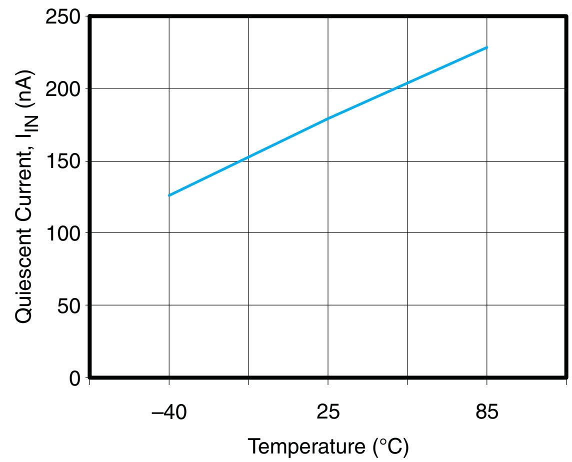


Figure 12. Quiescent Current vs T_A (V_{IN} = 3.3 V, ON2 = V_{IN}, ON1–ON3 = 0 V, I_{out} = 0)

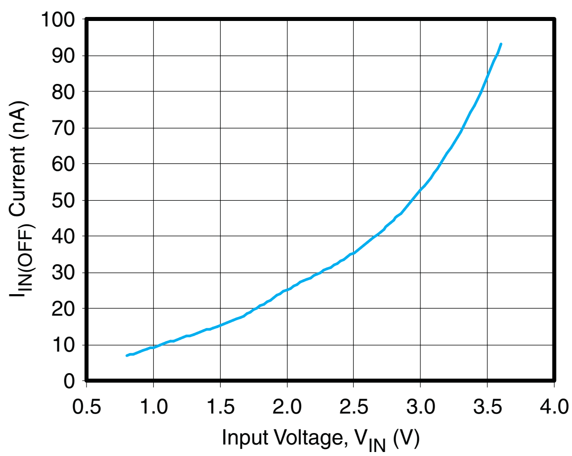


Figure 13. $I_{IN(OFF)}$ vs V_{IN} (ON1–ON2–ON3 = 0 V)

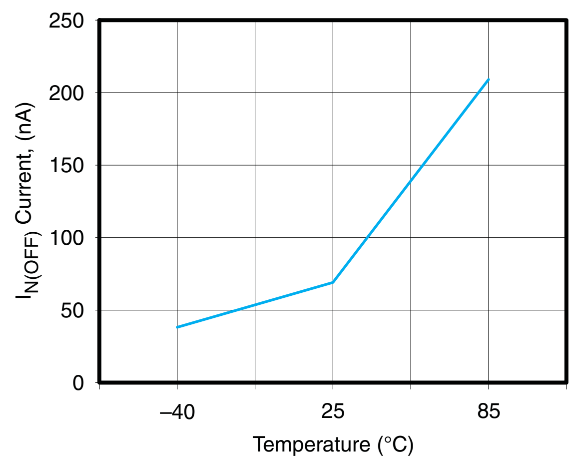


Figure 14. $I_{IN(OFF)}$ vs Temperature (V_{IN} = 3.3 V, ON1–ON2–ON3 = 0 V)

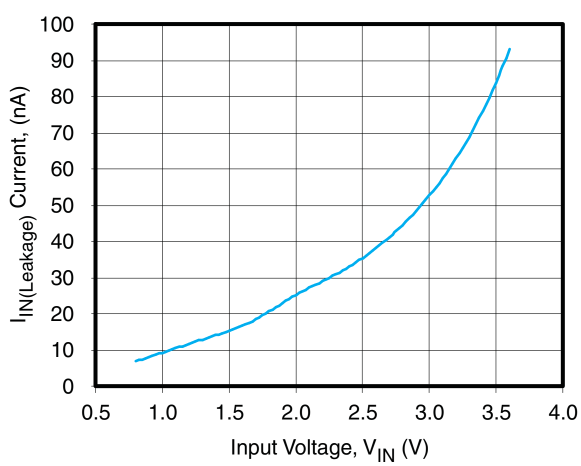


Figure 15. $I_{IN(Leakage)}$ vs V_{IN} (ON1–ON2–ON3 = 0 V, V_{out} = 0)

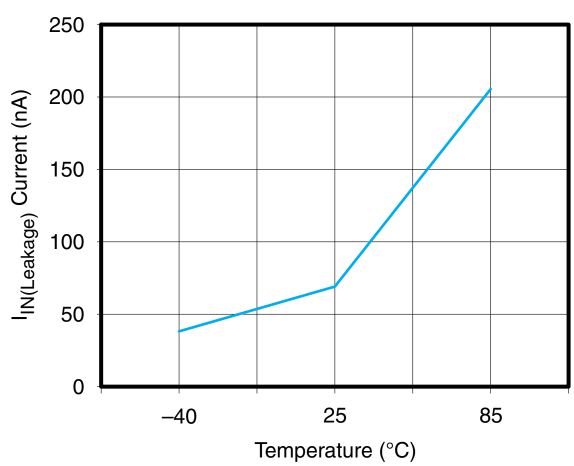


Figure 16. $I_{IN(Leakage)}$ vs Temperature (V_{IN} = 3.3 V, ON1–ON2–ON3 = 0 V)

TYPICAL CHARACTERISTICS (continued)

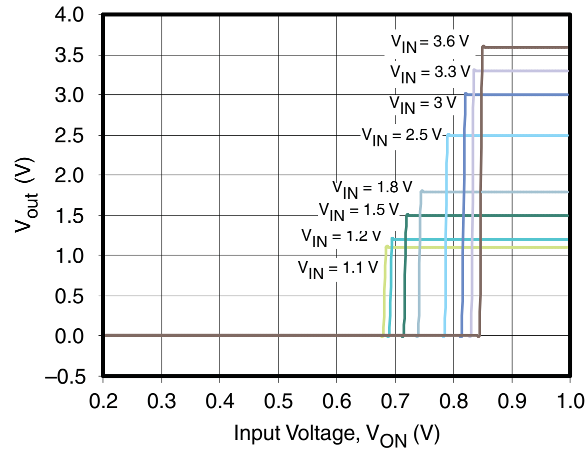


Figure 17. ON-Input Threshold

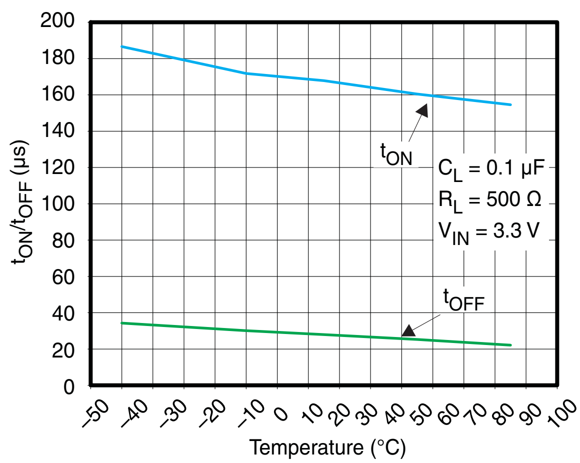


Figure 18. t_{ON}/t_{OFF} vs Temperature

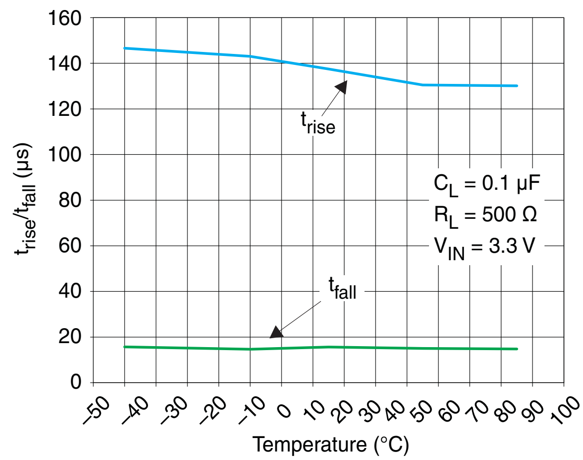


Figure 19. t_{rise}/t_{fall} vs Temperature

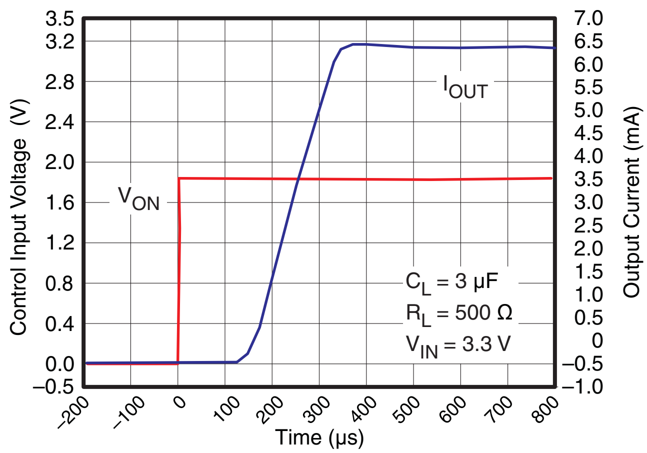


Figure 20. t_{ON} Response

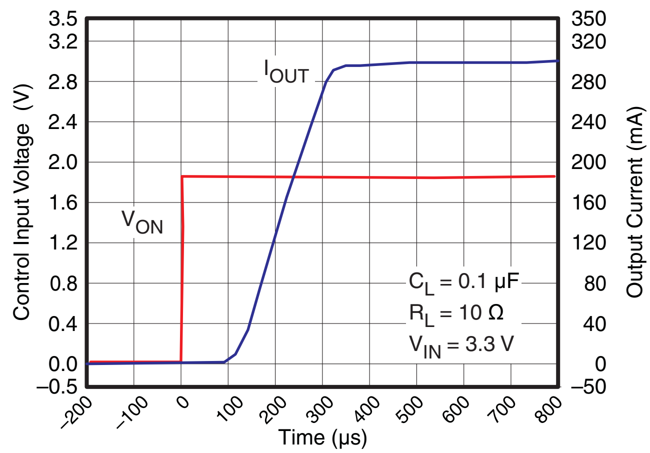


Figure 21. t_{ON} Response

TYPICAL CHARACTERISTICS (continued)

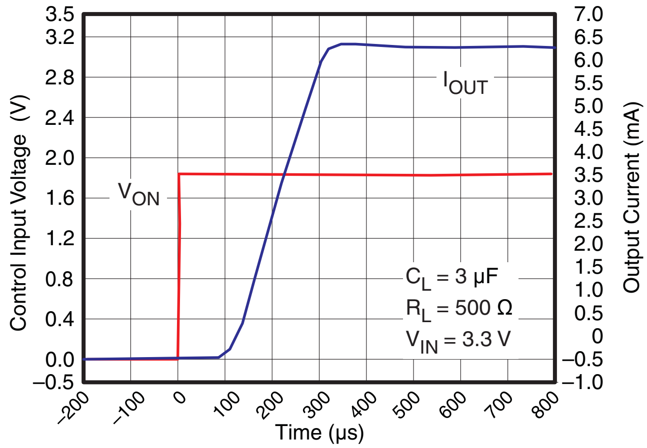


Figure 22. t_{ON} Response

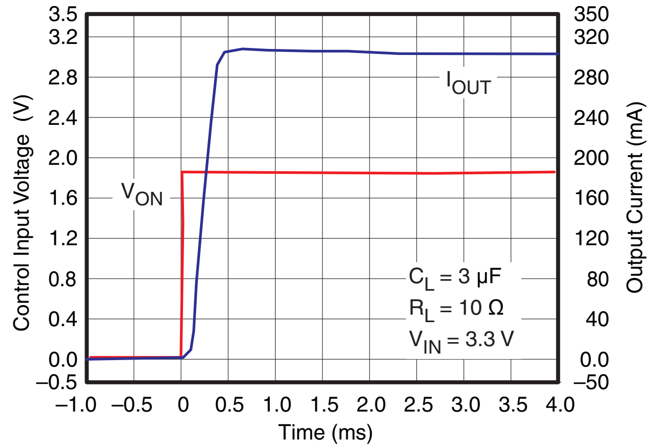


Figure 23. t_{ON} Response

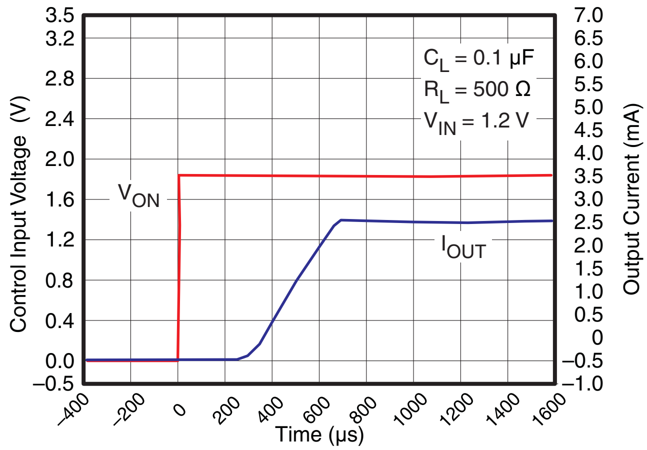


Figure 24. t_{ON} Response

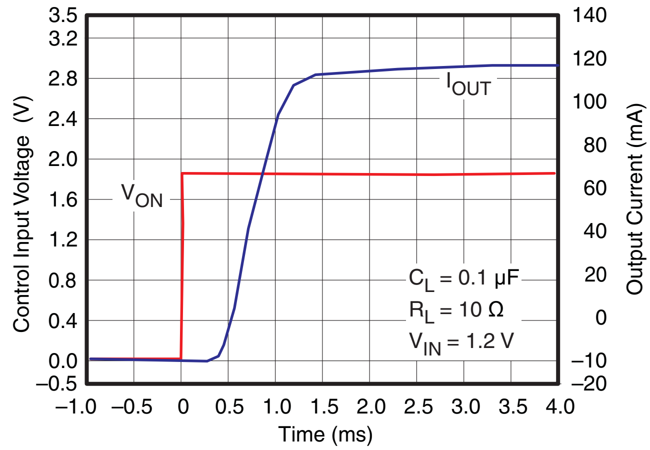


Figure 25. t_{ON} Response

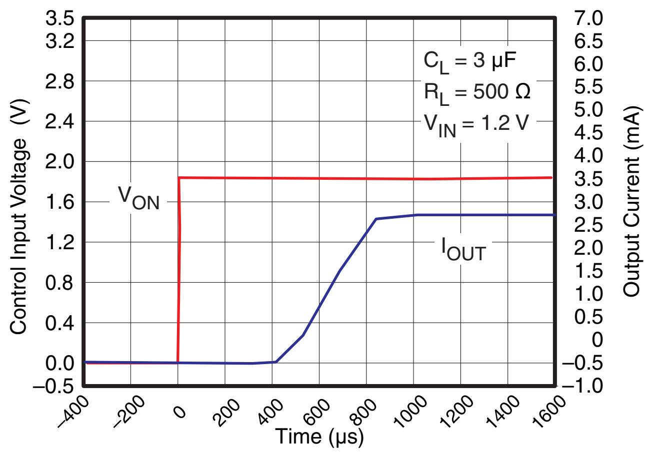


Figure 26. t_{ON} Response

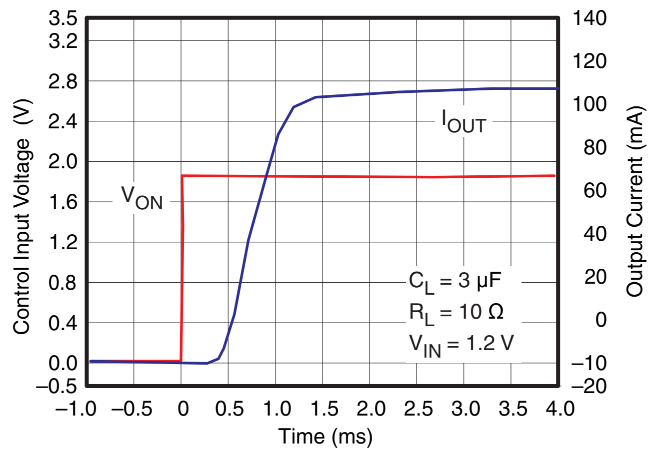


Figure 27. t_{ON} Response

TYPICAL CHARACTERISTICS (continued)

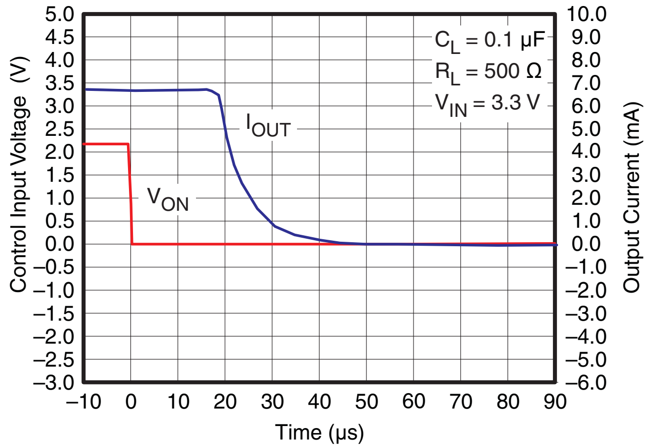


Figure 28. t_{OFF} Response

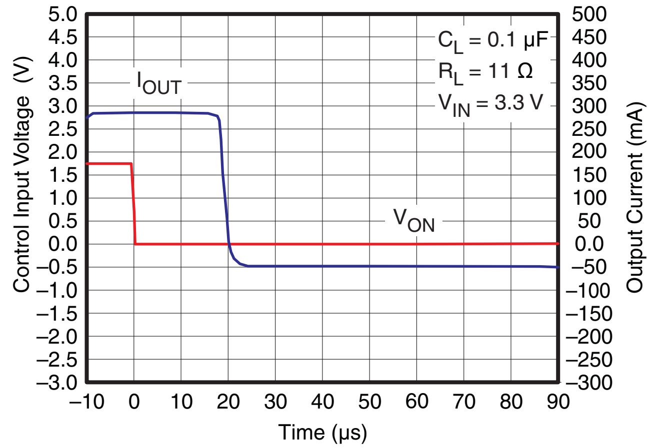


Figure 29. t_{OFF} Response

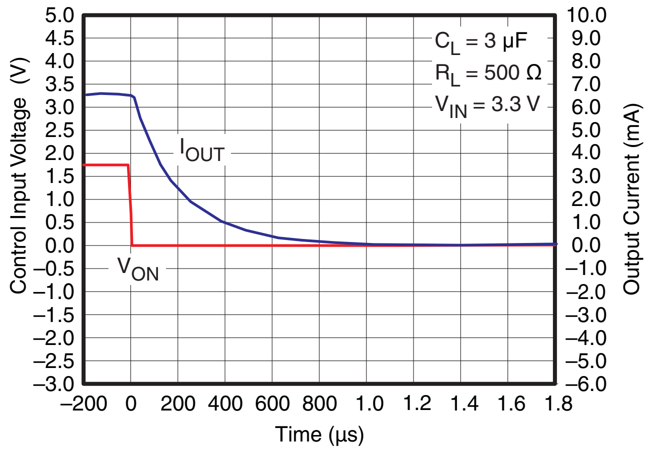


Figure 30. t_{OFF} Response

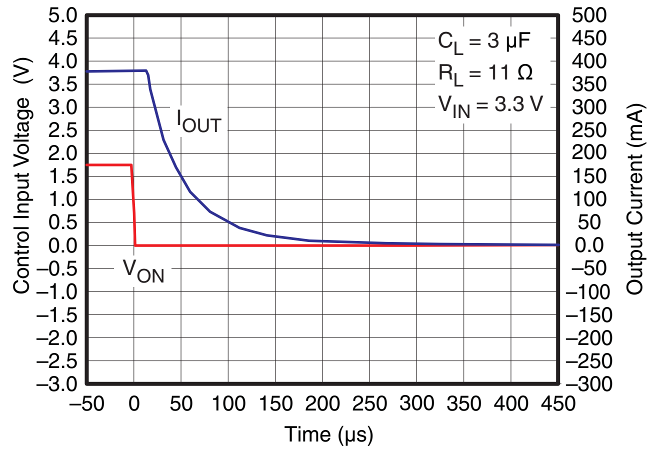


Figure 31. t_{OFF} Response

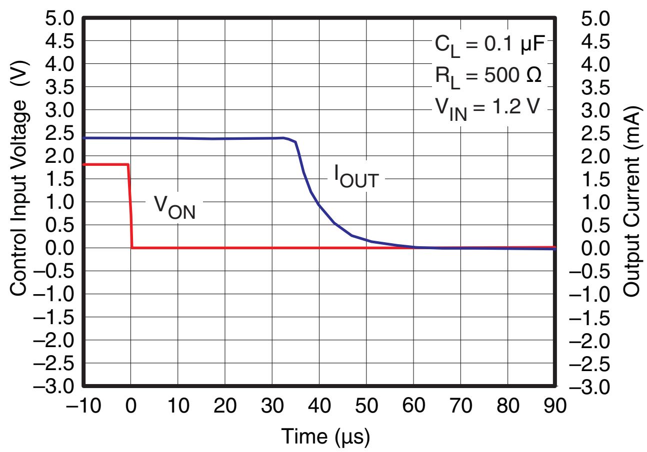


Figure 32. t_{OFF} Response

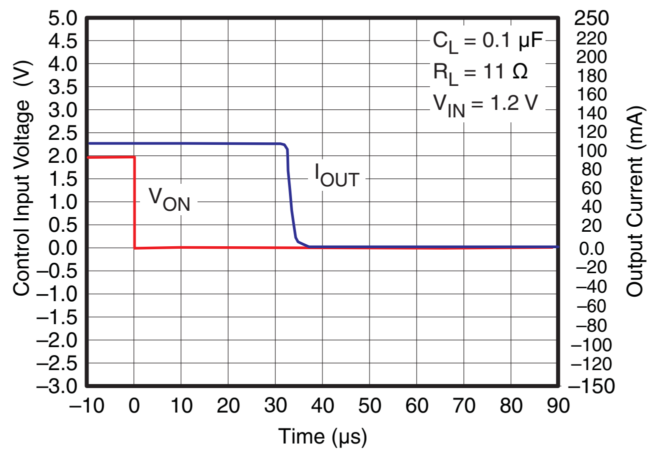


Figure 33. t_{OFF} Response

TYPICAL CHARACTERISTICS (continued)

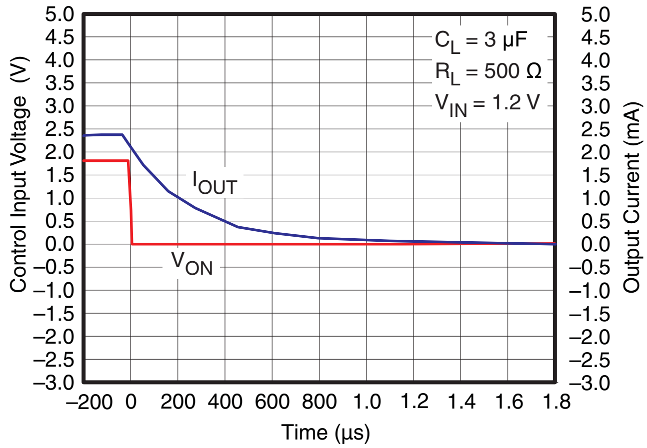


Figure 34. t_{OFF} Response

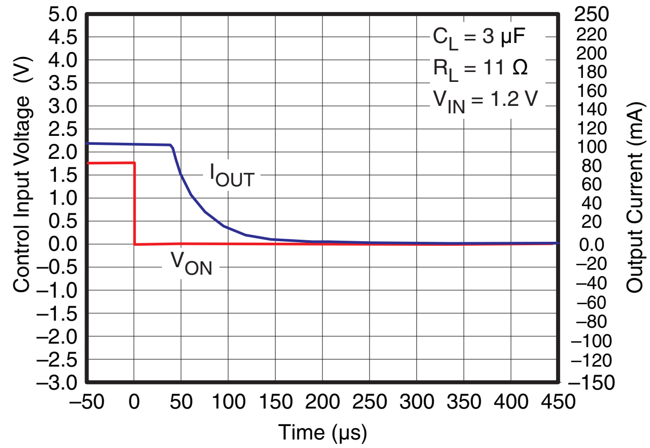
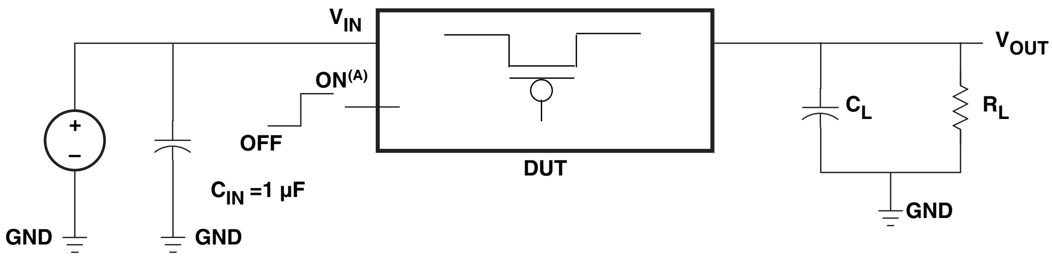
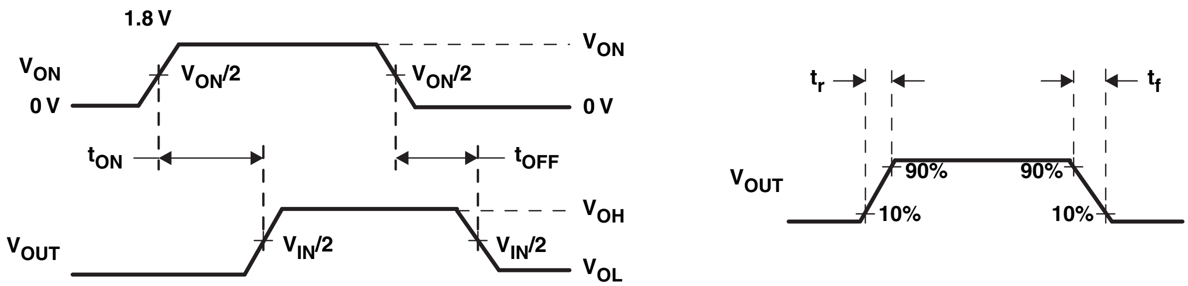


Figure 35. t_{OFF} Response

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



t_{ON}/t_{OFF} WAVEFORMS

A. t_{rise} and t_{fall} of the control signal is 100 ns.

Figure 36. Test Circuit and t_{ON}/t_{OFF} Waveforms

APPLICATION INFORMATION

ON/OFF Control

The ON pin controls the state of the switch. Activating ON continuously holds the switch in the on state so long as there is no fault. ON is active HI and has a low threshold making it capable of interfacing with low voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V or 3.3-V GPIOs.

Input Capacitor

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor must be placed between V_{IN} and GND . A 1-µF ceramic capacitor, C_{IN}, placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during higher current application. When switching a heavy load, it is recommended to have an input capacitor about 10 or more times higher than the output capacitor in order to avoid any supply drop.

Output Capacitor

Due to the integral body diode in the PMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}.

Board Layout

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for V_{IN}, V_{OUT}, and GND will help minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS22932BYFPR	ACTIVE	DSBGA	YFP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS22932BYFPT	ACTIVE	DSBGA	YFP	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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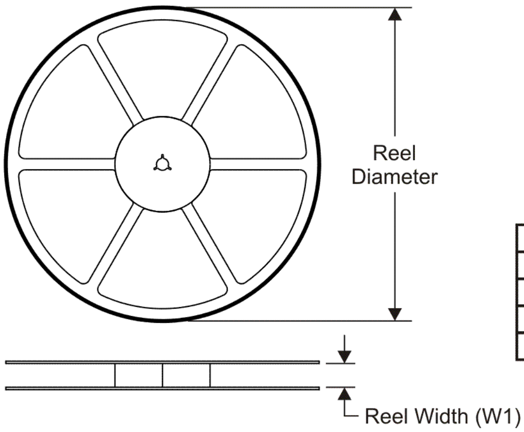
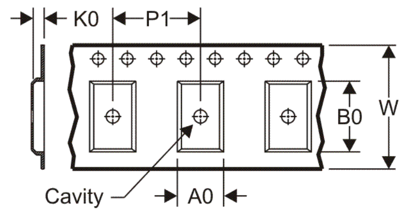
TAPE AND REEL INFORMATION

REEL DIMENSIONS

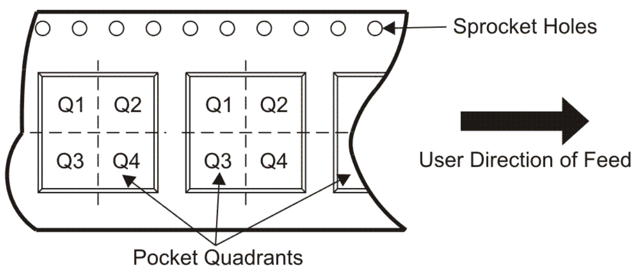


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

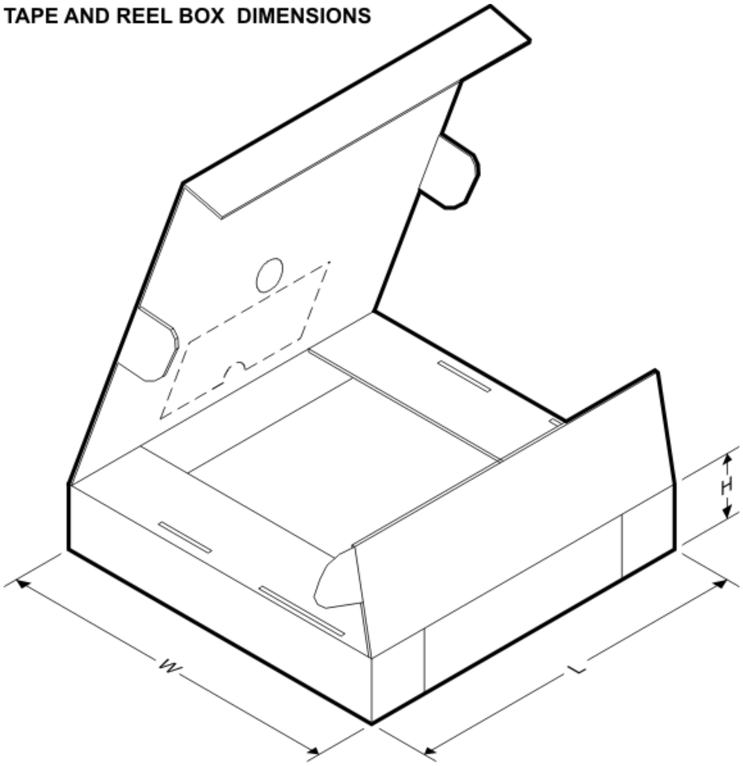
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22932BYFPR	DSBGA	YFP	6	3000	180.0	8.4	0.89	1.29	0.62	4.0	8.0	Q1
TPS22932BYFPT	DSBGA	YFP	6	250	180.0	8.4	0.89	1.29	0.62	4.0	8.0	Q1

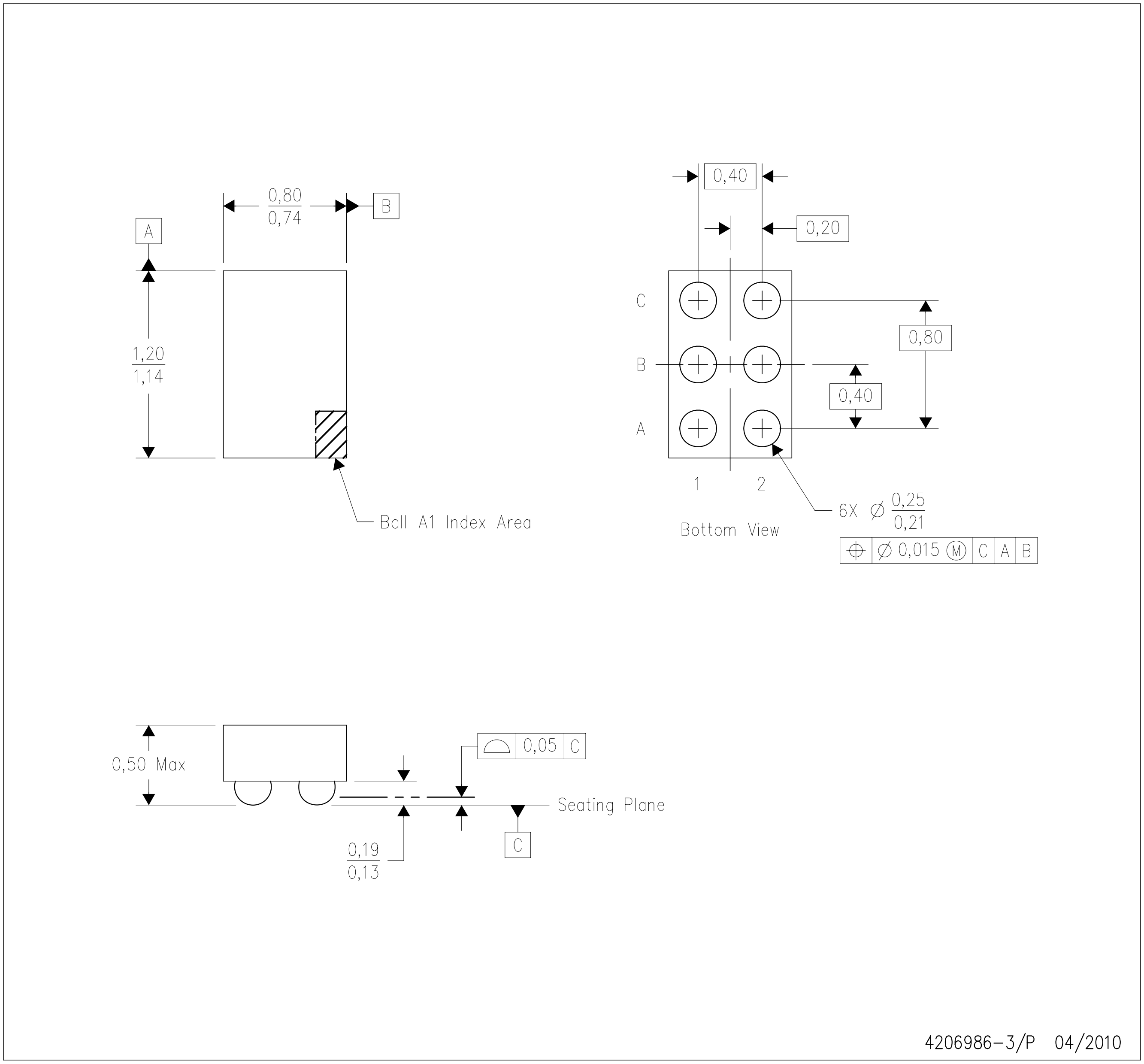
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

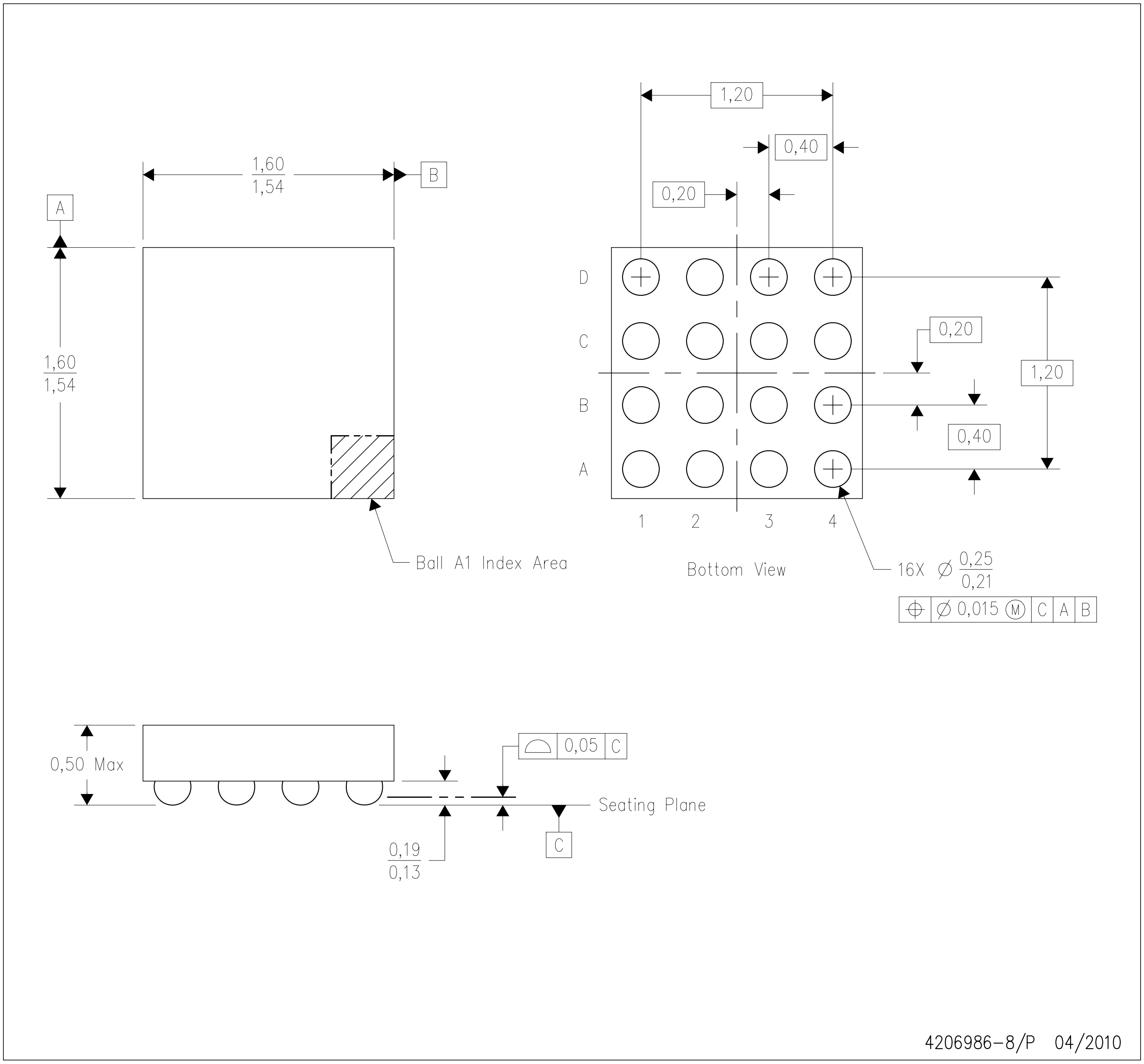
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22932BYFPR	DSBGA	YFP	6	3000	220.0	220.0	34.0
TPS22932BYFPT	DSBGA	YFP	6	250	220.0	220.0	34.0

YFP (R–XBGA–N6) DIE–SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. This is a Pb–free solder ball design.

YFP (S–XBGA–N16) DIE–SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. This is a Pb–free solder ball design.

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