

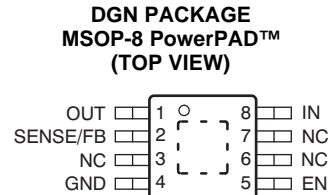
50 mA, 3 V TO 80 V, MICROPOWER, LOW-DROPOUT LINEAR REGULATOR

FEATURES

- Qualified for Automotive Applications
- Wide Input Voltage Range: 3 V to 80 V
- Low Quiescent Current: 40 μ A (Typ)
- Low Dropout Voltage: 300 mV (Typ)
- Output Current: 50 mA
- No Input Protection Diodes Needed
- Adjustable Output From 1.26 V to 28 V
- 1- μ A Quiescent Current in Shutdown
- Stable With 1- μ F Output Capacitor
- Stable With Aluminum, Tantalum, or Ceramic Capacitors
- Reverse Input-Battery Protection
- Reverse Output Current Flow Protection
- Thermal Limiting
- Available in MSOP-8 Package

APPLICATIONS

- Low-Current, High-Voltage Regulators
- Regulators for Battery-Powered Systems
- Telecom
- Automotive



Note: The exposed thermal pad is connected to ground via pin 4 (GND).

DESCRIPTION

The TPS798xx is the first device in a line of 80-V high-voltage micropower low-dropout (LDO) linear regulators. This device is capable of supplying 50-mA output current with a dropout voltage of only 300 mV. Designed for low quiescent current high voltage (80 V) applications, 40 μ A operating and 1 μ A in shutdown makes the TPS798xx an ideal choice for battery-powered or high-voltage systems. Quiescent current is also well-controlled in dropout.

Other features of the TPS798xx include the ability to operate with low equivalent series resistance (ESR) ceramic output capacitors. This device is stable with only 1 μ F on the output; most older devices require between 10- μ F and 100- μ F tantalum capacitors for stability. Small ceramic capacitors can be used without the necessary addition of ESR, as is common with other regulators. Internal protection circuitry includes reverse input-battery protection, reverse output current protection, current limiting, and thermal limiting to protect the device in various fault conditions.

This device is available in a fixed output voltage of 5 V (TPS79850) and with an adjustable output voltage with a 1.275-V reference voltage (TPS79801). The TPS798xx regulator is available in a 8-lead MSOP (DGN) package with an exposed pad for enhanced thermal management capability.

ORDERING INFORMATION⁽¹⁾

T _J	V _{OUT} (NOM)	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	–40°C to 125°C	Adjustable	MSOP – DGN	Reel of 2500	TPS79801QDGNRQ1
5 V		TPS79850QDGNRQ1			OOLQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) For fixed 1.24 V, tie FB to out.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range (unless otherwise noted).

V _{IN}	Input voltage range	IN	-65 V to 80 V
		OUT	-0.3 V to 28 V
		Input-to-output differential	-65 V to 28 V
		FB	-0.3 V to 7 V
		EN	-65 V to 80 V
		Enable to IN differential	0.6 V < V _{IN}
θ _{JA}	Thermal impedance, junction to free air	JEDEC 51-5 ⁽²⁾	60°C/W
		JEDEC 51-7 ⁽³⁾	130°C/W
T _{LEAD}	Maximum lead temperature (10 s soldering time)		300°C
T _J	Junction temperature range		-40°C to 125°C
T _{STG}	Storage temperature range		-65°C to 150°C
ESD rating		Human-Body Model (HBM)	2000 V
		Charged-Device Model (CDM)	1000 V

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The thermal data is based on using JEDEC 51-5. The copper pad is soldered to the thermal land pattern and using 5 by 8 thermal array (vias). Correct attachment procedure must be incorporated.
- (3) The thermal data is based on using JEDEC 51-7. The copper pad is soldered to the thermal land. No thermal vias. Correct attachment procedure must be incorporated.

DISSIPATION RATINGS⁽¹⁾

BOARD	PACKAGE	R _{θJC}	R _{θJA}	DERATING FACTOR ABOVE T _A = 25°C	T _A ≤ 25°C POWER RATING	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
High-K ⁽²⁾	DGN	8.2°C/W	60°C/W	16.6 mW/°C	1.83 W	1.08 W	0.833 W

- (1) See [Thermal Considerations](#) in the *Applications Information* section for more information related to thermal design.
- (2) The JEDEC High-K (1s) board design used to derive this data was a 4.5-inch x 3-inch, 2-layer board with 2-ounce copper traces on top of the board.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT	
V _{IN}	Input voltage	IN	-65	80	V
		OUT	-0.3	28	
		Input-to-output differential	-65	80	
		ADJ	-0.3	7	
		SHDN	-65	80	
I _{OUT}	Output current		50	mA	
T _J	Operating junction temperature ⁽¹⁾⁽²⁾⁽³⁾	-40	125	°C	

- (1) Operating conditions are limited by maximum junction temperature. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.
- (2) The TPS798xx is specified to meet performance specifications from -40°C to 125°C operating junction temperature. Specifications over the -40°C to 125°C operating junction temperature range are specified by design, characterization, and correlation with statistical process controls.
- (3) This device includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature exceeds 125°C Min. when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

ELECTRICAL CHARACTERISTICS

Over the operating temperature range of $T_J = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = V_{OUT(NOM)} + 1.0\text{ V}$ or 4.0 V (whichever is greater for either fixed or adjustable versions), $I_{LOAD} = 1.0\text{ mA}$, $V_{EN} = 3.0\text{ V}$, $C_{OUT} = C_{IN} = 2.2\text{ }\mu\text{F}$. For TPS79801 FB pin tied to V_{OUT} . Typical values are at $T_J = 25^{\circ}\text{C}$. Min and max values are over full operating temperature range, unless otherwise noted.

PARAMETER	TEST CONDITIONS	T_J	TPS798xx			UNIT		
			MIN	TYP	MAX			
V_{IN}	Minimum input voltage	$I_{LOAD} = 50\text{ mA}$	Full range		3	4	V	
Fixed V_{OUT}	Initial output voltage accuracy	$V_{IN} = V_{OUT\text{ nom}} + 0.5\text{ V}$	25°C		-1.5	+1.5	%	
	Output voltage accuracy over line, load, and full temperature range	$V_{IN} = V_{OUT\text{ nom}} + 1\text{ V}$ to 80 V , $I_{LOAD} = 1\text{ mA}$ to 50 mA	Full range		-3.0	+3.0	%	
Adjustable V_{OUT}	Initial output voltage accuracy	$V_{IN} = 3\text{ V}$	25°C		1.256	1.275	1.294	V
	Output voltage accuracy over line, load, and full temperature range	$V_{IN} = 4\text{ V}$ to 80 V , $I_{LOAD} = 1\text{ mA}$ to 50 mA	Full range		1.237	1.275	1.313	V
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation, adjustable V_{OUT}	$\Delta V_{IN} = 3\text{ V}$ to 80 V	Full range		13		mV	
	Line regulation, fixed V_{OUT}	$\Delta V_{IN} = V_{OUT\text{ nom}} + 0.5\text{ V}$ to 80 V ,	Full range		15		mV	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation, adjustable V_{OUT}	$\Delta I_{LOAD} = 1\text{ mA}$ to 50 mA	25°C		20		mV	
			Full range		32		mV	
	Load regulation, fixed V_{OUT}	$\Delta I_{LOAD} = 1\text{ mA}$ to 50 mA	25°C		50		mV	
			Full range		90		mV	
Adjustable V_{OUT}	Output voltage range ⁽¹⁾⁽²⁾	$V_{IN} = 38\text{ V}$	Full range		1.229	28	V	
V_{DO}	Dropout voltage ⁽³⁾⁽⁴⁾	$V_{IN} = V_{OUT(NOM)} - 0.1\text{ V}$	25°C		85	150	mV	
			Full range		190		mV	
		$I_{LOAD} = 10\text{ mA}$, $V_{IN} = V_{OUT(NOM)} - 0.1\text{ V}$	25°C		170	260	mV	
			Full range		350		mV	
		$I_{LOAD} = 50\text{ mA}$, $V_{IN} = V_{OUT(NOM)} - 0.1\text{ V}$	25°C		300	370	mV	
			Full range		550		mV	
I_{GND}	GND pin current ⁽⁵⁾	$V_{IN} = V_{OUT(NOM)}$	$I_{LOAD} = 0\text{ mA}$	Full range		30	80	μA
			$I_{LOAD} = 1\text{ mA}$	Full range		100	180	μA
			$I_{LOAD} = 10\text{ mA}$	Full range		400	700	μA
			$I_{LOAD} = 50\text{ mA}$	Full range		1.8	3.3	mA
V_N	Output voltage noise	$C_{OUT} = 10\text{ }\mu\text{F}$, $I_{LOAD} = 50\text{ mA}$, BW = 10 Hz to 100 kHz, $V_{IN} = 4.3\text{ V}$, $V_{OUT} = 3.3\text{ V}$ (adjustable used)	25°C		100		μV_{RMS}	
I_{FB}	FB pin bias current ⁽⁶⁾	$V_{IN} = 3.0\text{ V}$	25°C		0.53	0.7	μA	
V_{EN}	EN pin high (enabled) ⁽⁷⁾	OFF to ON, $V_{IN} = 6.0\text{ V}$	Full range		1.5		V	
	EN pin low (shutdown) ⁽⁷⁾	ON to OFF, $V_{IN} = 6.0\text{ V}$	25°C		0.4 V		V	
	EN pin low (shutdown) ⁽⁷⁾	ON to OFF, $V_{IN} = 6.0\text{ V}$	Full range		0.2 V		V	
I_{EN}	EN pin current ⁽⁷⁾	$V_{EN} = 0\text{ V}$, $V_{IN} = 6.0\text{ V}$, $I_{LOAD} = 0\text{ mA}$	Full range		0.4	2.0	μA	
		$V_{EN} = 3\text{ V}$, $V_{IN} = 6.0\text{ V}$, $I_{LOAD} = 0\text{ mA}$	Full range		0.4	0.5	μA	
$I_{shutdown}$	GND pin current ⁽⁵⁾	$V_{IN} = 6\text{ V}$, $V_{EN} = 0\text{ V}$, $I_{LOAD} = 0\text{ mA}$	Full range		3	25	μA	
PSRR	Power-supply rejection ratio	$V_{IN} = 4.3\text{ V}$, $V_{OUT} = 3.3\text{-V}$, $V_{RIPPLE} = 0.5\text{ V}_{PP}$, $f_{RIPPLE} = 120\text{ Hz}$, $I_{LOAD} = 50\text{ mA}$	25°C		65		dB	

- (1) This parameter is tested and specified under pulse load conditions such that $T_J = T_A$. This device is 100% production tested at $T_A = 25^{\circ}\text{C}$. Performance at $T_A = -40^{\circ}\text{C}$ to 125°C is specified by design, characterization, bench to ATE correlation testing, and other statistical process controls.
- (2) This device is limited by a maximum junction temperature of $T_J = 125^{\circ}\text{C}$. The regulated output voltage specification cannot be applied to all combinations of various V_{IN} , V_{OUT} , ambient temperature, and I_{OUT} conditions. When operating with large voltage differentials across the device, the output load must be limited so as not to violate the maximum junction temperature for a given ambient temperature.
- (3) In the adjustable version test, the output uses an external voltage divider. This resistor voltage divider is made up of $R_1 = 215\text{ k}\Omega$ and R_2 (bottom resistor) = $340\text{ k}\Omega$. This configuration preloads the output with $6.0\text{ }\mu\text{A}$.
- (4) By definition, dropout voltage is the minimum input voltage needed to maintain a given output voltage at a specific load current. For dropout testing, minimum $V_{IN} = V_{OUT(NOM)} \times 0.96$. This specification ensures that the device is in dropout and takes into account the output voltage tolerance over the full temperature range.
- (5) Ground pin current is tested with $V_{IN} = V_{OUT(NOM)}$ or 3 V , whichever is greater.
- (6) FB pin current flows into the FB pin.
- (7) EN pin current flows into the EN pin.

ELECTRICAL CHARACTERISTICS (continued)

Over the operating temperature range of $T_J = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = V_{OUT(NOM)} + 1.0\text{ V}$ or 4.0 V (whichever is greater for either fixed or adjustable versions), $I_{LOAD} = 1.0\text{ mA}$, $V_{EN} = 3.0\text{ V}$, $C_{OUT} = C_{IN} = 2.2\text{ }\mu\text{F}$. For TPS79801 FB pin tied to V_{OUT} . Typical values are at $T_J = 25^{\circ}\text{C}$. Min and max values are over full operating temperature range, unless otherwise noted.

PARAMETER		TEST CONDITIONS	T_J	TPS798xx			UNIT
				MIN	TYP	MAX	
I_{LIMIT}	Fixed current limit ⁽⁸⁾	$\Delta V_{OUT} = V_{OUT(NOM)} - 0.1\text{ V}$	Full range	60		200	mA
	Adjustable current limit	$\Delta V_{OUT} = V_{OUT(NOM)} - 0.1\text{ V}$	Full range	60		200	mA
I_{RL}	Input reverse leakage current(reverse battery test)	$V_{IN} = -60\text{ V}$, $V_{OUT} = \text{open}$, C_{IN} open	Full range			6	mA
I_{RO}	Reverse output current ⁽⁹⁾	$V_{OUT} = V_{OUT(NOM)}$, $V_{IN} = \text{ground}$	25°C		19	25	μA
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing	25°C		165		$^{\circ}\text{C}$
		Reset, temperature decreasing	25°C		140		$^{\circ}\text{C}$

- (8) Current limit is tested with $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or 3.0 V , whichever is greater. V_{OUT} is forced to $V_{OUT(NOM)} - 0.1\text{ V}$ and the output current is measured.
- (9) Reverse output current is tested with the IN pin tied to ground and the output forced to $V_{OUT(NOM)} + 0.1\text{ V}$. This current flows into the OUT pin and out of the GND pin and then measured.

FUNCTIONAL BLOCK DIAGRAMS

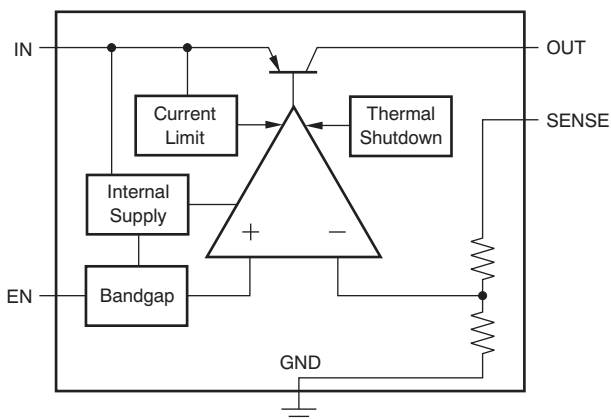


Figure 1. Fixed Voltage Output Version

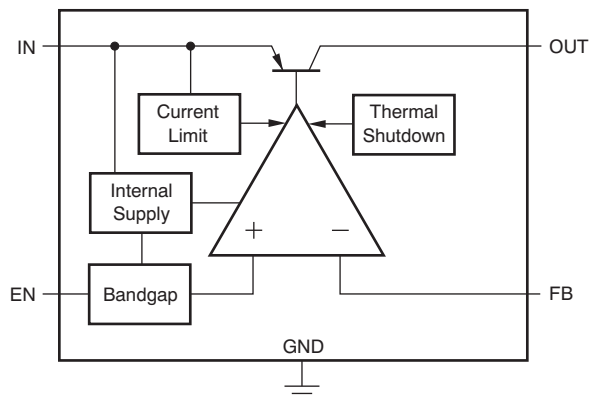
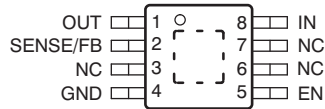


Figure 2. Adjustable Voltage Output Version

PIN CONFIGURATIONS

**DGN PACKAGE
MSOP-8 PowerPAD
(TOP VIEW)**

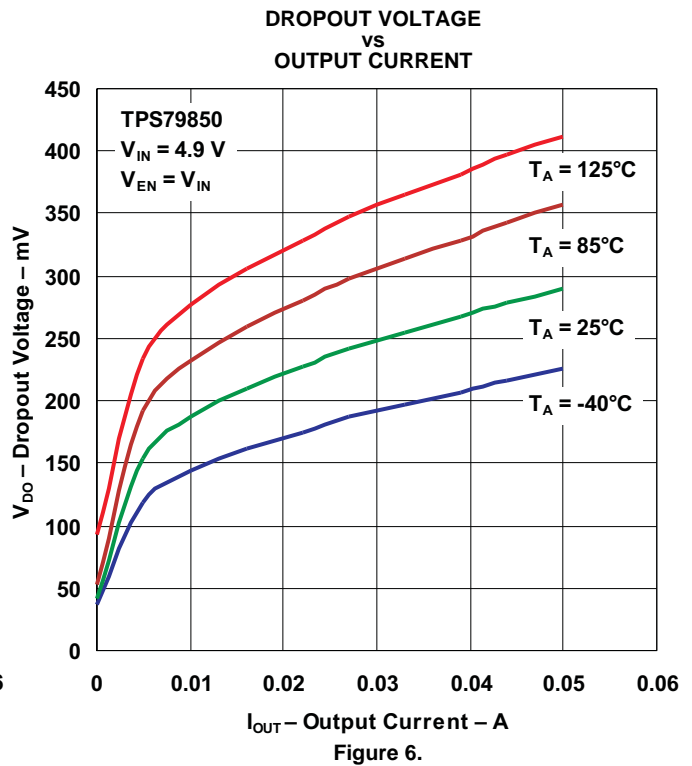
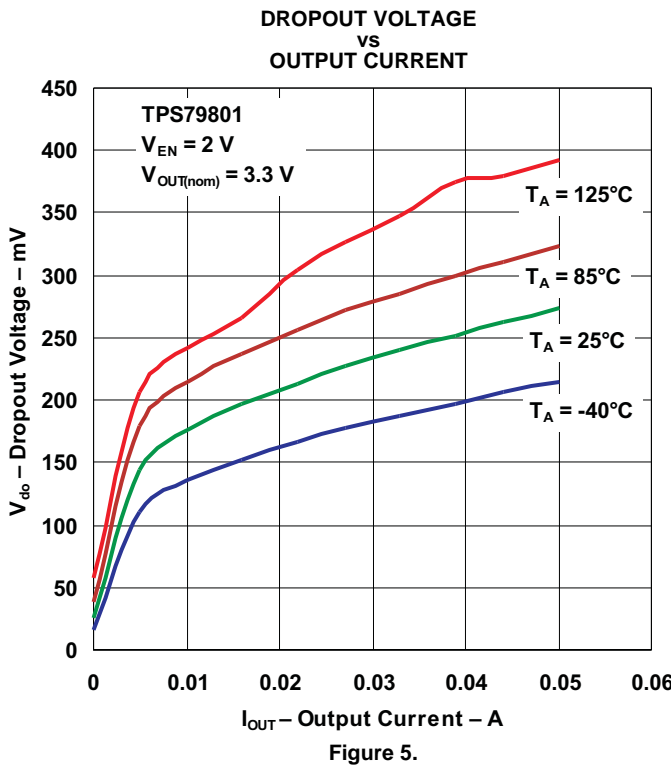
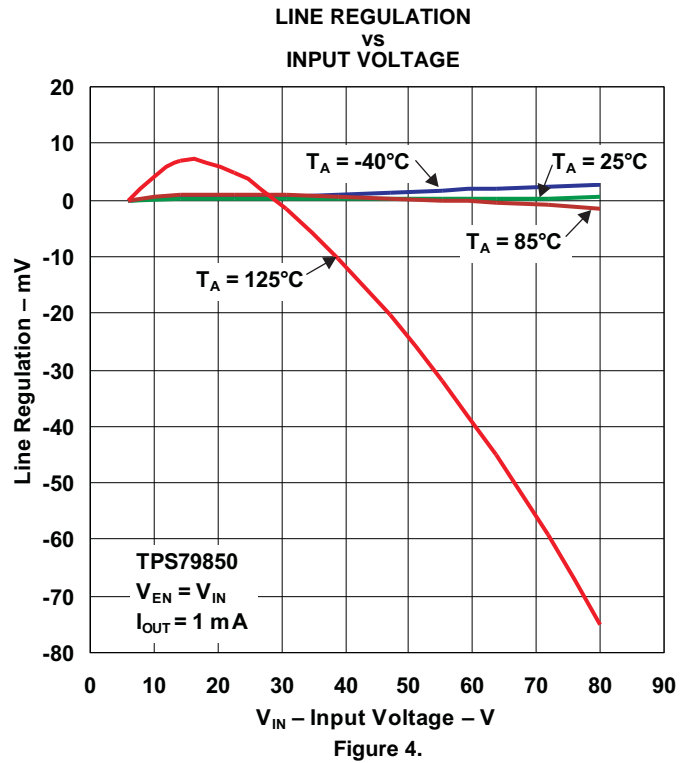
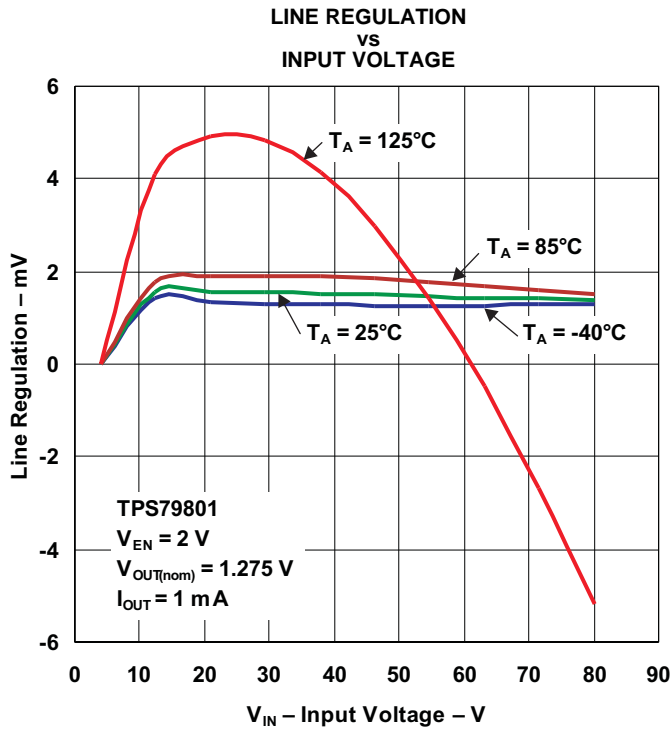


Note: The exposed thermal pad is connected to ground via pin 4 (GND).

PIN DESCRIPTIONS

PIN		DESCRIPTION
NAME	DGN	
EN	5	Enable pin. Driving the EN pin high turns on the regulator over full operating range. Driving this pin low puts the regulator into shutdown mode over full operating range.
IN	8	Input pin. A 0.1- μ F ceramic or greater capacitor is recommended from this pin to ground to assure stability. Both input and output capacitor grounds should be tied back to the IC ground with no significant impedance between them.
GND	4	Ground. The exposed thermal pad is connected to ground via this pin.
OUT	1	Regulated output voltage pin. A small (1 μ F) capacitor is needed from this pin to ground to assure stability.
SENSE/FB	2	This pin is the input to the control loop error amplifier; it is used to set the output voltage of the device.
NC	3, 6, 7	No internal connection

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS (continued)

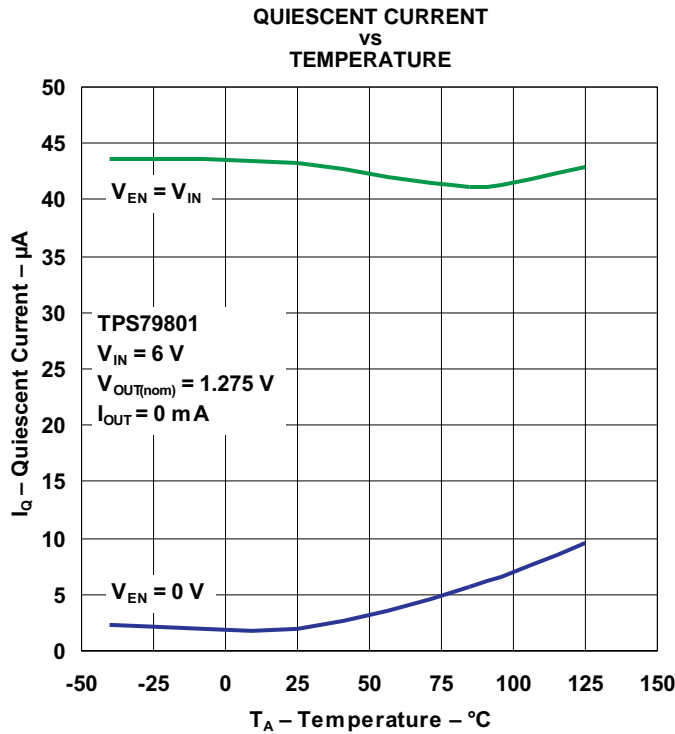


Figure 7.

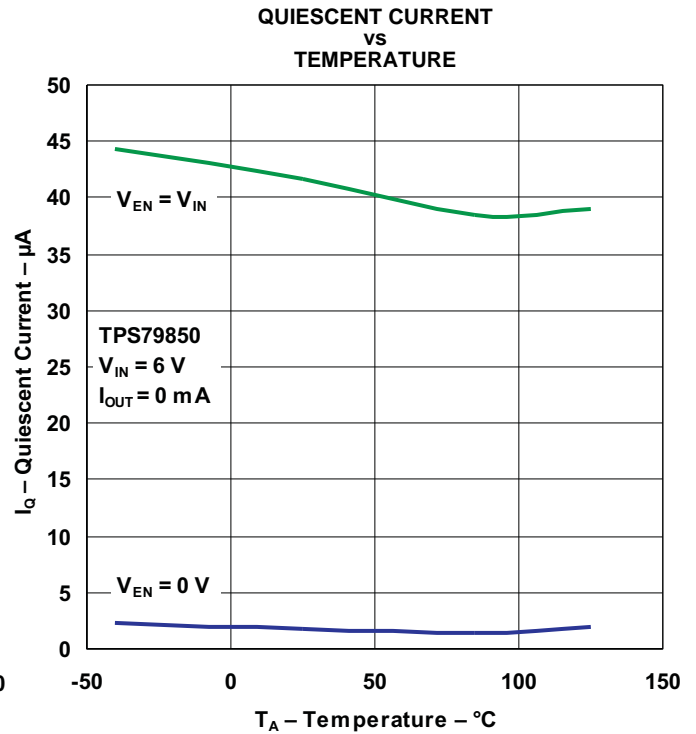


Figure 8.

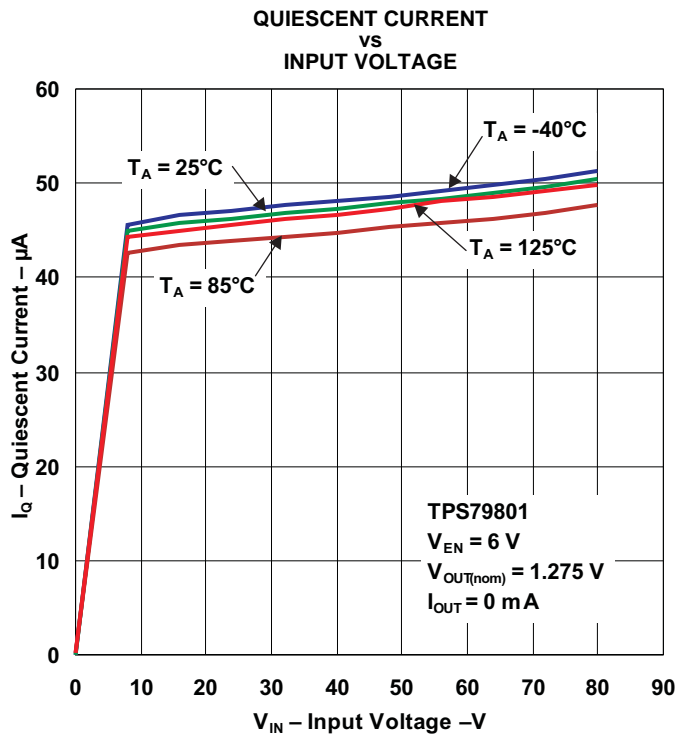


Figure 9.

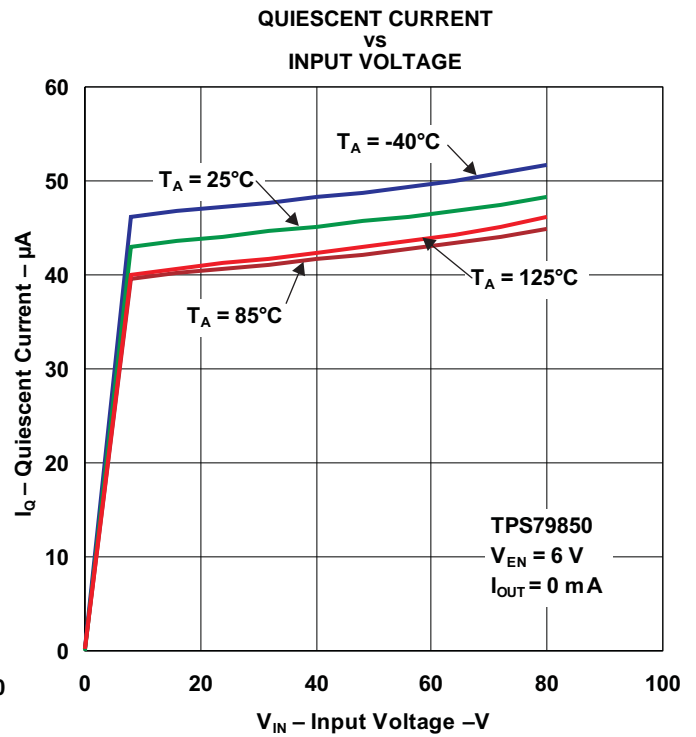
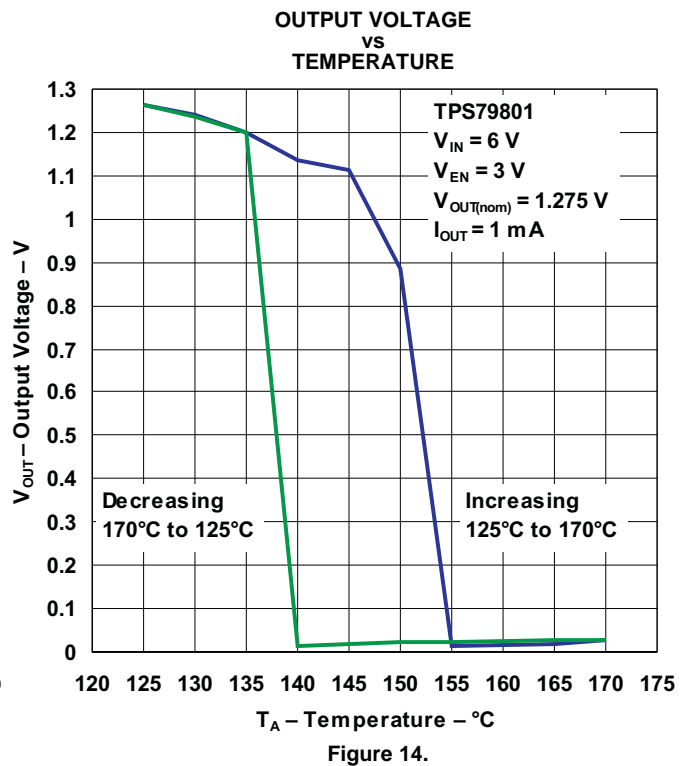
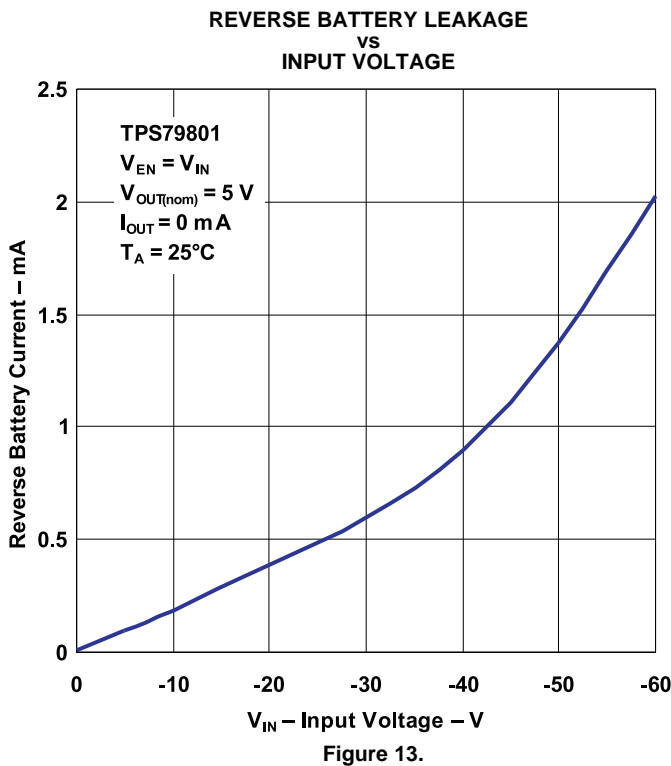
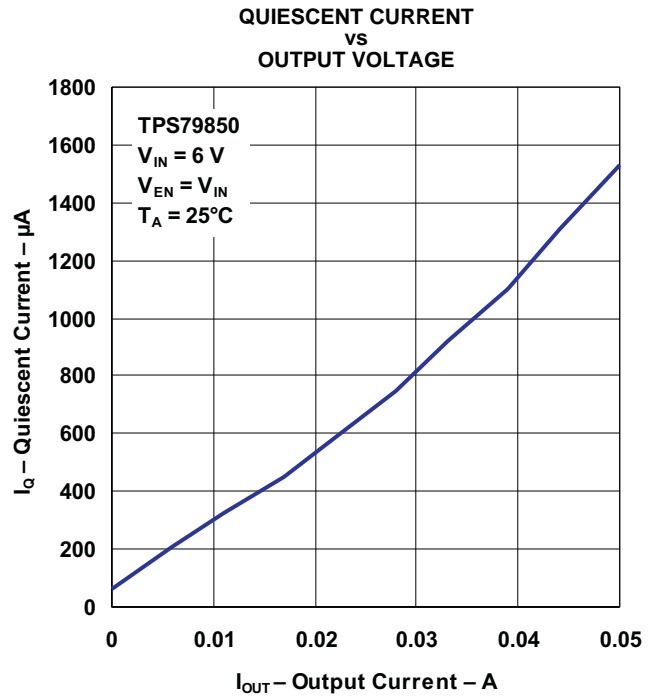
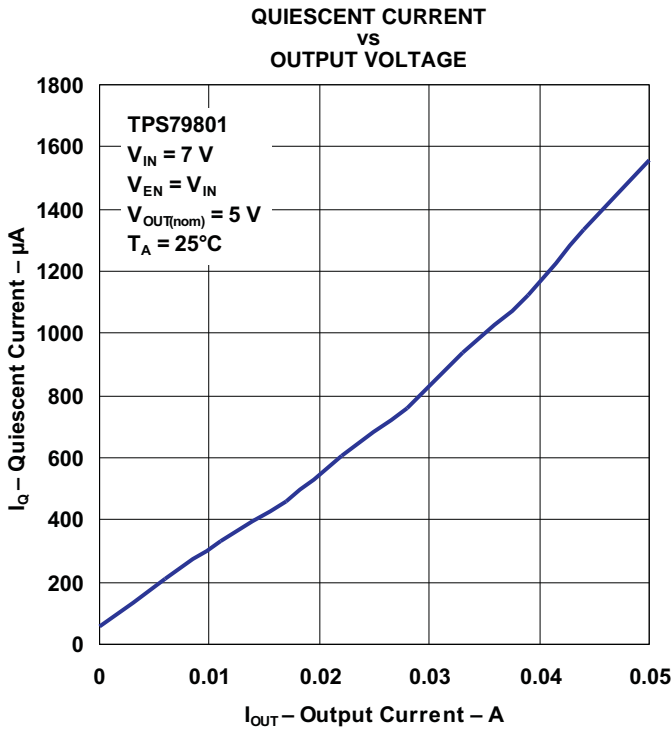
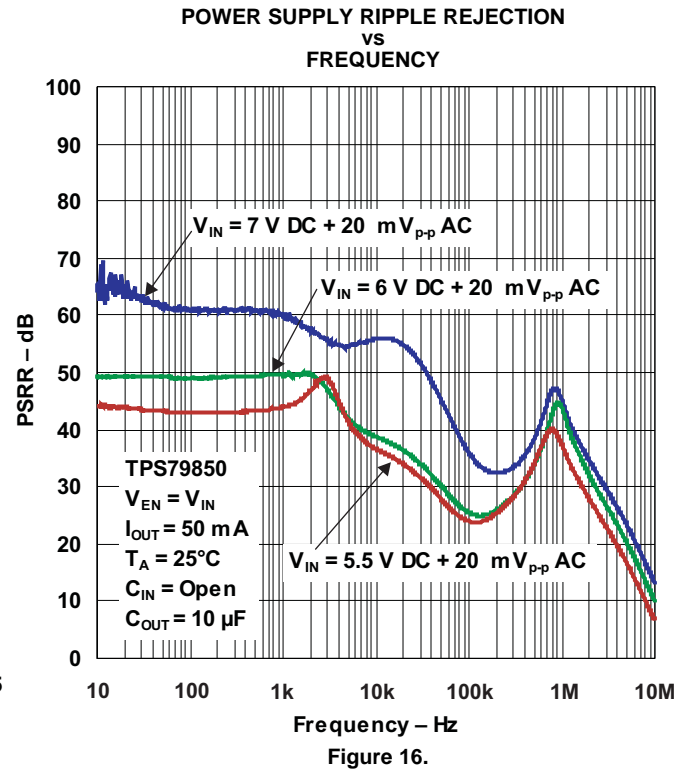
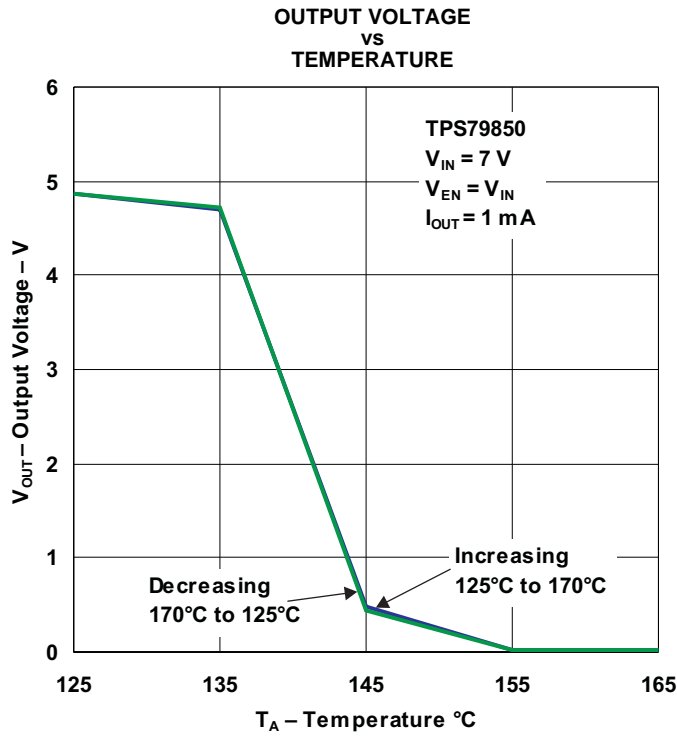


Figure 10.

TYPICAL CHARACTERISTICS (continued)



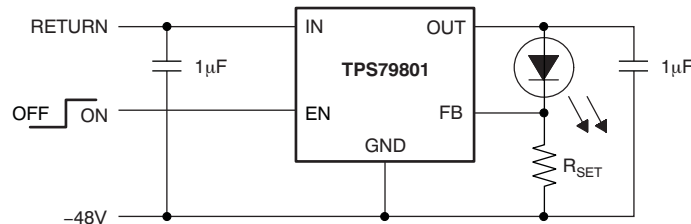
TYPICAL CHARACTERISTICS (continued)



APPLICATION INFORMATION

The TPS798xx is a 50-mA high-voltage LDO regulator with micropower quiescent current and shutdown. The device is capable of supplying 50 mA at a dropout voltage of 300 mV (typ). The low operating quiescent current (40 μ A) drops to 1 μ A in shutdown. In addition to the low quiescent current, the TPS798xx incorporates several protection features that make it ideal for battery-powered applications.

The device is protected against both reverse-input and reverse-output voltages. In battery-backup applications, where the output can be held up by a backup battery when the input is pulled to ground, the TPS798xx acts as if it has a diode in series with its output and prevents reverse current flow. [Figure 17](#) and [Figure 18](#) illustrate two typical applications.



Note: $I_{LED} = 1.275 \text{ V}/R_{SET}$
 -48 V can vary from -4 V to -80 V

Figure 17. Constant Brightness for Indicator LED Over Wide Input Voltage Range

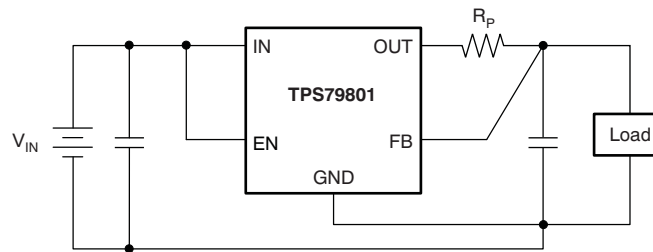
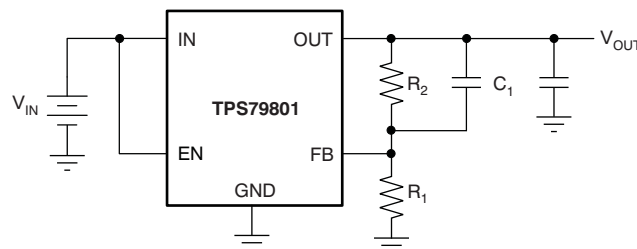


Figure 18. Kelvin Sense Connection

Adjustable Operation

The TPS798xx has an output voltage range of 1.275 V to 28 V. The output voltage is set by the ratio of two external resistors as shown in [Figure 19](#). The feedback loop monitors the output to maintain the voltage at the adjust pin at 1.275 V referenced to ground. The current in R_1 is then equal to $1.275 \text{ V}/R_1$, and the current in R_2 is the current in R_1 plus the FB pin bias current. The FB pin bias current, 0.53 μ A at 25°C, flows through R_2 into the FB pin. The output voltage can be calculated using the formula in [Figure 19](#). The value of R_1 should be less than 250 k Ω to minimize errors in the output voltage caused by the FB pin bias current. Note that in shutdown, the output is turned off and the divider current is zero.



$$V_{OUT} = 1.275 \text{ V} \left(1 + \frac{R_2}{R_1} \right) + I_{FB} R_2$$

$$V_{FB} = 1.275 \text{ V}$$

$$I_{FB} = 50 \text{ nA at } 25^\circ\text{C}$$

$$\text{Output Range} = 1.275 \text{ V to } 28 \text{ V}$$

Figure 19. Adjustable Operation

A 100-pF capacitor (C_1) placed in parallel with the top resistor (R_2) of the output divider is necessary for stability and transient performance of the adjustable TPS798xx. The impedance of C_1 at 10 kHz should be less than the value of R_1 .

The adjustable device is tested and specified with the FB pin tied to the OUT pin and a 1 mA dc load (unless otherwise specified) for an output voltage of 1.275 V. Specifications for output voltages greater than 1.275 V are proportional to the ratio of the desired output voltage to 1.275 V ($V_{OUT}/1.275$ V). For example, load regulation for an output current change of 1 mA to 50 mA is -10 mV (typ) at $V_{OUT} = 1.275$ V.

At $V_{OUT} = 12$ V, load regulation is:

$$(12 \text{ V}/1.275 \text{ V}) \times (-10 \text{ mV}) = -94 \text{ mV}$$

Output Capacitance and Transient Response

The TPS798xx is designed to be stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. A minimum output capacitor of $1 \mu\text{F}$ with an ESR of 3Ω or less is recommended to prevent oscillations. The TPS798xx is a micropower device, and output transient response is a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the TPS798xx, increase the effective output capacitor value.

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. The most common dielectrics used are Z5U, Y5 V, X5R, and X7R. The Z5U and Y5 V dielectrics are good for providing high capacitances in a small package, but exhibit strong voltage and temperature coefficients. When used with a 5 V regulator, a $10 \mu\text{F}$ Y5 V capacitor can exhibit an effective value as low as $1 \mu\text{F}$ to $2 \mu\text{F}$ over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals because of mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients.

Thermal Considerations

The power handling capability of the device is limited by the maximum rated junction temperature (125°C). The power dissipated by the device consists of two components:

- Output current multiplied by the input/output voltage differential: $I_{OUT} \times (V_{IN} - V_{OUT})$
- GND pin current multiplied by the input voltage: $I_{GND} \times V_{IN}$

The GND pin current can be found by examining the GND pin current curves in the [Typical Characteristics](#). Power dissipation is equal to the sum of the two components listed previously.

The TPS798xx series regulators have internal thermal limiting designed to protect the device during overload conditions. For continuous normal conditions, do not exceed the maximum junction temperature rating of 125°C . It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

For surface-mount devices, heat sinking is accomplished by using the heat-spreading capabilities of the printed circuit board (PCB) and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

Calculating Junction Temperature

Given an output voltage of 5 V, an input voltage range of 15 V to 24 V, an output current range of 0 mA to 50 mA, and a maximum ambient temperature of 50°C, the maximum junction temperature is calculated as follows.

The power dissipated (P_{DISS}) by the DGN package is equal to:

$$I_{OUT(MAX)}(V_{IN(MAX)} - V_{OUT}) + I_{GND}(V_{IN(MAX)})$$

Where:

$$I_{OUT(MAX)} = 50 \text{ mA}$$

$$V_{IN(MAX)} = 24 \text{ V}$$

$$V_{OUT} = 5 \text{ V}$$

$$I_{GND} \text{ at } (I_{OUT} = 50 \text{ mA}, V_{IN} = 24 \text{ V}) = 1 \text{ mA}$$

Therefore,

$$P_{DISS} = 50 \text{ mA } (24 \text{ V} - 5 \text{ V}) + 1 \text{ mA } (24 \text{ V}) = 0.974 \text{ W}$$

The thermal resistance is approximately 60°C/W, based on JEDEC 51-5 profile. Therefore, the junction temperature rise above ambient is approximately equal to:

$$0.974 \text{ W} \times 60^\circ\text{C/W} = 58.44^\circ\text{C}$$

The maximum junction temperature is then equal to the maximum junction temperature rise above ambient plus the maximum ambient temperature or:

$$T_J \text{ max} = 50^\circ\text{C} + 58.44^\circ\text{C} = 108.44^\circ\text{C}$$

Protection Features

The TPS798xx incorporates several protection features that make it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device is protected against reverse-input voltages, and reverse currents from output to input.

Current-limit protection and thermal-overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature should not exceed 125°C.

The input of the device withstands reverse voltages of –60 V. Current flow into the device is limited to less than 6 mA (typically, less than 100 μA), and no negative voltage appears at the output. The device protects both itself and the load. This architecture also provides protection against batteries that may be plugged in backwards.

The FB pin of the adjustable device can be pulled above or below ground by as much as 7 V without damaging the device. If the input is left open or grounded, the FB pin behaves as an open circuit when pulled below ground, or as a large resistor (typically, 100 k Ω) in series with a diode when pulled above ground. If the input is powered by a voltage source, pulling the FB pin below the reference voltage increases the output voltage. This configuration causes the output to go to a unregulated high voltage. Pulling the FB pin above the reference voltage turns off all output current.

In situations where the FB pin is connected to a resistor divider that would pull the FB pin above its 7 V clamp voltage if the output is pulled high, the FB pin input current must be limited to less than 5 mA. For example, a resistor divider provides a regulated 1.5 V output from the 1.23-V reference when the output is forced to 28 V. The top resistor of the resistor divider must be chosen to limit the current into the FB pin to less than 5 mA when the FB pin is at 7 V. The 21-V difference between the OUT and FB pins divided by the 5-mA maximum current into the FB pin yields a minimum top resistor value of 5.8 k Ω .

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage, or is left open. The rise in reverse output current above 7 V occurs from the breakdown of the 7 V clamp on the FB pin. With a resistor divider on the regulator output, this current is reduced, depending on the size of the resistor divider.

When the IN pin of the TPS798xx is forced below the OUT pin, or the OUT pin is pulled above the IN pin, input current typically drops to less than 0.6 mA. This scenario can occur if the input of the TPS798xx is connected to a discharged (low voltage) battery and the output is held up by either a backup battery or a second regulator circuit. The state of the EN pin has no effect on the reverse output current when the output is pulled above the input.

Thermal Information

The amount of heat that an LDO linear regulator generates is directly proportional to the amount of power it dissipates during operation. All integrated circuits have a maximum allowable junction temperature ($T_J \text{ max}$) above which normal operation is not assured. The operating environment must be designed so that the operating junction temperature (T_J) does not exceed the maximum junction temperature ($T_J \text{ max}$). The two primary environmental variables that can be used to improve thermal performance are air flow and external heatsinks. The purpose of this section is to help the designer to determine the proper operating environment for a linear regulator that operates at a specific power level.

In general, the maximum expected power ($P_D \text{ max}$) consumed by a linear regulator is computed as shown in [Equation 1](#):

$$P_{D \text{ max}} = (V_{IN(\text{avg})} - V_{OUT(\text{avg})}) \times I_{OUT(\text{avg})} + V_{I(\text{avg})} \times I_Q$$

Where:

$V_{IN(\text{avg})}$ is the average input voltage.

$V_{OUT(\text{avg})}$ is the average output voltage.

$I_{OUT(\text{avg})}$ is the average output current.

I_Q is the quiescent current.

(1)

For most TI LDO regulators, the quiescent current is insignificant compared to the average output current; therefore, the term $V_{IN(\text{avg})} \times I_Q$ can be ignored. The operating junction temperature is computed by adding the ambient temperature (T_A) and the increase in temperature as a result of the regulator power dissipation. The temperature rise is computed by multiplying the maximum expected power dissipation by the sum of the thermal resistances between the junction and the case ($R_{\theta JC}$), the case to heatsink ($R_{\theta CS}$), and the heatsink to ambient ($R_{\theta SA}$). Thermal resistances are measurements of how effectively an object dissipates heat. Typically, the larger the device, the more surface area available for power dissipation and the lower the device thermal resistance.

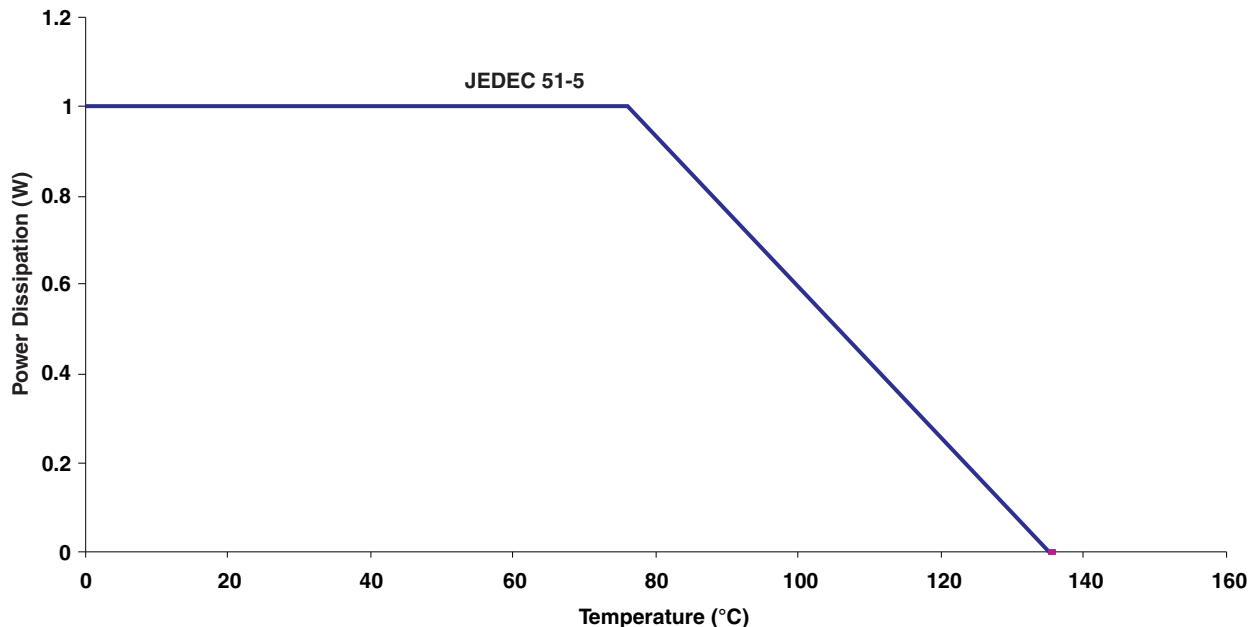


Figure 20. Power Dissipation vs Temperature

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS79801QDGNRQ1	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79850QDGNRQ1	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79801QDGNRQ1	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS79850QDGNRQ1	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

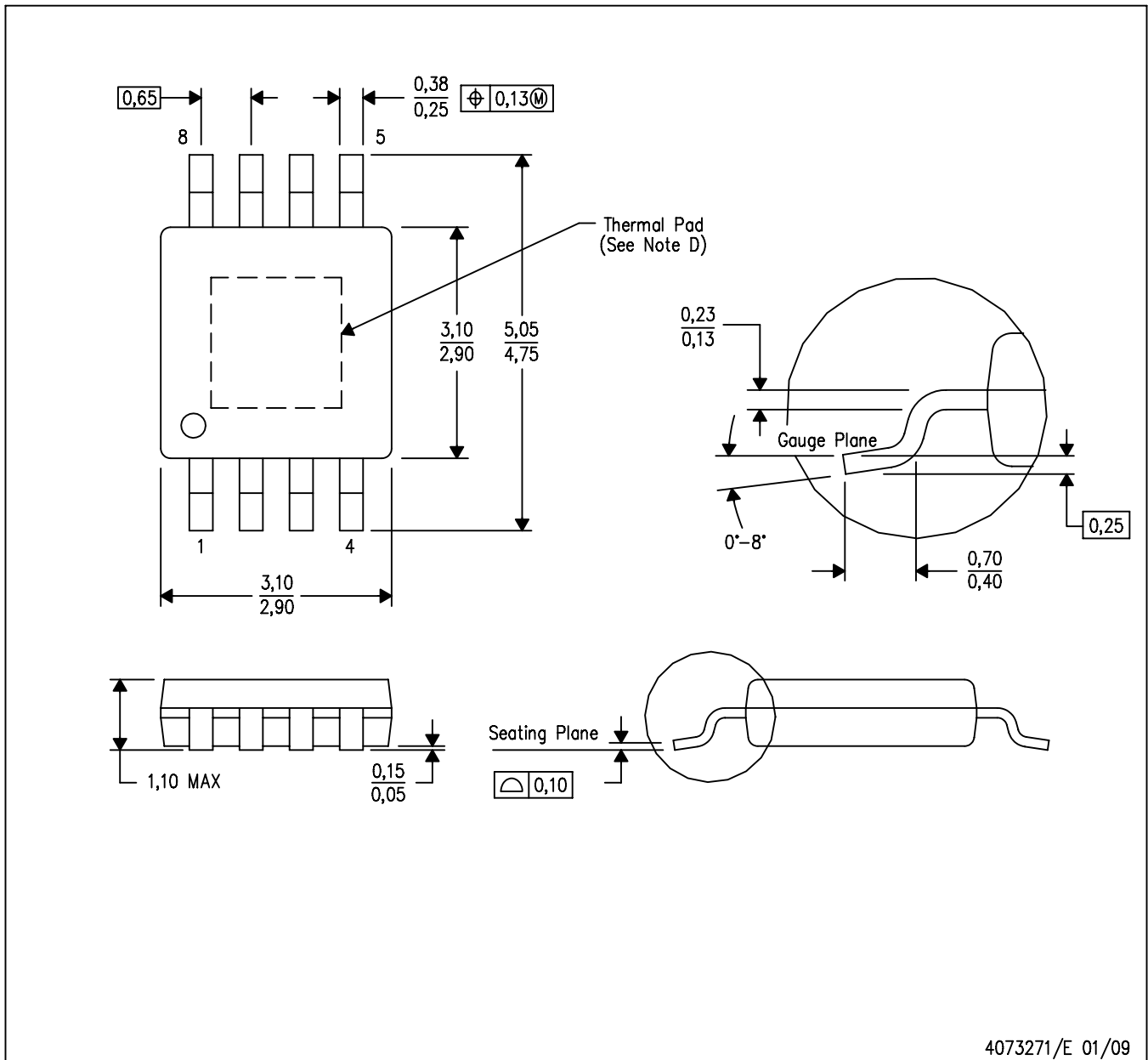

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79801QDGNRQ1	MSOP-PowerPAD	DGN	8	2500	370.0	355.0	55.0
TPS79850QDGNRQ1	MSOP-PowerPAD	DGN	8	2500	370.0	355.0	55.0

MECHANICAL DATA

DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



4073271/E 01/09

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - Falls within JEDEC MO-187 variation AA-T

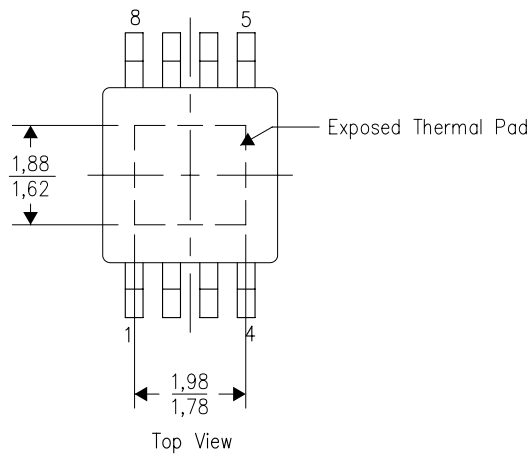
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

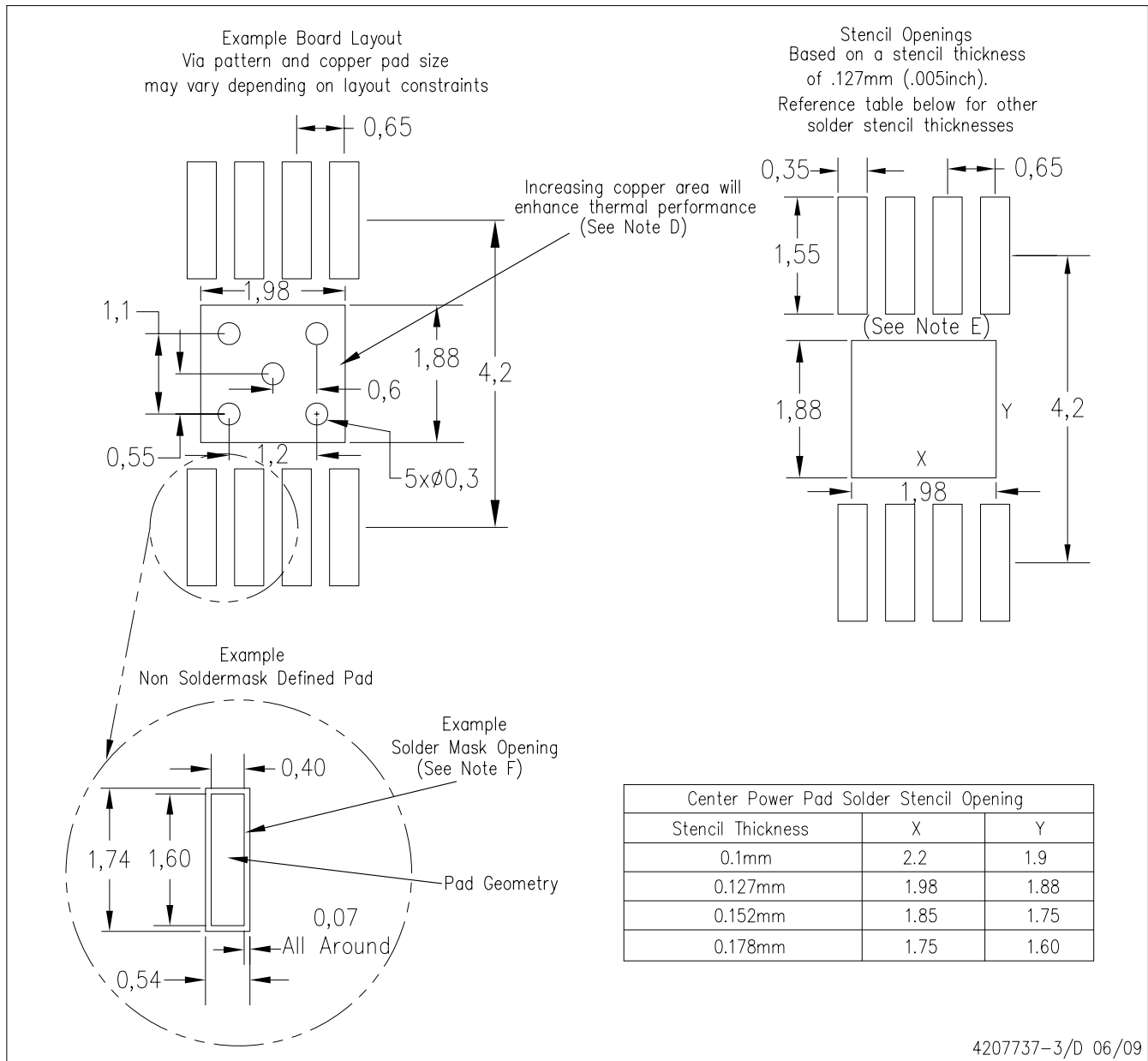
The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DGN (R-PDSO-G8) PowerPAD™



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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