

## BICMOS ADVANCED PHASE-SHIFT PWM CONTROLLER

### FEATURES

- Programmable Output Turn-on Delay
- Adaptive Delay Set
- Bidirectional Oscillator Synchronization
- Voltage-Mode, Peak Current-Mode, or Average Current-Mode Control
- Programmable Softstart/Softstop and Chip Disable via a Single Pin
- 0% to 100% Duty-Cycle Control
- 7-MHz Error Amplifier
- Operation to 1 MHz
- Typical 5-mA Operating Current at 500 kHz
- Very Low 150- $\mu$ A Current During UVLO

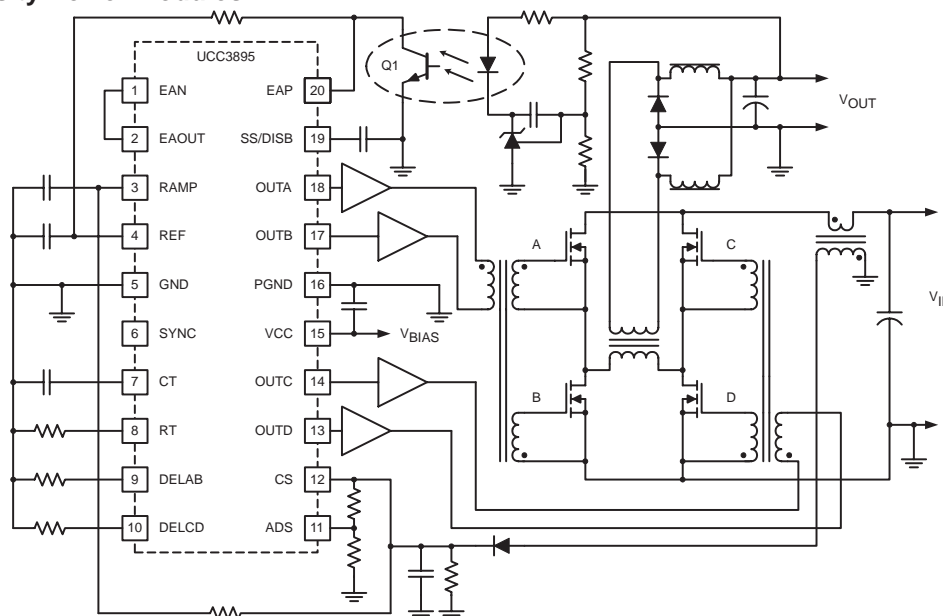
### DESCRIPTION

The UCC3895 is a phase-shift PWM controller that implements control of a full-bridge power stage by phase shifting the switching of one half-bridge with respect to the other. It allows constant frequency pulse-width modulation in conjunction with resonant zero-voltage switching to provide high efficiency at high frequencies. The part can be used either as a voltage-mode or current-mode controller.

While the UCC3895 maintains the functionality of the UC3875/6/7/8 family and UC3879, it improves on that controller family with additional features such as enhanced control logic, adaptive delay set, and shutdown capability. Since it is built using the BCDMOS process, it operates with dramatically less supply current than its bipolar counterparts. The UCC3895 can operate with a maximum clock frequency of 1 MHz.

### APPLICATIONS

- Phase-Shifted Full-Bridge Converters
- Off-Line, Telecom, Datacom and Servers
- Distributed Power Architecture
- High-Density Power Modules



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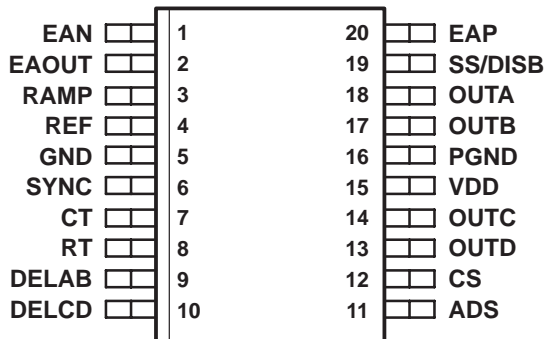
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**ORDERING INFORMATION**

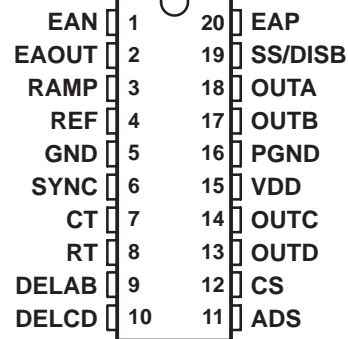
| T <sub>A</sub> | PACKAGED DEVICES           |            |                     |                           |            |            |
|----------------|----------------------------|------------|---------------------|---------------------------|------------|------------|
|                | SOIC–20(DW) <sup>(1)</sup> | PDIP–20(N) | TSSOP–20(PW)<br>(1) | PLCC–20(Q) <sup>(1)</sup> | CLCC–20(L) | CDIP–20(J) |
| –55°C to 125°C |                            |            |                     |                           | UCC1895L   | UCC1895J   |
| –40°C to 85°C  | UCC2895DW                  | UCC2895N   | UCC2895PW           | UCC2895Q                  |            |            |
| 0°C to 70°C    | UCC3895DW                  | UCC3895N   | UCC3895PW           | UCC3895Q                  |            |            |

(1) The DW, PW and Q packages are available taped and reeled. Add TR suffix to device type (e.g. UCC2895DWTR) to order quantities of 2000 devices per reel for DW.

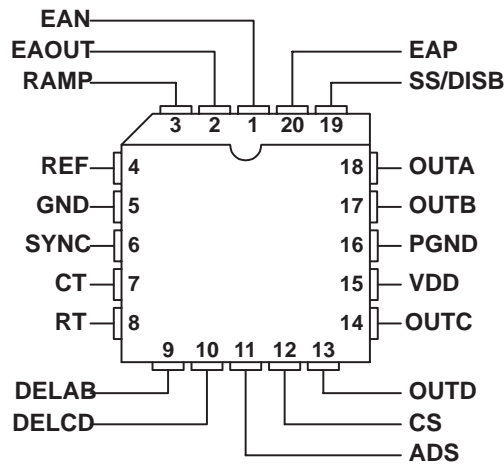
**PW and DW PACKAGE  
(TOP VIEW)**



**N and J PACKAGE  
(TOP VIEW)**



**Q and L PACKAGE  
(TOP VIEW)**



## ABSOLUTE MAXIMUM RATINGS

–40°C ≤ T<sub>A</sub> ≤ 85°C, all voltage values are with respect to the network ground terminal unless otherwise noted. (2)

|  |   | UCC2895N              | UNIT |
|--|---|-----------------------|------|
| Supply voltage   | (I <sub>DD</sub> < 10 mA)                     | 17                    | V    |
| Supply current   |   | 30                    | mA   |
| Reference current  |   | 15                    |      |
| Output current   |   | 100                   |      |
| Analog inputs  | EAP, EAN, EAOUT, RAMP, SYNC, ADS, CS, SS/DISB | –0.3 V to REF+0.3 V   | V    |
| Drive outputs  | OUTA, OUTB, OUTC, OUTD                        | –0.3 V to VCC + 0.3 V |      |
| Power dissipation at T <sub>A</sub> = 25°C                   | DW–20 package                                 | 650                   | mW   |
|  | N–20 package                                  | 1                     | W    |
| Storage temperature range, T <sub>stg</sub>                  |   | –65 to 150            | °C   |
| Junction temperature range, T <sub>J</sub>                   |   | –55 to 150            |      |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |   | 300                   |      |

(2) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability

## RECOMMENDED OPERATING CONDITIONS

|  | MIN | TYP | MAX  | UNIT |
|--|-----|-----|------|------|
| Supply voltage, V <sub>DD</sub>                                    | 9   |     | 17   | V    |
| Supply voltage bypass capacitor, V <sub>DD</sub>                   |     | 0.1 |      | μF   |
| Reference bypass capacitor, C <sub>REF</sub>                       |     | 0.1 | 0.47 |      |
| Timing capacitor, C <sub>T</sub> (for 500 kHz switching frequency) |     | 220 |      | pF   |
| Timing resistor, R <sub>T</sub> (for 500 kHz switching frequency)  |     | 82  |      | kΩ   |
| Delay resistor R <sub>DEL_AB</sub> , R <sub>DEL_CD</sub>           | 2.5 |     | 40   | pF   |
| Operating junction temperature, T <sub>J</sub> (3)                 | –55 |     | 125  | °C   |

(3) It is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

**ELECTRICAL CHARACTERISTICS**  $V_{DD} = 12\text{ V}$ ,  $R_T = 82\text{ k}\Omega$ ,  $C_T = 220\text{ pF}$ ,  $R_{DELAB} = 10\text{ k}\Omega$ ,  $R_{DELCD} = 10\text{ k}\Omega$ ,  $C_{REF} = 0.1\text{ }\mu\text{F}$ ,  $C_{VDD} = 0.1\text{ }\mu\text{F}$  and no load on the outputs,  $T_A = T_J$ .  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  for UCC3895x,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  for UCC2895x and  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$  for the UCC1895x. (unless otherwise noted)

| PARAMETER                          |  | TEST CONDITIONS   | MIN   | TYP  | MAX   | UNITS            |
|------------------------------------|--|---|-------|------|-------|------------------|
| <b>UVLO (UNDERVOLTAGE LOCKOUT)</b> |  |   |       |      |       |                  |
| UVLO <sub>(on)</sub>               | Start-up voltage threshold               |   | 10.2  | 11   | 11.8  | V                |
| UVLO <sub>(off)</sub>              | Minimum operating voltage after start-up |   | 8.2   | 9    | 9.8   |                  |
| UVLO <sub>(hys)</sub>              | Hysteresis                               |   | 1.0   | 2.0  | 3.0   |                  |
| <b>SUPPLY</b>                      |  |   |       |      |       |                  |
| I <sub>START</sub>                 | Start-up current                         | $V_{DD} = 8\text{ V}$   |       | 150  | 250   | $\mu\text{A}$    |
| I <sub>DD</sub>                    | Operating current                        |   |       | 5    | 6     | mA               |
| V <sub>DD_CLAMP</sub>              | V <sub>DD</sub> clamp voltage            | I <sub>DD</sub> = 10 mA   | 16.5  | 17.5 | 18.5  | V                |
| <b>VOLTAGE REFERENCE</b>           |  |   |       |      |       |                  |
| V <sub>REF</sub>                   | Output voltage                           | $T_J = 25^\circ\text{C}$  | 4.94  | 5.00 | 5.06  | V                |
|                                    |  | $10\text{ V} < V_{DD} < V_{DD\_CLAMP}$ ,<br>$0\text{ mA} < I_{REF} < 5\text{ mA}$ ,<br>temperature    | 4.85  | 5    | 5.15  |                  |
| I <sub>SC</sub>                    | Short circuit current                    | REF = 0 V, $T_J = 25^\circ\text{C}$   | 10    | 20   |       | mA               |
| <b>ERROR AMPLIFIER</b>             |  |   |       |      |       |                  |
| CMRR                               | Common-mode input voltage range          |   | -0.1  |      | 3.6   | V                |
| V <sub>IO</sub>                    | Offset voltage                           |   | -7    |      | 7     | mV               |
| I <sub>BIAS</sub>                  | Input bias current (EAP, EAN)            |   | -1    |      | 1     | $\mu\text{A}$    |
| EAOUT <sub>_VOH</sub>              | High-level output voltage                | EAP-EAN = 500 mV, I <sub>EAOUT</sub> = -0.5 mA  | 4.0   | 4.5  | 5.0   | V                |
| EAOUT <sub>_VOL</sub>              | Low-level output voltage                 | EAP-EAN = -500 mV, I <sub>EAOUT</sub> = 0.5 mA  | 0     | 0.2  | 0.4   |                  |
| I <sub>SOURCE</sub>                | Error amplifier output source current    | EAP-EAN = 500 mV, EAOUT = 2.5 V   | 1.0   | 1.5  |       | mA               |
| I <sub>SINK</sub>                  | Error amplifier output sink current      | EAP-EAN = -500 mV, EAOUT = 2.5 V  | 2.5   | 4.5  |       |                  |
| A <sub>VOL</sub>                   | Open-loop dc gain                        |   | 75    | 85   |       | dB               |
| GBW                                | Unity gain bandwidth <sup>(1)</sup>      |   | 5.0   | 7.0  |       | MHz              |
|                                    | Slew rate <sup>(1)</sup>                 | $1\text{ V} < \text{EAN} < 0\text{ V}$ , EAP = 500 mV<br>$0.5\text{ V} < \text{EAOUT} < 3.0\text{ V}$ | 1.5   | 2.2  |       | V/ $\mu\text{s}$ |
|                                    | No-load comparator turn-off threshold    |   | 0.45  | 0.50 | 0.55  | V                |
|                                    | No-load comparator turn-on threshold     |   | 0.55  | 0.60 | 0.69  |                  |
|                                    | No-load comparator hysteresis            |   | 0.035 | 0.10 | 0.165 |                  |
| <b>OSCILLATOR</b>                  |  |   |       |      |       |                  |
| f <sub>OSC</sub>                   | Frequency                                | $T_J = 25^\circ\text{C}$  | 473   | 500  | 527   | kHz              |
|                                    | Frequency total variation <sup>(1)</sup> | Over line, temperature  |       | 2.5% | 5%    |                  |
| V <sub>IH_SYNC</sub>               | High-level input voltage, SYNC           |   | 2.05  | 2.10 | 2.40  | V                |
| V <sub>OH_SYNC</sub>               | High-level input voltage, SYNC           | I <sub>SYNC</sub> = -400 $\mu\text{A}$ , V <sub>CT</sub> = 2.6 V                                      | 4.1   | 4.5  | 5.0   |                  |
| V <sub>OL_SYNC</sub>               | Low-level output voltage, SYNC           | I <sub>SYNC</sub> = 100 $\mu\text{A}$ , V <sub>CT</sub> = 2.6 V                                       | 0.0   | 0.5  | 1.0   |                  |
|                                    | Sync output pulse width                  | LOAD <sub>SYNC</sub> = 3.9 k $\Omega$ and 30 pF in parallel   |       | 85   | 135   |                  |
| V <sub>RT</sub>                    | Timing resistor voltage                  |   | 2.9   | 3    | 3.1   | V                |
| V <sub>CT(peak)</sub>              | Timing capacitor peak voltage            |   | 2.25  | 2.35 | 2.55  |                  |
| V <sub>CT(valley)</sub>            | Timing capacitor valley voltage          |   | 0.0   | 0.2  | 0.4   |                  |

(1) Ensured by design. Not production tested.

**ELECTRICAL CHARACTERISTICS**  $V_{DD} = 12\text{ V}$ ,  $R_T = 82\text{ k}\Omega$ ,  $C_T = 220\text{ pF}$ ,  $R_{DELAB} = 10\text{ k}\Omega$ ,  $R_{DELCD} = 10\text{ k}\Omega$ ,  $C_{REF} = 0.1\text{ }\mu\text{F}$ ,  $C_{VDD} = 0.1\text{ }\mu\text{F}$  and no load on the outputs,  $T_A = T_J$ .  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  for UCC3895x,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  for UCC2895x and  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$  for the UCC1895x. (unless otherwise noted)

| PARAMETER                       |   | TEST CONDITIONS                                     |                                  | MIN  | TYP  | MAX  | UNITS         |
|---------------------------------|---|---|----------------------------------|------|------|------|---------------|
| <b>CURRENT SENSE</b>            |   |   |                                  |      |      |      |               |
| $I_{CS(\text{bias})}$           | Current sense bias current              | $0\text{ V} < CS < 2.5\text{ V}$ ,                  | $0\text{ V ADS} < 2.5\text{ V}$  | -4.5 |      | 20   | $\mu\text{A}$ |
|                                 | Peak current threshold                  |   |                                  | 1.90 | 2.00 | 2.10 | V             |
|                                 | Overcurrent threshold                   |   |                                  | 2.4  | 2.5  | 2.6  | V             |
|                                 | Current sense to output delay           | $0\text{V} \leq CS \leq 2.3\text{ V}$ ,             | DELAB=DELCD=REF                  |      | 75   | 110  | ns            |
| <b>SOFT-START/SHUTDOWN</b>      |   |   |                                  |      |      |      |               |
| $I_{\text{SOURCE}}$             | Softstart source current                | SS/DISB = 3.0 V,                                    | CS = 1.9 V                       | -40  | -35  | -30  | $\mu\text{A}$ |
| $I_{\text{SINK}}$               | Softstart sink current                  | SS/DISB = 3.0 V,                                    | CS = 2.6 V                       | 325  | 350  | 375  | $\mu\text{A}$ |
|                                 | Softstart/disable comparator threshold  |   |                                  | 0.44 | 0.50 | 0.56 | V             |
| <b>ADAPTIVE DELAY SET (ADS)</b> |   |   |                                  |      |      |      |               |
|                                 | DELAB/DELCD output voltage              | ADS = CS = 0 V                                      |                                  | 0.45 | 0.50 | 0.55 | V             |
|                                 |   | ADS = 0 V,  | CS = 2.0 V                       | 1.9  | 2.0  | 2.1  | V             |
| $t_{\text{DELAY}}$              | Output delay <sup>(1)(3)</sup>          | ADS = CS = 0 V                                      |                                  | 450  | 560  | 620  | ns            |
|                                 | ADS bias current                        | $0\text{ V} < ADS < 2.5\text{ V}$ ,                 | $0\text{ V} < CS < 2.5\text{ V}$ | -20  |      | 20   | $\mu\text{A}$ |
| <b>OUTPUT</b>                   |   |   |                                  |      |      |      |               |
| $V_{\text{OH}}$                 | High-level output voltage (all outputs) | $I_{\text{OUT}} = -10\text{ mA}$ ,<br>VDD to output |                                  |      | 250  | 400  | mV            |
| $V_{\text{OL}}$                 | Low-level output voltage (all outputs)  | $I_{\text{OUT}} = 10\text{ mA}$                     |                                  |      | 150  | 250  | mV            |
| $t_{\text{R}}$                  | Rise time <sup>(1)</sup>                | $C_{\text{LOAD}} = 100\text{ pF}$                   |                                  |      | 20   | 35   | ns            |
| $t_{\text{F}}$                  | Fall time <sup>(1)</sup>                | $C_{\text{LOAD}} = 100\text{ pF}$                   |                                  |      | 20   | 35   | ns            |

(1) Ensured by design. Not production tested.

(2) Minimum phase shift is defined as:

$$\Phi = 180 \times \frac{t_{\text{f(OUTC)}} - t_{\text{f(OUTA)}}}{t_{\text{PERIOD}}} \quad \text{or} \quad \Phi = 180 \times \frac{t_{\text{f(OUTC)}} - t_{\text{f(OUTB)}}}{t_{\text{PERIOD}}} \quad \text{where}$$

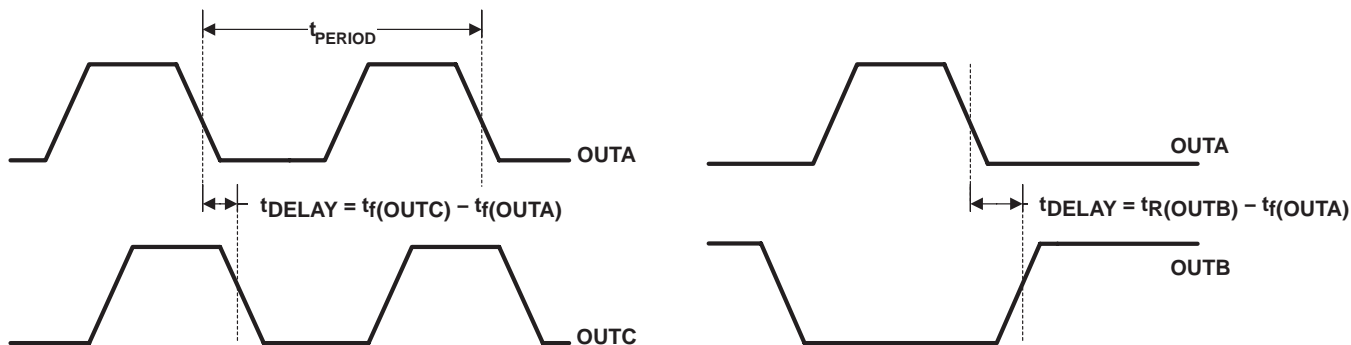
$t_{\text{f(OUTA)}}$  = falling edge of OUTA signal,  $t_{\text{f(OUTB)}}$  = falling edge of OUTB signal

$t_{\text{f(OUTC)}}$  = falling edge of OUTC signal,  $t_{\text{f(OUTD)}}$  = falling edge of OUTD signal

$t_{\text{PERIOD}}$  = period of OUTA or OUTB signal

(3) Output delay is measured between OUTA/OUTB or OUTC/OUTD. Output delay is defined as shown below where:

$t_{\text{f(OUTA)}}$  = falling edge of OUTA signal,  $t_{\text{r(OUTB)}}$  = rising edge of OUTB signal



Same applies to OUTB and OUTD

Same applies to OUTC and OUTD

# UCC1895 UCC2895 UCC3895

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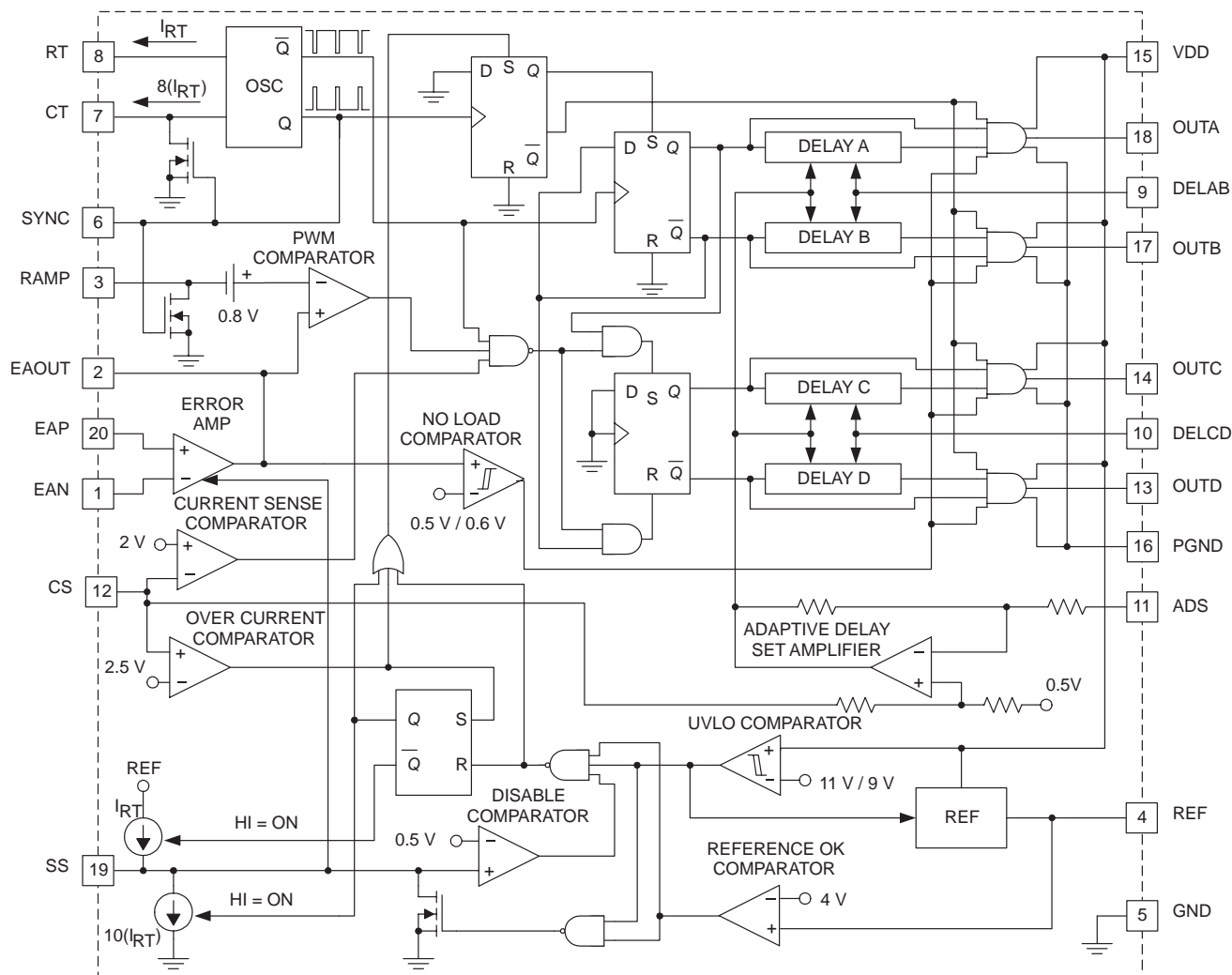
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| PARAMETER  |  | TEST CONDITIONS                                       |                 | MIN  | TYP  | MAX  | UNITS         |
|--|--|---|-----------------|------|------|------|---------------|
| <b>PWM COMPARATOR</b>  |  |   |                 |      |      |      |               |
| EAOUT to RAMP input offset voltage                                 |  | RAMP = 0 V,   | DELAB=DELCD=REF | 0.72 | 0.85 | 1.05 | V             |
| Minimum phase shift <sup>(2)</sup><br>(OUTA to OUTC, OUTB to OUTD) |  | RAMP = 0 V  | EAOUT = 650 mV  | .0%  | .85% | 1.4% |               |
| $t_{DELAY}$  | Delay <sup>(3)</sup><br>(RAMP to OUTC, RAMP to OUTD) | 0 V < RAMP < 2.5 V, EAOUT = 1.2 V,<br>DELAB=DELCD=REF |                 |      | 70   | 120  | ns            |
| $I_R(\text{bias})$   | RAMP bias current                                    | RAMP < 5 V,   | CT = 2.2 V      | -5   |      | 5    | $\mu\text{A}$ |
| $I_R(\text{sink})$   | RAMP sink current                                    | RAMP = 5 V,   | CT = 2.6 V      | 12   | 19   |      | mA            |

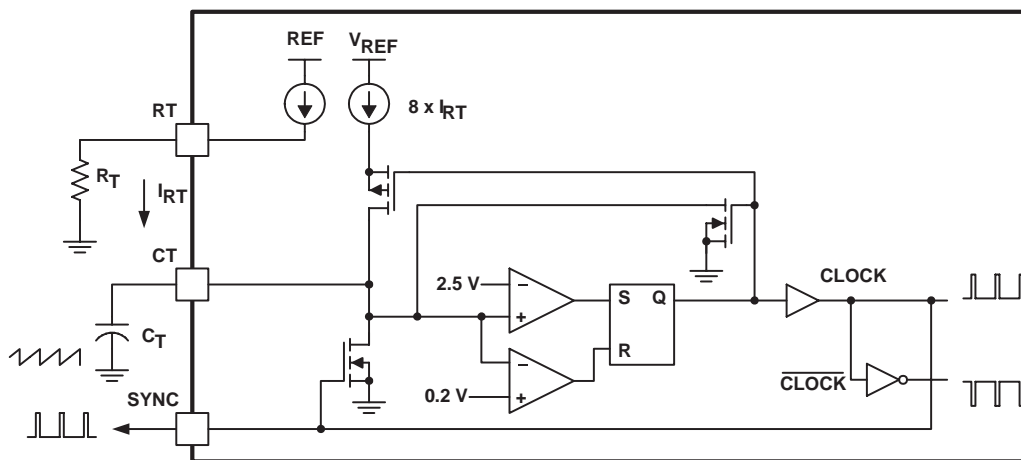
## TERMINAL FUNCTIONS

| TERMINAL NAME | NO. | I/O | DESCRIPTION  |
|---------------|-----|-----|--|
| ADS           | 11  | I   | Adaptive delay set. Sets the ratio between the maximum and minimum programmed output delay dead time.  |
| CS            | 12  | I   | Current sense input for cycle-by-cycle current limiting and for over-current comparator.   |
| CT            | 7   | I   | Oscillator timing capacitor for programming the switching frequency. The UCC3895's oscillator charges CT via a programmed current.   |
| DELAB         | 9   | I   | Delay programming between complementary outputs. DELAB programs the dead time between switching of output A and output B.  |
| DELCD         | 10  | I   | Delay programming between complementary outputs. DELCD programs the dead time between switching of output C and output D.  |
| EAOUT         | 2   | I/O | Error amplifier output   |
| EAP           | 20  | I   | Non-inverting input to the error amplifier   |
| EAN           | 1   | I   | Inverting input to the error amplifier   |
| GND           | 5   | -   | Chip ground for all circuits except the output stages  |
| OUTA          | 18  | O   | The four outputs are 100-mA complementary MOS drivers, and are optimized to drive FET driver circuits such as UCC27424 or gate drive transformers.   |
| OUTB          | 17  | O   |  |
| OUTC          | 14  | O   |  |
| OUTD          | 13  | O   |  |
| PGND          | 16  | -   | Output stage ground  |
| RAMP          | 3   | I   | Inverting input of the PWM comparator  |
| REF           | 4   | O   | 5 V, $\pm 1.2\%$ , 5 mA voltage reference. For best performance, bypass with a 0.1- $\mu\text{F}$ low ESR, low ESL capacitor to ground. Do not use more than 1.0 $\mu\text{F}$ of total capacitance on this pin. |
| RT            | 8   | I   | Oscillator timing resistor for programming the switching frequency   |
| SS/DISB       | 19  | I   | Soft-start/disable. This pin combines the two independent functions.   |
| SYNC          | 6   | I/O | Oscillator synchronization. This pin is bidirectional.   |
| VDD           | 15  | I   | Power supply input pin. VDD must be bypassed with a minimum of a 1.0- $\mu\text{F}$ low ESR, low ESL capacitor to ground.  |

**BLOCK DIAGRAM**

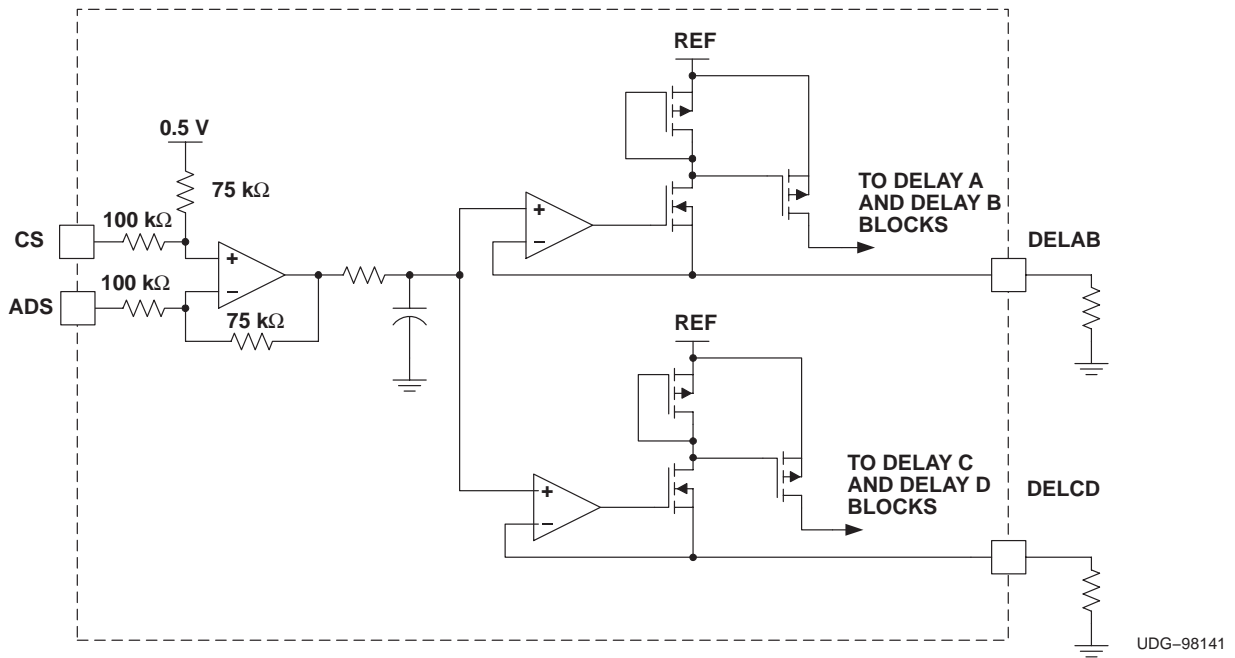


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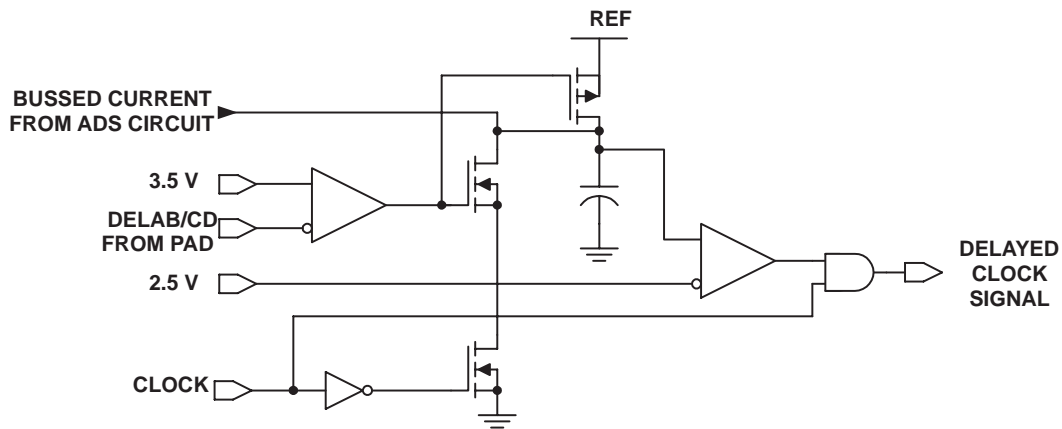


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**Figure 1. Oscillator Block Diagram**



**Figure 2. Adaptive Delay Set Block Diagram**



**Figure 3. Delay Block Diagram (One Delay Block Per Outlet)**



## DETAILED PIN DESCRIPTION

### Adaptive Delay Set (ADS)

This function sets the ratio between the maximum and minimum programmed output-delay dead time. When the ADS pin is directly connected to the CS pin, no delay modulation occurs. The maximum delay modulation occurs when ADS is grounded. In this case, delay time is four times longer when CS = 0 than when CS = 2.0 V (the peak-current threshold), ADS changes the output voltage on the delay pins DELAB and DELCD by the following formula:

$$V_{\text{DEL}} = \left[ 0.75 \times (V_{\text{CS}} - V_{\text{ADS}}) \right] + 0.5 \text{ V} \quad (1)$$

where  $V_{\text{CS}}$  and  $V_{\text{ADS}}$  are in volts. ADS must be limited to between 0 V and 2.5 V and must be less than or equal to CS. DELAB and DELCD are clamped to a minimum of 0.5 V.

### Current Sense (CS)

The inverting input of the current-sense comparator and the non-inverting input of the overcurrent comparator and the ADS amplifier. The current sense signal is used for cycle-by-cycle current limiting in peak current mode control, and for overcurrent protection in all cases with a secondary threshold for output shutdown. An output disable initiated by an overcurrent fault also results in a restart cycle, called *soft stop*, with full soft start.

### Oscillator Timing Capacitor (CT)

The UCC3895's oscillator charges CT via a programmed current. The waveform on  $C_T$  is a sawtooth, with a peak voltage of 2.35 V. The approximate oscillator period is calculated by the following formula:

$$t_{\text{OSC}} = \frac{5 \times R_T \times C_T}{48} + 120 \text{ ns} \quad (2)$$

where  $C_T$  is in Farads, and  $R_T$  is in Ohms and  $t_{\text{OSC}}$  is in seconds.  $C_T$  can range from 100 pF to 880 pF.

**NOTE:** A large  $C_T$  and a small  $R_T$  combination results in extended fall times on the  $C_T$  waveform. The increased fall time increases the SYNC pulse width, hence limiting the maximum phase shift between OUTA, OUTB and OUTC, OUTD outputs, which limits the maximum duty cycle of the converter. (Refer to Figure 1)

### Delay Programming Between Complementary Outputs (DELAB, DELCD)

DELAB programs the dead time between switching of OUTA and OUTB, and DELCD programs the dead time between OUTC and OUTD. This delay is introduced between complementary outputs in the same leg of the external bridge. The UCC2895N allows the user to select the delay, in which the resonant switching of the external power stages takes place. Separate delays are provided for the two half-bridges to accommodate differences in resonant-capacitor charging currents. The delay in each stage is set according to the following formula:

$$t_{\text{DELAY}} = \frac{(25 \times 10^{-12}) \times R_{\text{DEL}}}{V_{\text{DEL}}} + 25 \text{ ns} \quad (3)$$

where  $V_{\text{DEL}}$  (V), and  $R_{\text{DEL}}$  is in ( $\Omega$ ) and  $t_{\text{DELAY}}$  is in seconds. DELAB and DELCD can source about 1 mA maximum. Choose the delay resistors so that this maximum is not exceeded. Programmable output delay is defeated by tying DELAB and/or DELCD to REF. For an optimum performance keep stray capacitance on these pins at less than 10 pF.

## DETAILED PIN DESCRIPTION (continued)

### Error Amplifier (EAOUT), (EAP), (EAN)

EAOUT connected internally to the non-inverting input of the PWM comparator and the no-load comparator. EAOUT is internally clamped to the soft-start voltage. The no-load comparator shuts down the output stages when EAOUT falls below 500 mV, and allows the outputs to turn on again when EAOUT rises above 600 mV.

EAP is the non-inverting and the EAN is the inverting input to the error amplifier.

### Output MOSFET Drivers (OUTA, OUTB, OUTC, OUTD)

The 4 outputs are 100-mA complementary MOS drivers, and are optimized to drive MOSFET driver circuits. OUTA and OUTB are fully complementary, (assuming no programming delay). They operate near 50% duty cycle and one-half the oscillator frequency. OUTA and OUTB are intended to drive one half-bridge circuit in an external power stage. OUTC and OUTD drive the other half-bridge and have the same characteristics as OUTA and OUTB. OUTC is phase shifted with respect to OUTA, and OUTD is phase shifted with respect to OUTB.

**NOTE:** Changing the phase relationship of OUTC and OUTD with respect to OUTA and OUTB requires other than the nominal 50% duty ratio on OUTC and OUTD during those transients.

### Power Ground (PGND)

To keep output switching noise from critical analog circuits, the UCC3895 has two different ground connections. PGND is the ground connection for the high-current output stages. Both GND and PGND must be electrically tied together. Also, since PGND carries high current, board traces must be low impedance.

### Inverting Input of the PWM Comparator (RAMP)

This pin receives either the  $C_T$  waveform in voltage and average current-mode controls, or the current signal (plus slope compensation) in peak current-mode control.

### Voltage Reference (REF)

The 5 V,  $\pm 1.2\%$  reference supplies power to internal circuitry, and can also supply up to 5 mA to external loads. The reference is shut down during undervoltage lockout but is operational during all other disable modes. For best performance, bypass with a 0.1- $\mu$ F, low-ESR, low-ESL capacitor to GND. Do not use more than 1.0  $\mu$ F of total capacitance on this pin. To ensure the stability of the internal reference.

### Oscillator Timing Resistor (RT)

The oscillator in the UCC3895 operates by charging an external timing capacitor,  $C_T$ , with a fixed current programmed by  $R_T$ .  $R_T$  current is calculated as follows:

$$I_{RT} \text{ (A)} = \frac{3.0 \text{ V}}{R_T \text{ } (\Omega)} \quad (4)$$

$R_T$  can range from 40 k $\Omega$  to 120 k $\Omega$ . Soft-start charging and discharging currents are also programmed by  $I_{RT}$  (Refer to Figure 1).

### Analog Ground (GND)

This pin is the chip ground for all internal circuits except the output stages.

---

## DETAILED PIN DESCRIPTION (continued)

### Soft-Start/Disable (SS/DISB)

This pin combines two independent functions.

**Disable Mode:** A rapid shutdown of the chip is accomplished by externally forcing SS/DISB below 0.5 V, externally forcing REF below 4 V, or if VDD drops below the undervoltage lockout threshold. In the case of REF being pulled below 4 V or an undervoltage condition, SS/DISB is actively pulled to ground via an internal MOSFET switch.

If an overcurrent fault is sensed ( $CS = 2.5\text{ V}$ ), a *soft-stop* is initiated. In this mode, SS/DISB sinks a constant current of  $(10 \times I_{RT})$ . The soft-stop continues until SS/DISB falls below 0.5 V. When any of these faults are detected, all outputs are forced to ground immediately.

**NOTE:** If SS/DISB is forced below 0.5 V, the pin starts to source current equal to  $I_{RT}$ . The only time the part switches into low  $I_{DD}$  current mode, though, is when the part is in undervoltage lockout.

**Soft-start Mode:** After a fault or disable condition has passed, VDD is above the start threshold, and/or SS/DISB falls below 0.5 V during a soft-stop, SS/DISB switches to a soft-start mode. The pin then sources current, equal to  $I_{RT}$ . A user-selected resistor/capacitor combination on SS/DISB determines the soft start time constant.

**NOTE:** SS/DISB actively clamps the EAOUT pin voltage to approximately the SS/DISB pin voltage during both soft-start, soft-stop, and disable conditions.

### Oscillator Synchronization (SYNC)

This pin is bidirectional (refer to Figure 1). When used as an output, SYNC can be used as a clock, which is the same as the device's internal clock. When used as an input, SYNC overrides the chip's internal oscillator and act as it's clock signal. This bidirectional feature allows synchronization of multiple power supplies. Also, the SYNC signal internally discharge the  $C_T$  capacitor and any filter capacitors that are present on the RAMP pin. The internal SYNC circuitry is level sensitive, with an input-low threshold of 1.9 V, and an input-high threshold of 2.1 V. A resistor as small as 3.9 k $\Omega$  may be tied between SYNC and GND to reduce the sync pulse width.

### Chip Supply (VDD)

This is the input pin to the chip. VDD must be bypassed with a minimum of 1.0  $\mu\text{F}$  low ESR, low ESL capacitor to ground.

**APPLICATION INFORMATION**

**Programming DELAB, DELCD and the Adaptive Delay Set**

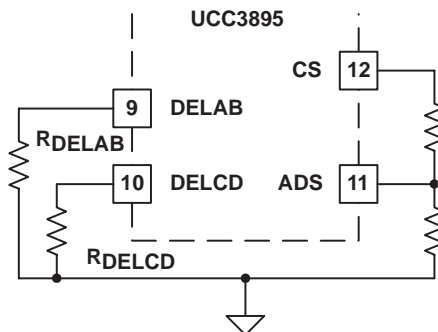
The UCC2895N allows the user to set the delay between switch commands within each leg of the full-bridge power circuit according to equations:

$$t_{\text{DELAY}} = \frac{(25 \times 10^{-12}) \times R_{\text{DEL}}}{V_{\text{DEL}}} + 25 \text{ ns} \tag{5}$$

From this equation  $V_{\text{DEL}}$  is determined in conjunction with the desire to use (or not) the adaptive delay set feature from the following formula:

$$V_{\text{DEL}} = [0.75 \times (V_{\text{CS}} - V_{\text{ADS}})] + 0.5 \text{ V} \tag{6}$$

The following diagram illustrates the resistors needed to program the delay periods and the adaptive delay set function.



**Figure 4. Programming Adaptive Delay Set**

The adaptive delay set feature (ADS) allows the user to vary the delay times between switch commands within each of the converter’s two legs. The delay-time modulation is implemented by connecting ADS (pin 11) to CS, GND, or a resistive divider from CS through ADS to GND to set  $V_{\text{ADS}}$  as shown in Figure 1. From equation (5) for  $V_{\text{DEL}}$ , if ADS is tied to GND then  $V_{\text{DEL}}$  rises in direct proportion to  $V_{\text{CS}}$ , causing a decrease in  $t_{\text{DELAY}}$  as the load increases. In this condition, the maximum value of  $V_{\text{DEL}}$  is 2 V.

If ADS is connected to a resistive divider between CS and GND, the term  $(V_{\text{CS}} - V_{\text{ADS}})$  becomes smaller, reducing the level of  $V_{\text{DEL}}$ . This decreases the amount of delay modulation. In the limit of ADS tied to CS,  $V_{\text{DEL}} = 0.5 \text{ V}$  and no delay modulation occurs. Figure 5 graphically shows the delay time vs. load for varying adaptive delay set feature voltages ( $V_{\text{ADS}}$ ).

In the case of maximum delay modulation (ADS=GND), when the circuit goes from light load to heavy load, the variation of  $V_{\text{DEL}}$  is from 0.5 V to 2 V. This causes the delay times to vary by a 4:1 ratio as the load is changed.

The ability to program an adaptive delay is a desirable feature because the optimum delay time is a function of the current flowing in the primary winding of the transformer, and can change by a factor of 10:1 or more as circuit loading changes. Reference[5] describes the many interrelated factors for choosing the optimum delay times for the most efficient power conversion, and illustrates an external circuit to enable adaptive delay set using the UC3879. Implementing this adaptive feature is simplified in the UCC3895 controller, giving the user the ability to tailor the delay times to suit a particular application with a minimum of external parts.

APPLICATION INFORMATION

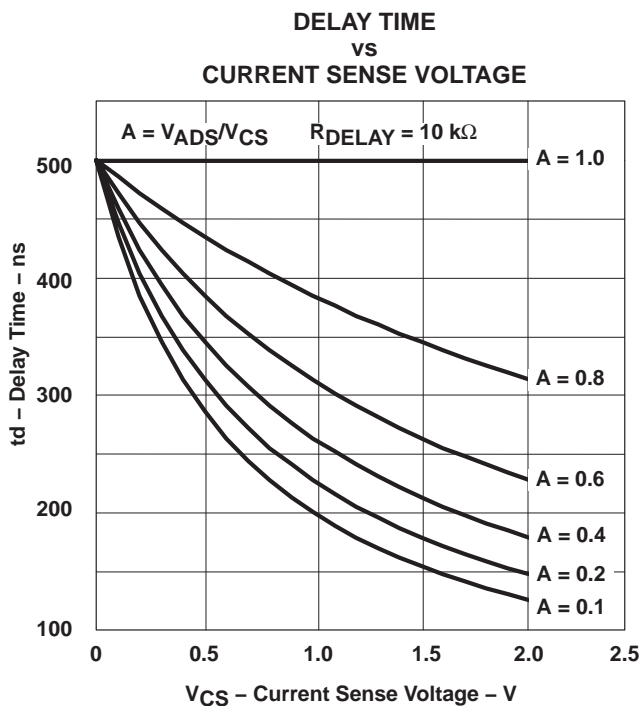


Figure 5. Delay Time Under Varying ADS Voltages

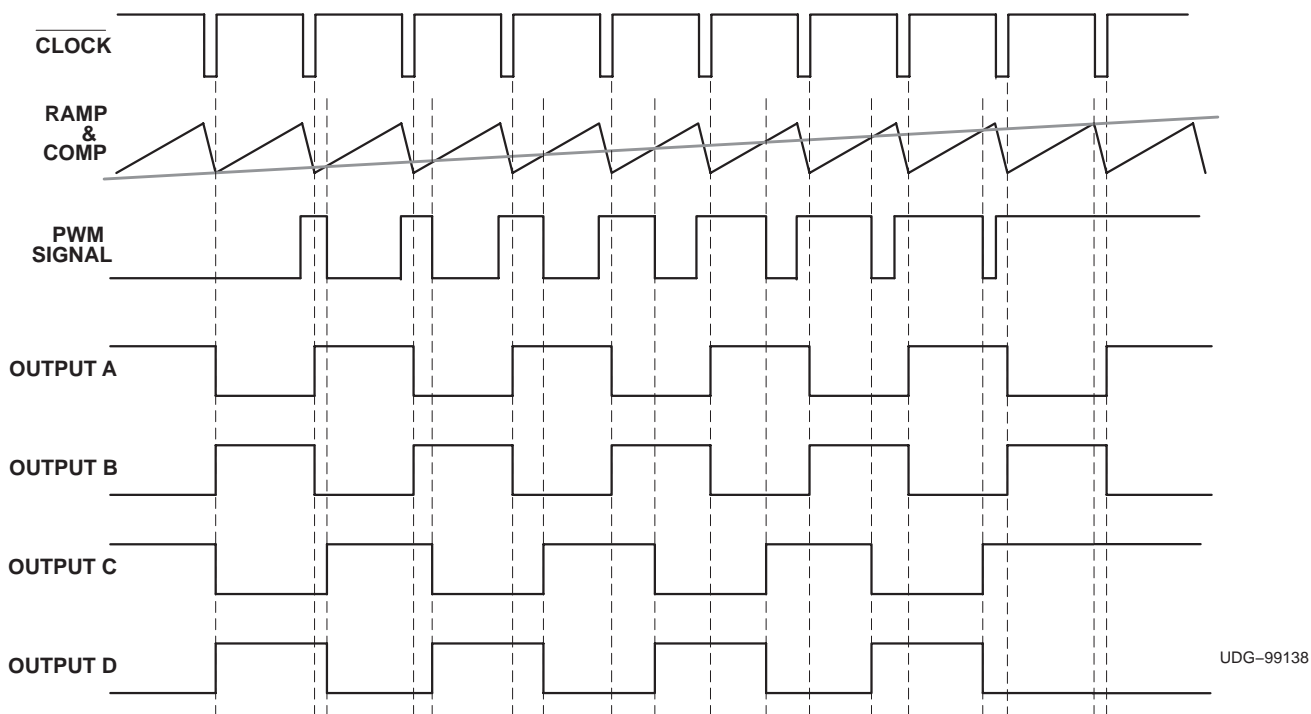


Figure 6. UCC3895 Timing Diagram (No Output Delay Shown, COMP to RAMP offset not included)

TYPICAL CHARACTERISTICS

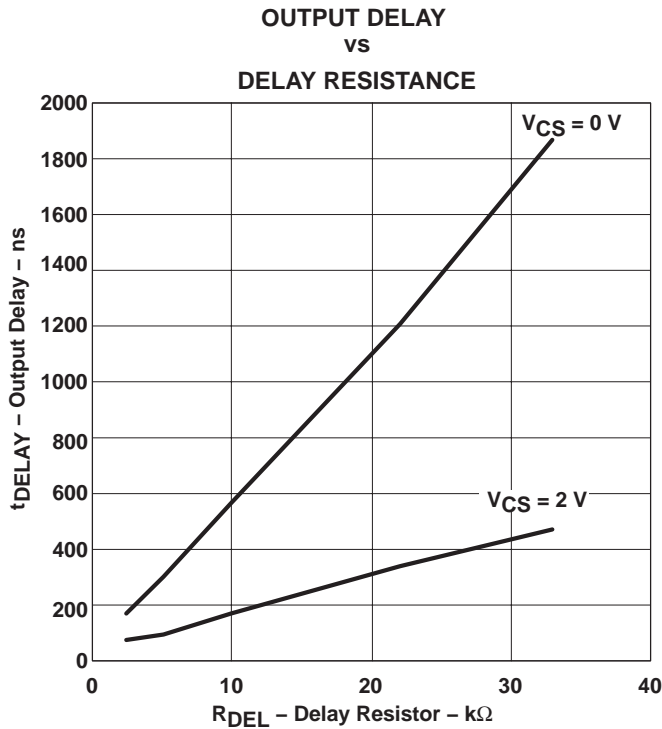


Figure 7

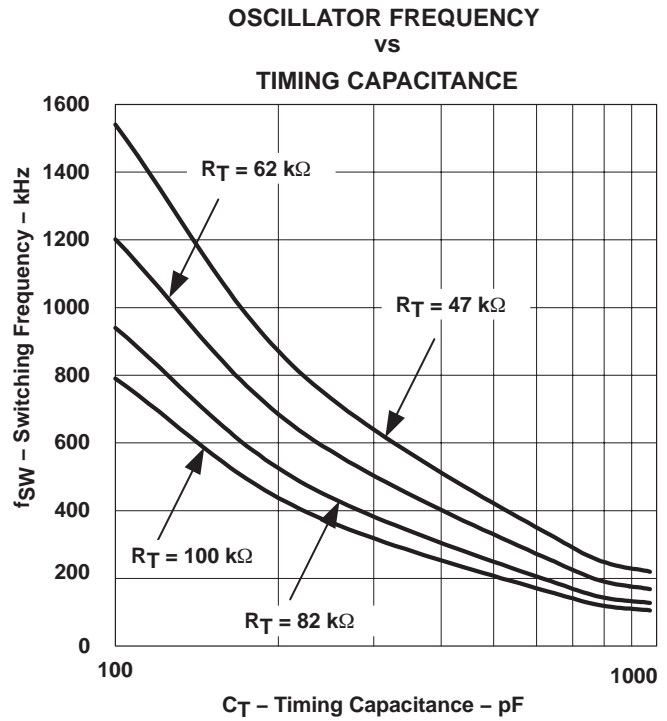


Figure 8

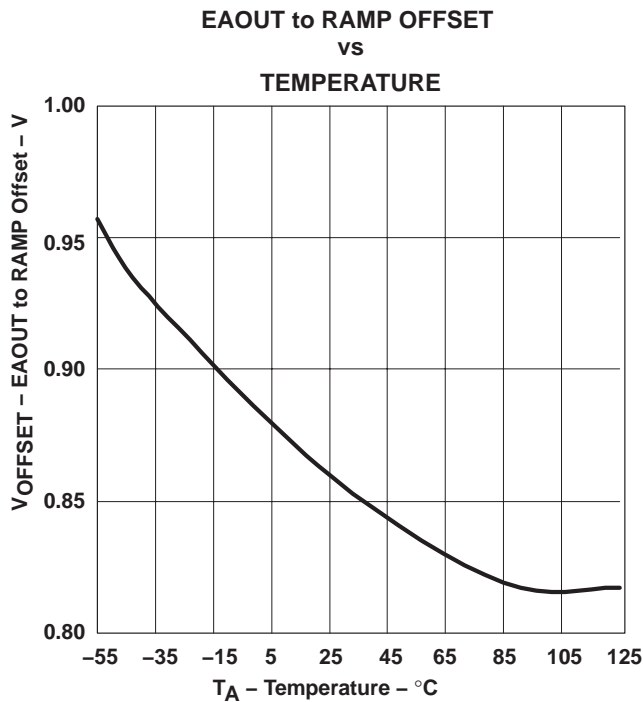


Figure 9

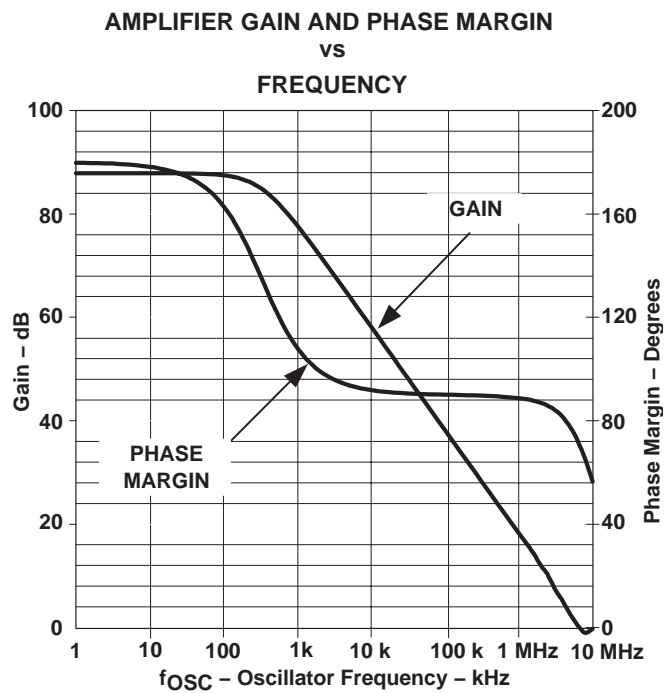


Figure 10

TYPICAL CHARACTERISTICS

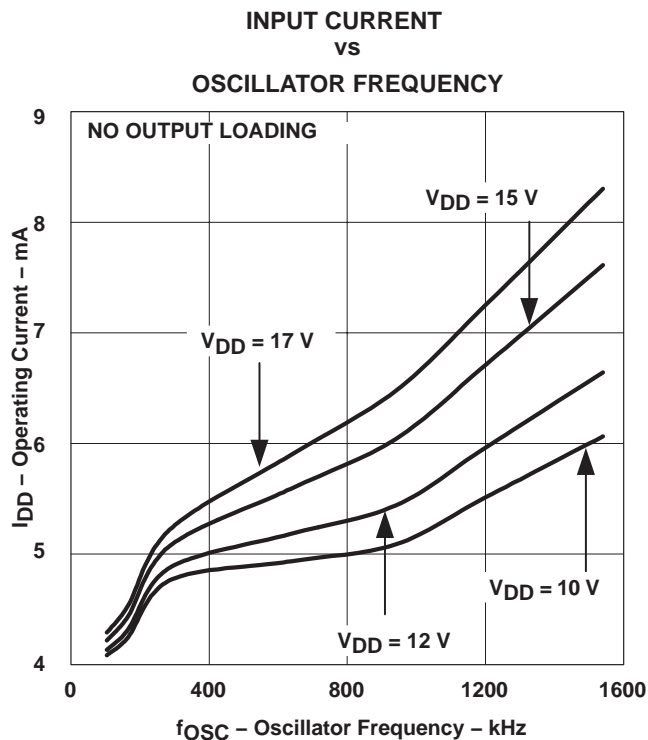


Figure 11

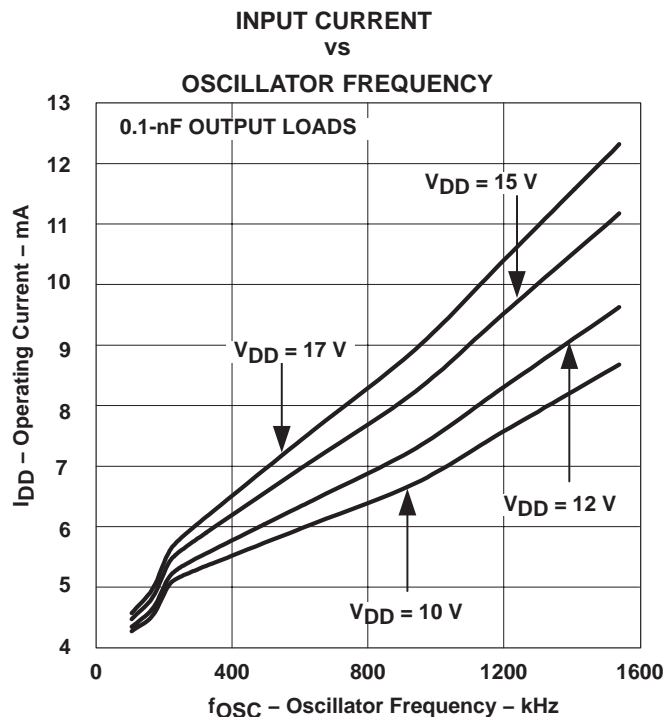


Figure 12

REFERENCES

1. M. Dennis, *A Comparison Between the BiCMOS UCC3895 Phase Shift Controller and the UC3875* Application Note (SLUA246).
2. L. Balogh, *The Current-Doubler Rectifier: An Alternative Rectification Technique for Push-Pull and Bridge Converters* Application Note (SLUA121).
3. W. Andreyca, *Phase Shifted, Zero Voltage Transition Design Considerations*, Application Note (SLUA107).
4. L. Balogh, *The New UC3879 Phase Shifted PWM Controller Simplifies the Design of Zero Voltage Transition Full-Bridge Converters*, Application Note (SLUA122).
5. L. Balogh, *Design Review: 100 W, 400 kHz, dc-to-dc Converter with Current Doubler Synchronous Rectification Achieves 92% Efficiency*, Unitrode Power Supply Design Seminar Manual, SEM-1100, 1996, Topic 2.
6. UC3875 Phase Shift Resonant Controller, Datasheet, (SLUS229).
7. UC3879 Phase Shift Resonant Controller, Datasheet, (SLUS230).
8. UCC3895EVM-1, "Configuring the UCC3895 for direct Control Driven Synchronous Rectification, (Texas Instrument's Literature Number SLUU109A)
9. UCC3895, CD Output Asymmetrical Duty Cycle Operation, (Texas Instrument's Literature Number SLUA275)
10. Texas Instrument's Literature Number SLUA323
11. Synchronous Rectifiers of a Current Doubler, (Texas Instrument's Literature Number SLUA287)

**UCC1895**  
**UCC2895**  
**UCC3895**

SLUS1571 – DECEMBER 1999 – REVISED MARCH 2007

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**REVISION TABLE**

| DATE         | REVISION | CHANGES   |
|--------------|----------|---|
| October 2005 | C        | <ol style="list-style-type: none"><li>1. Modified SYNC VIH max spec from 2.25 to 2.4 V per PCN20040113000.</li><li>2. Modified CT peak voltage max spec from 2.5 V to 2.55 V per PCN20040113000.</li><li>3. Modified output delay max spec from 600 ns to 620 ns per PCN20040113000.</li><li>4. Added upper recommended VREF capacitance of 0.47 <math>\mu</math>F.</li><li>5. Changed absolute maximum junction temperature upper limit to 150°C.</li><li>6. Changed VREF output voltage test condition to say <math>10\text{ V} &lt; V_{DD} &lt; V_{DD\_CLAMP}</math> instead of <math>10\text{ V} &lt; V_{DD} &lt; 17.5\text{ V}</math></li><li>7. Modified UCC3895 timing diagram (<u>CLOCK</u>).</li></ol> |
|              |          |   |



**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| UCC1895J         | ACTIVE                | CDIP         | J               | 20   | 1           | TBD                     | A42 SNPB         | N / A for Pkg Type           |
| UCC1895L         | ACTIVE                | LCCC         | FK              | 20   | 1           | TBD                     | POST-PLATE       | N / A for Pkg Type           |
| UCC2895DW        | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC2895DWG4      | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC2895DWTR      | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC2895DWTRG4    | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC2895N         | ACTIVE                | PDIP         | N               | 20   | 20          | Green (RoHS & no Sb/Br) | CU NIPDAU        | N / A for Pkg Type           |
| UCC2895NG4       | ACTIVE                | PDIP         | N               | 20   | 20          | Green (RoHS & no Sb/Br) | CU NIPDAU        | N / A for Pkg Type           |
| UCC2895PW        | ACTIVE                | TSSOP        | PW              | 20   | 70          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC2895PWG4      | ACTIVE                | TSSOP        | PW              | 20   | 70          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC2895PWTR      | ACTIVE                | TSSOP        | PW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC2895PWTRG4    | ACTIVE                | TSSOP        | PW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC2895Q         | ACTIVE                | PLCC         | FN              | 20   | 46          | Green (RoHS & no Sb/Br) | CU SN            | Level-2-260C-1 YEAR          |
| UCC2895QG3       | ACTIVE                | PLCC         | FN              | 20   | 46          | Green (RoHS & no Sb/Br) | CU SN            | Level-2-260C-1 YEAR          |
| UCC3895DW        | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC3895DWG4      | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC3895DWTR      | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC3895DWTRG4    | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC3895N         | ACTIVE                | PDIP         | N               | 20   | 20          | Green (RoHS & no Sb/Br) | CU NIPDAU        | N / A for Pkg Type           |
| UCC3895NG4       | ACTIVE                | PDIP         | N               | 20   | 20          | Green (RoHS & no Sb/Br) | CU NIPDAU        | N / A for Pkg Type           |
| UCC3895PW        | ACTIVE                | TSSOP        | PW              | 20   | 70          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC3895PWG4      | ACTIVE                | TSSOP        | PW              | 20   | 70          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC3895PWTR      | ACTIVE                | TSSOP        | PW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC3895PWTRG4    | ACTIVE                | TSSOP        | PW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC3895Q         | ACTIVE                | PLCC         | FN              | 20   | 46          | Green (RoHS & no Sb/Br) | CU SN            | Level-2-260C-1 YEAR          |
| UCC3895QG3       | ACTIVE                | PLCC         | FN              | 20   | 46          | Green (RoHS & no Sb/Br) | CU SN            | Level-2-260C-1 YEAR          |

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
|                  |                       |              |                 |      |             | no Sb/Br)               |                  |                              |
| UCC3895QTR       | ACTIVE                | PLCC         | FN              | 20   | 1000        | Green (RoHS & no Sb/Br) | CU SN            | Level-2-260C-1 YEAR          |
| UCC3895QTRG3     | ACTIVE                | PLCC         | FN              | 20   | 1000        | Green (RoHS & no Sb/Br) | CU SN            | Level-2-260C-1 YEAR          |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

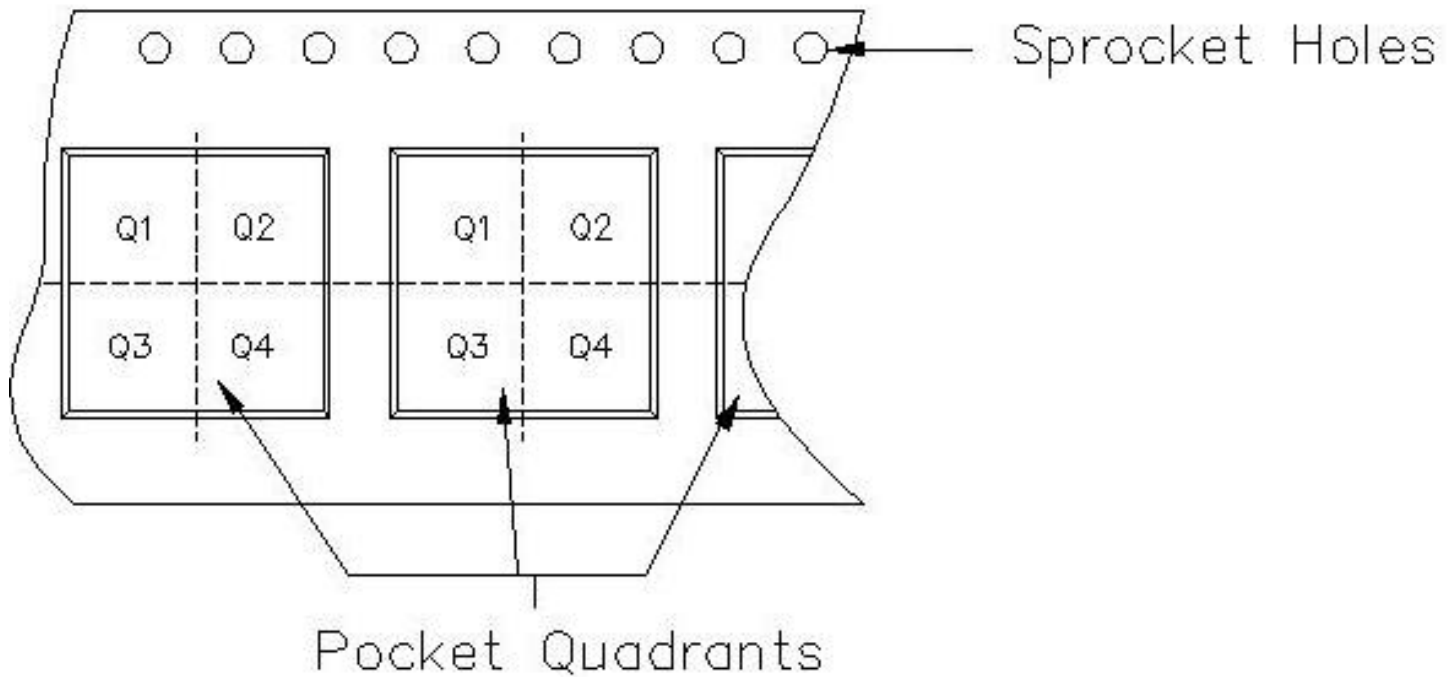
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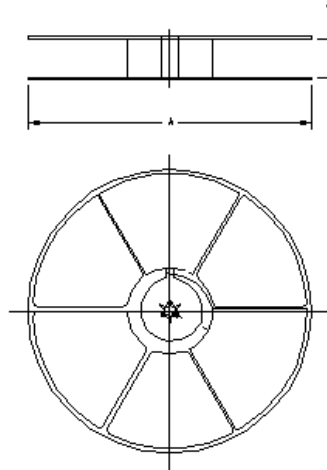
Carrier tape design is defined largely by the component length, width, and thickness.

|  |
|--|
| $A_o$ = Dimension designed to accommodate the component width.     |
| $B_o$ = Dimension designed to accommodate the component length.    |
| $K_o$ = Dimension designed to accommodate the component thickness. |
| $W$ = Overall width of the carrier tape.                           |
| $P$ = Pitch between successive cavity centers.                     |



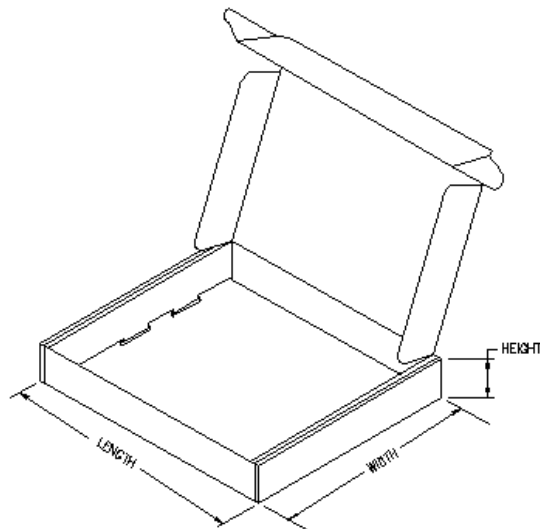
**TAPE AND REEL INFORMATION**

| Device      | Package | Pins | Site | Reel Diameter (mm) | Reel Width (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|---------|------|------|--------------------|-----------------|---------|---------|---------|---------|--------|---------------|
| UCC2895PWTR | PW      | 20   | MLA  | 330                | 16              | 6.95    | 7.1     | 1.6     | 8       | 16     | Q1            |
| UCC3895PWTR | PW      | 20   | MLA  | 330                | 16              | 6.95    | 7.1     | 1.6     | 8       | 16     | Q1            |



**TAPE AND REEL BOX INFORMATION**

| Device      | Package | Pins | Site | Length (mm) | Width (mm) | Height (mm) |
|-------------|---------|------|------|-------------|------------|-------------|
| UCC2895PWTR | PW      | 20   | MLA  | 0.0         | 0.0        | 0.0         |
| UCC3895PWTR | PW      | 20   | MLA  | 0.0         | 0.0        | 0.0         |



J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14                     | 16                     | 18                     | 20                     |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A             | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX         | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN         | —                      | —                      | —                      | —                      |
| C MAX         | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN         | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



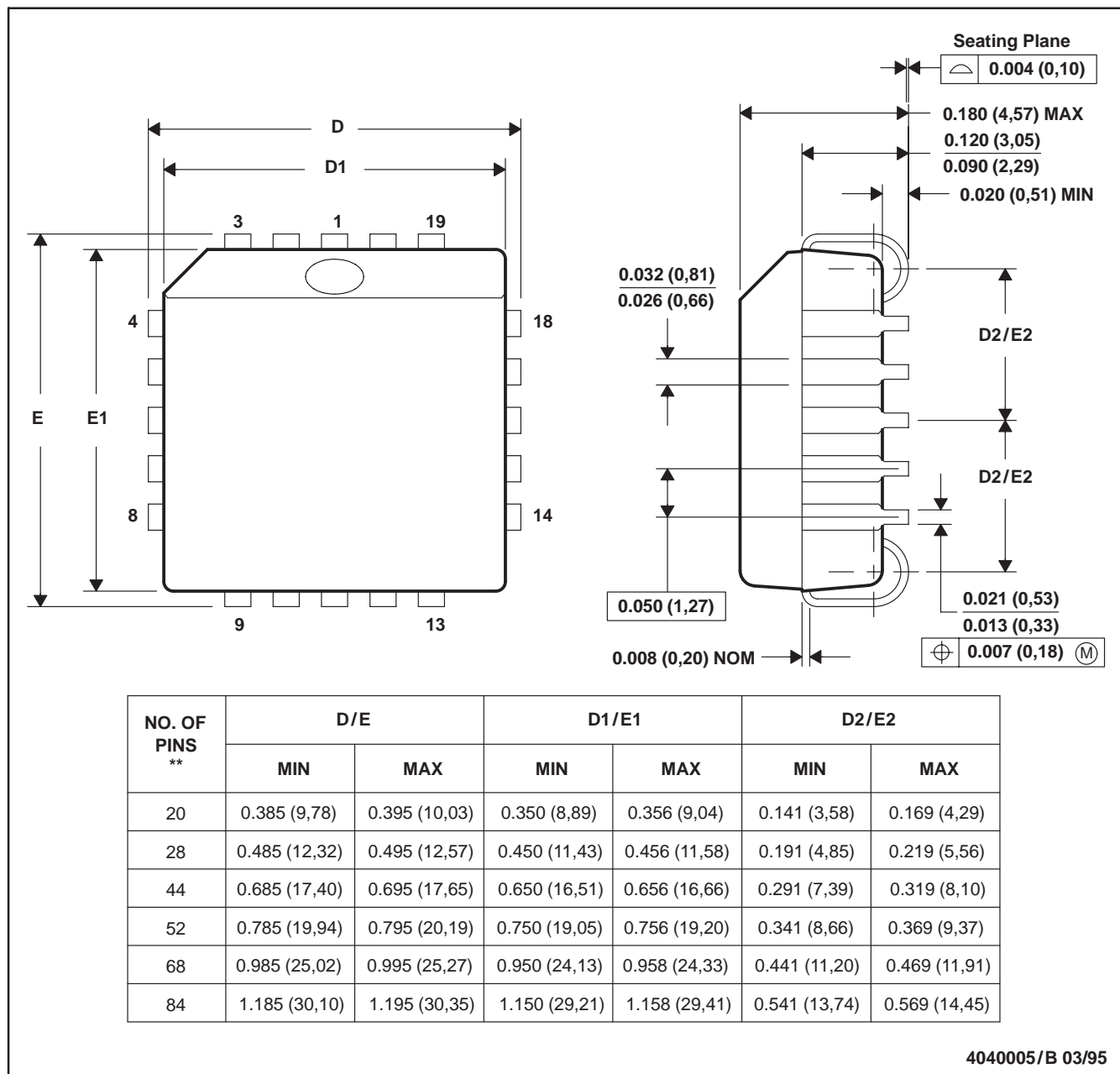
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.



FN (S-PQCC-J\*\*)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-018

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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